

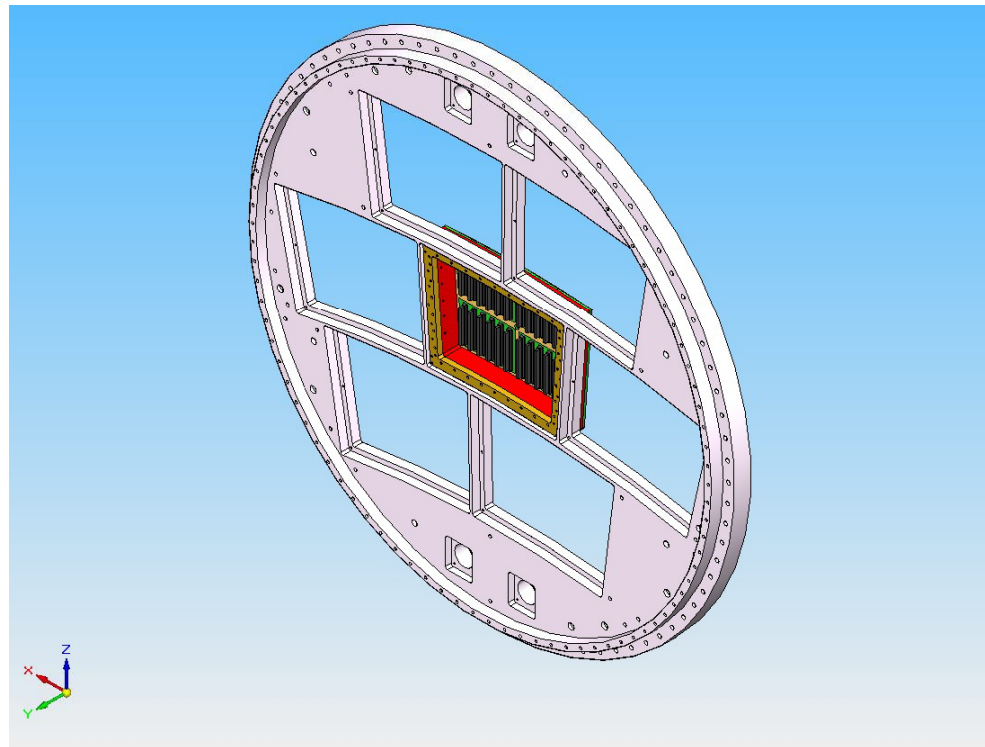
Resistive bulk Micromegas panels for the TPC

D. Attié, P. Colas, E. Delagnes, M. Dixit, A. Giganon, M. Riallot, F. Senée, S. Turnbull

Introduction

**Status of the Micromegas
Large Prototype panels**

**The four options for the
resistive coating**



Introduction

Avalanche size in Micromegas: 12-14 microns. => no natural charge sharing

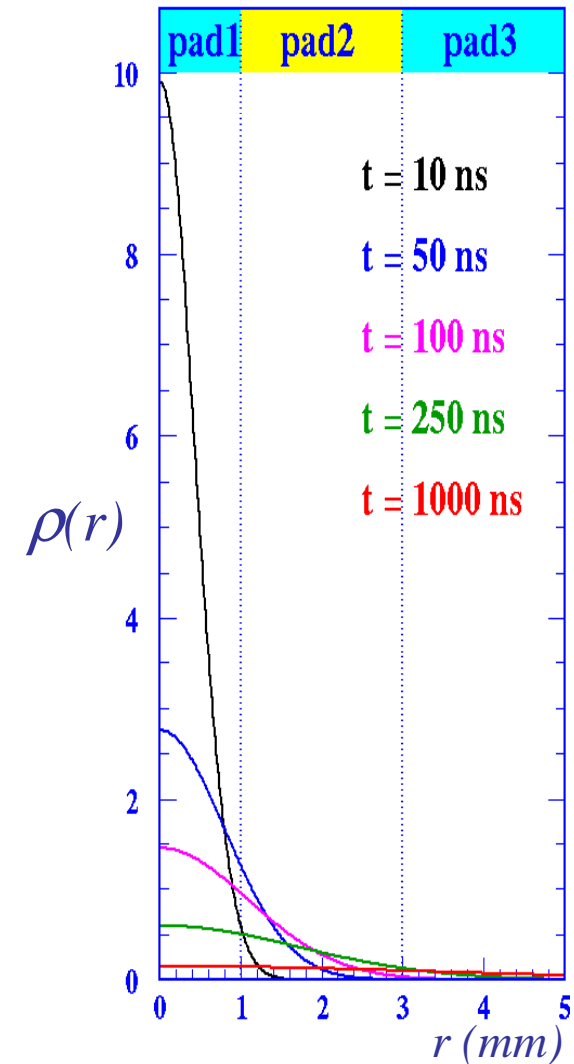
To obtain the best possible (diffusion-limited) resolution down to $z=0$, need to share the charge between pads

One solution (M. Dixit et al.) : use a continuous RC circuit to spread the charge.

In addition, by spreading the charge of sparks over space and time, they limit the effect of discharges.

On the other hand, bulk technique is mandatory to avoid dead areas and provide robustness

=> **Make compatible these two techniques**



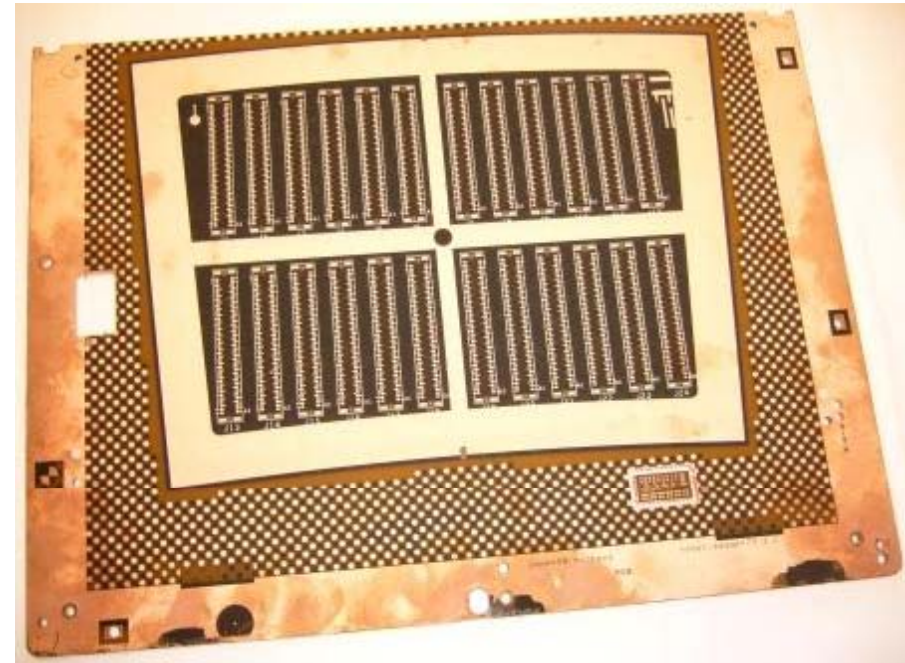
$$\frac{\partial \rho}{\partial t} = \frac{1}{RC} \left[\frac{\partial^2 \rho}{\partial r^2} + \frac{1}{r} \frac{\partial \rho}{\partial r} \right] \Rightarrow \rho(r, t) = \frac{RC}{2t} e^{-\frac{r^2 RC}{4t}}$$

The panels

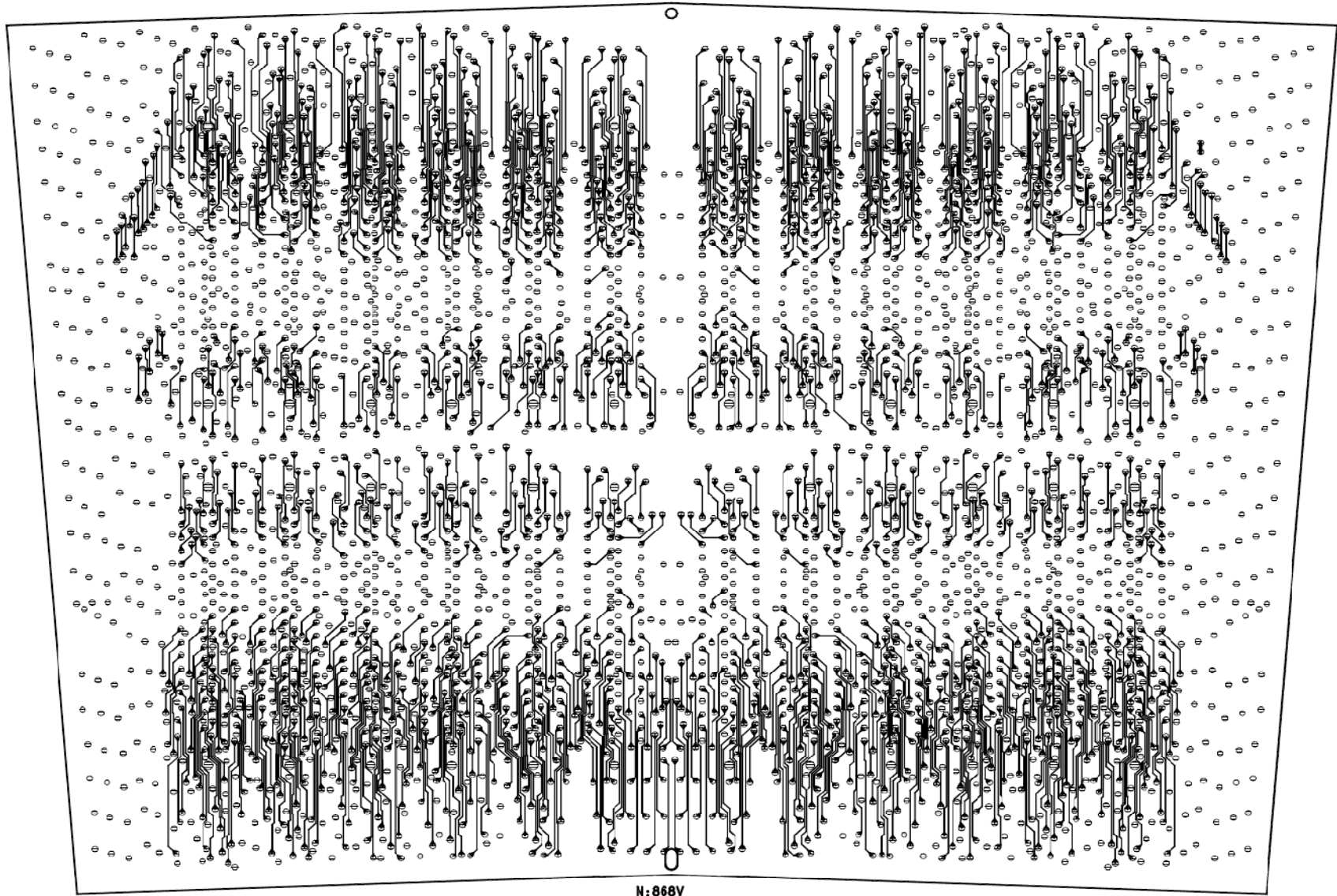
Two routings have been done

One in Saclay with 6 layers
(delivered early June)

One at CERN with 4 layers (to be
delivered next week)



HV



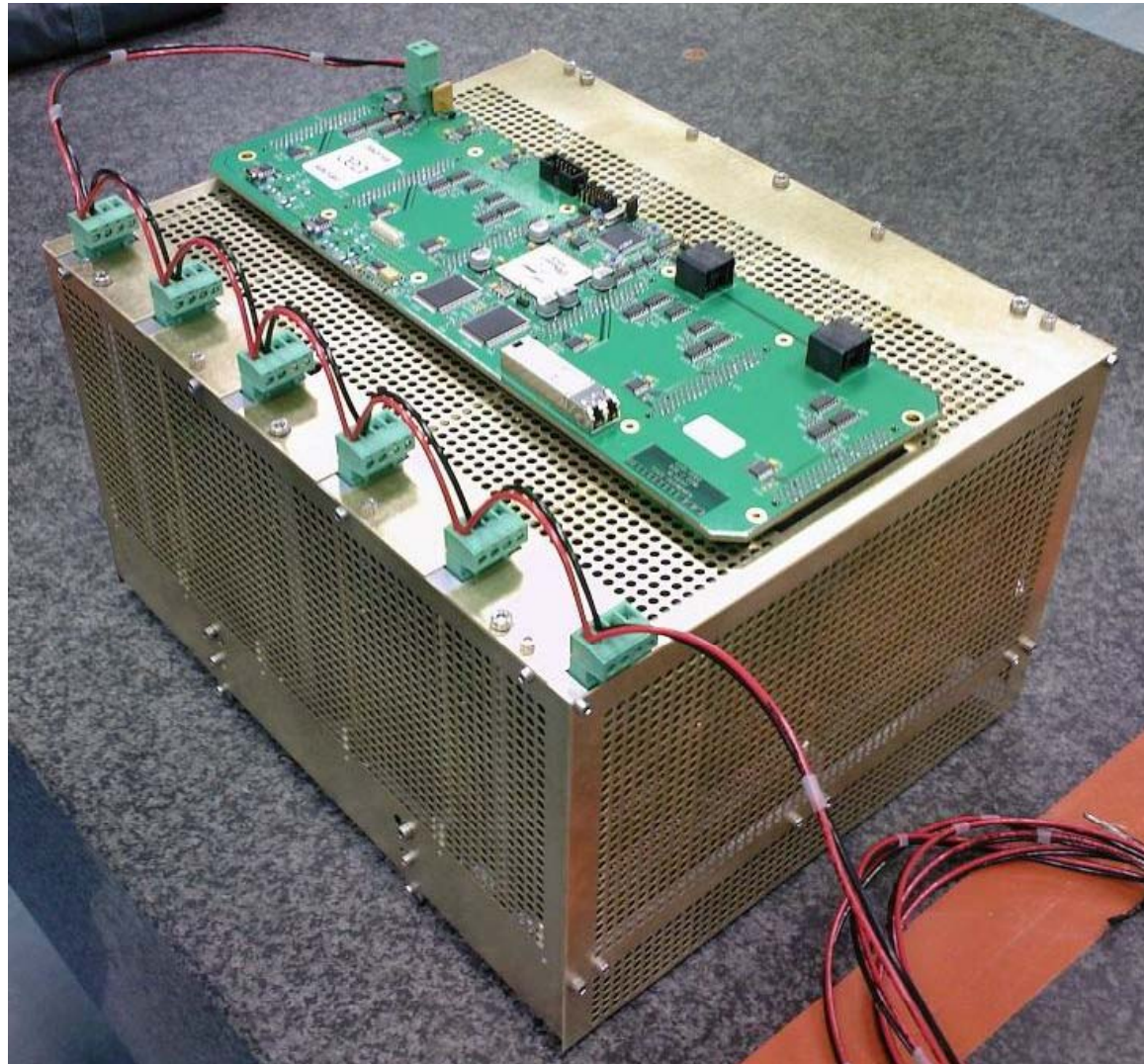
One of the 3 routing layers of the Saclay PCB

Mechanical support of the electronics

The AFTER-based (T2K) electronics has been fully commissioned.

The shielding and supporting structure for the cards has been assembled

The software for analysing pedestals (pad monitor) is up and running. (without shielding, the pedestal rms was already 4 ADC counts).

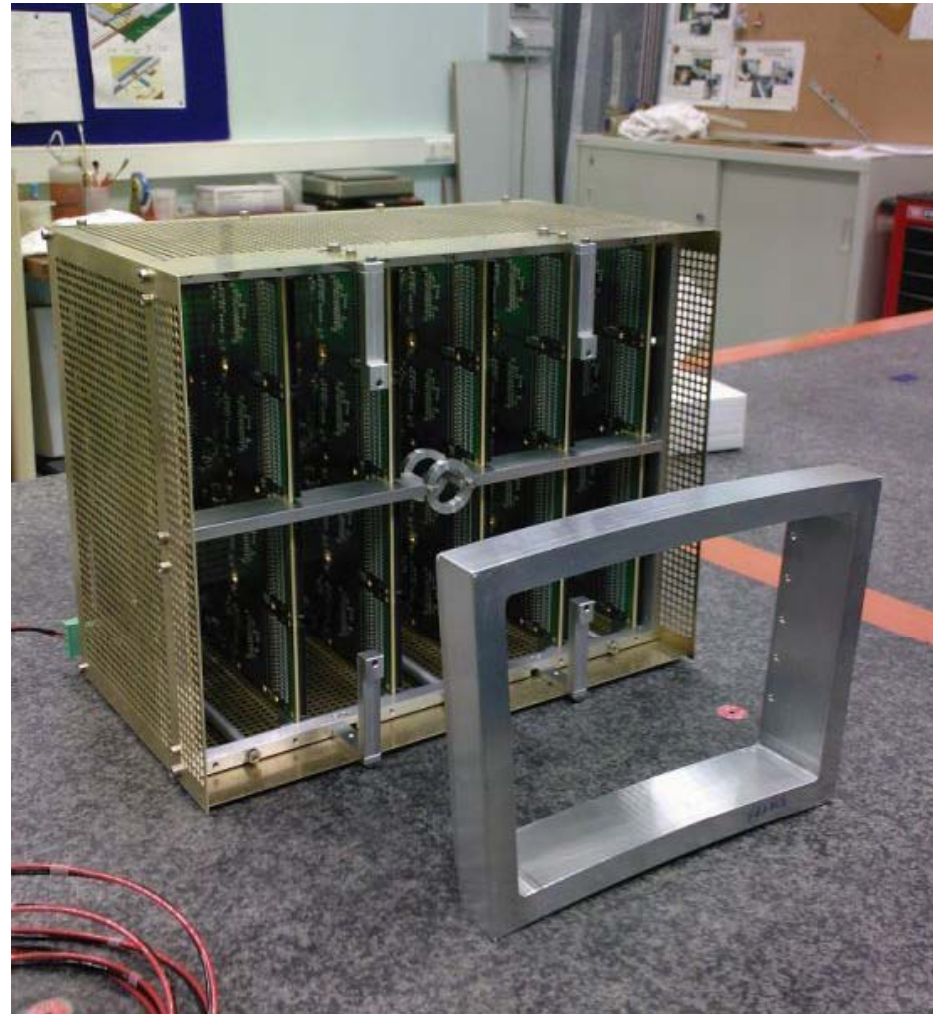


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P. Colas - Micromegas resistive panels

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Mechanical support of the electronics



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The problematic of resistive layers

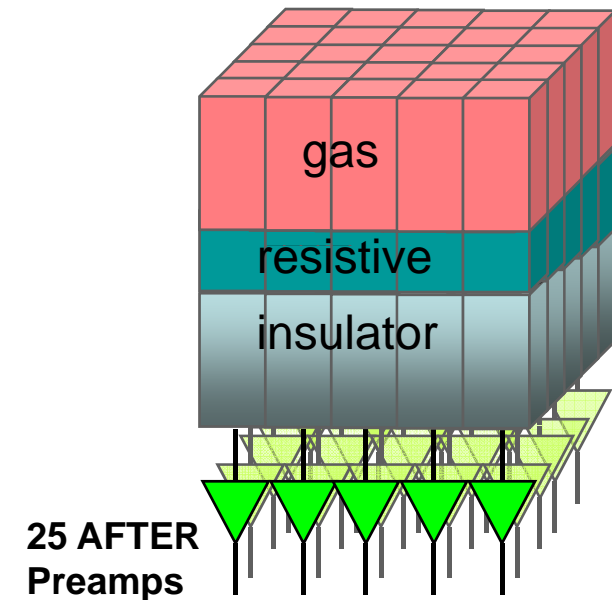
Resistive layers are difficult matter to work with.

They are often non-uniform, non-ohmic (the resistance depends on the voltage applied), they evolve with time (slow arrangements of dipoles, in the case of milled conductive solids in a resin).

In general the conductivity is governed by addition of tiny quantities of a dopant, so very difficult to master.

In addition, the market (mostly US) is rather closed, as high resistivity materials are used in radar furtiveness, or in high value applications as photovoltaics.

Simulations are on-going to optimise parameters (Analog Artist, E. Delagnes and S. Turnbull).



The 4 techniques. 1) resistively-covered kapton

This will be tried by Madhu Dixit on a Saclay panel. It is the following of the successful AlSi CERMET, but on kapton instead of mylar (Mylar would not stand the conditions for making bulks).

Sheets of diamond-like carbon ($10^{12} \Omega/\text{sq}$) have been sent to Rui de Oliveira at CERN for tests. By doping $10 \text{ MOhm}/\text{sq}$ should be possible

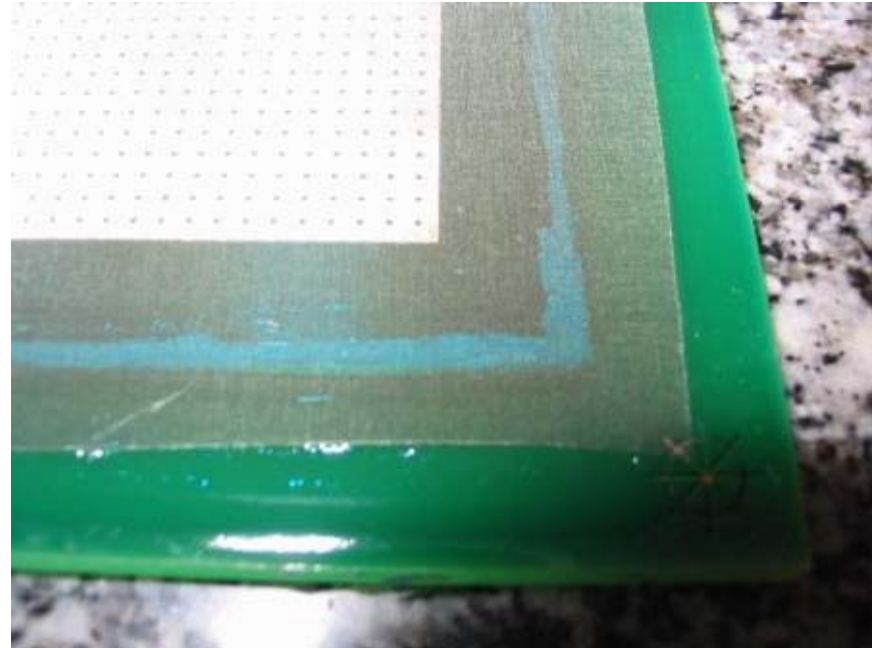
Also in the process to get an Yttrium-Al garnet.

The 4 techniques. 2) carbon-loaded kapton

This was the first technique used. It was abandoned since the resistivity was too low (0.5 M Ω /sq) and higher resistivities were not available.

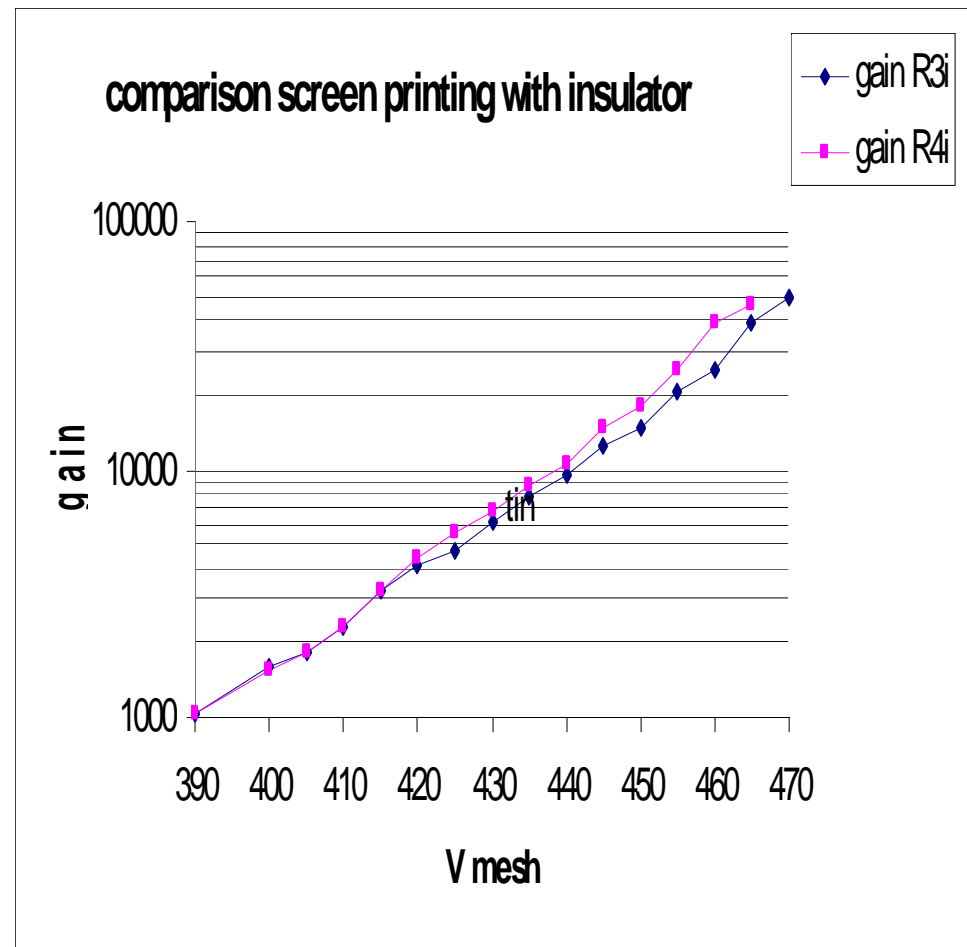
Rui de Oliveira managed to get a roll from Dupont, nominally 10 M Ω /sq (measured 2.7 M Ω /sq at 250 V)

2 prototypes will be made at CERN and this process will be tried on one of the CERN panels.



The 4 techniques. 3) prepreg + screen-printing

This has been tried at CERN. 2 prototypes of 10x10 cm (2 and 8 MOhm/sq) have been tried at Saclay. There is not clear evidence that they are spark protected. Even one of the detector has been damaged by the HV during the test. Still such a layer will be applied to a CERN panel.



The 4 techniques. 4) thin-layer deposition

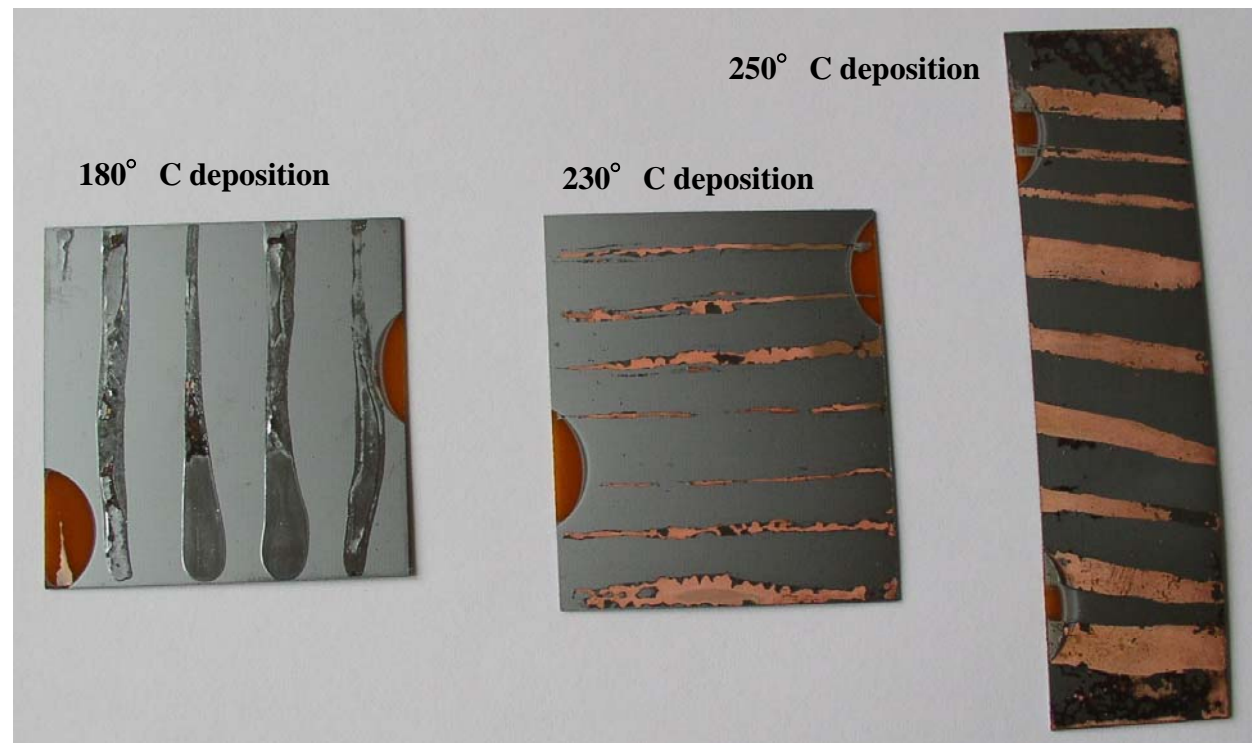
An agreement between CEA Saclay and Neuchatel University has been set up to study the feasibility and attempt to make a prototype from amorphous silicon deposition.

The first phase was to check that the NELCO 7000 PCB does not outgas, and perform tests of adherence and uniformity. These tests are in progress.

At 230 and 250 °C the resistive layer does not adhere to copper.

At 180 it adheres but peels off with time.

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The 4 techniques. 4) thin-layer deposition

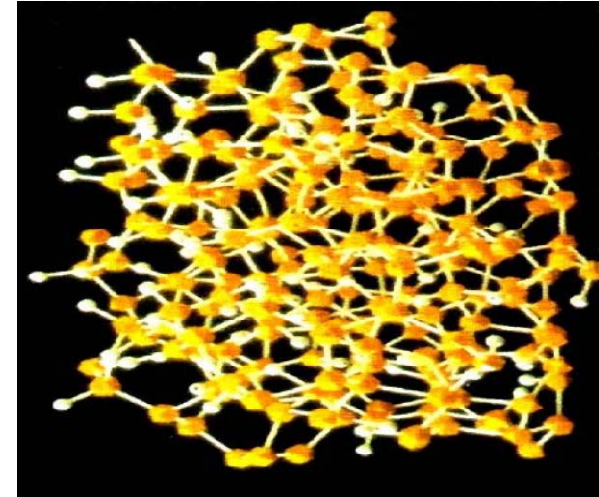
Orders of magnitude calculation :

We obtained good results with 75 micron insulator, $\epsilon_r = 2.5$, $R_{\text{surf}} = 1 \text{ M}\Omega/\text{sq}$

To keep the same RC, with aSiH as 'insulator' and doped aSiH (or another resistive deposition) on top, we calculate the resistivity of the top layer assuming 5 micron for the lower layer ($\epsilon_r = 11$) and 0.5 micron for the top layer.

This implies a surface resistivity of $15 \text{ k}\Omega/\text{sq}$, and a bulk resistivity of $0.75 \text{ }\Omega\cdot\text{cm}$.

It might be difficult to obtain such a low bulk resistivity by simple doping.



Conclusion

The basics mechanics, electronics and DAQ software are ready for the LP test. The bulk technique for applying the mesh is well established at CERN.

There is still some work for developing and optimising the resistive layer. A lot of work is going on at CERN, Saclay, Carleton and Neuchatel to this end.