AGH

Development of readout electronics for ILC Forward Calorimeter

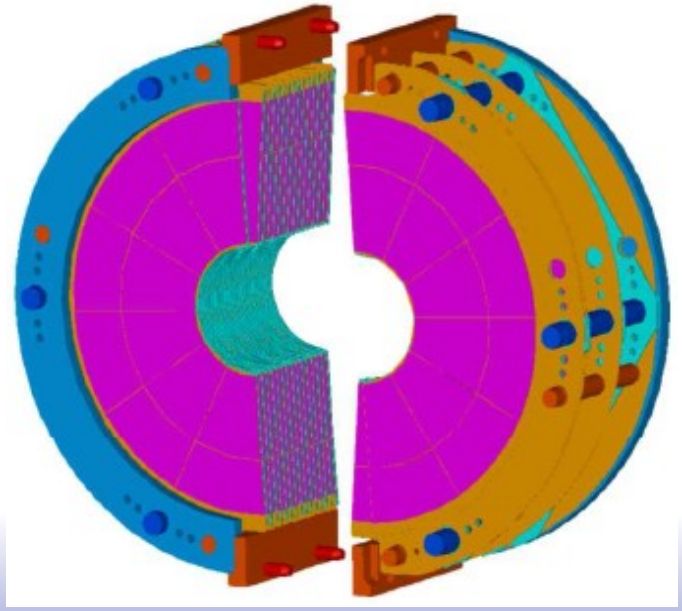
FCAL Collaboration
High precision design

Marek Idzik, AGH-UST Kraków

on behalf of the FCAL collaboration

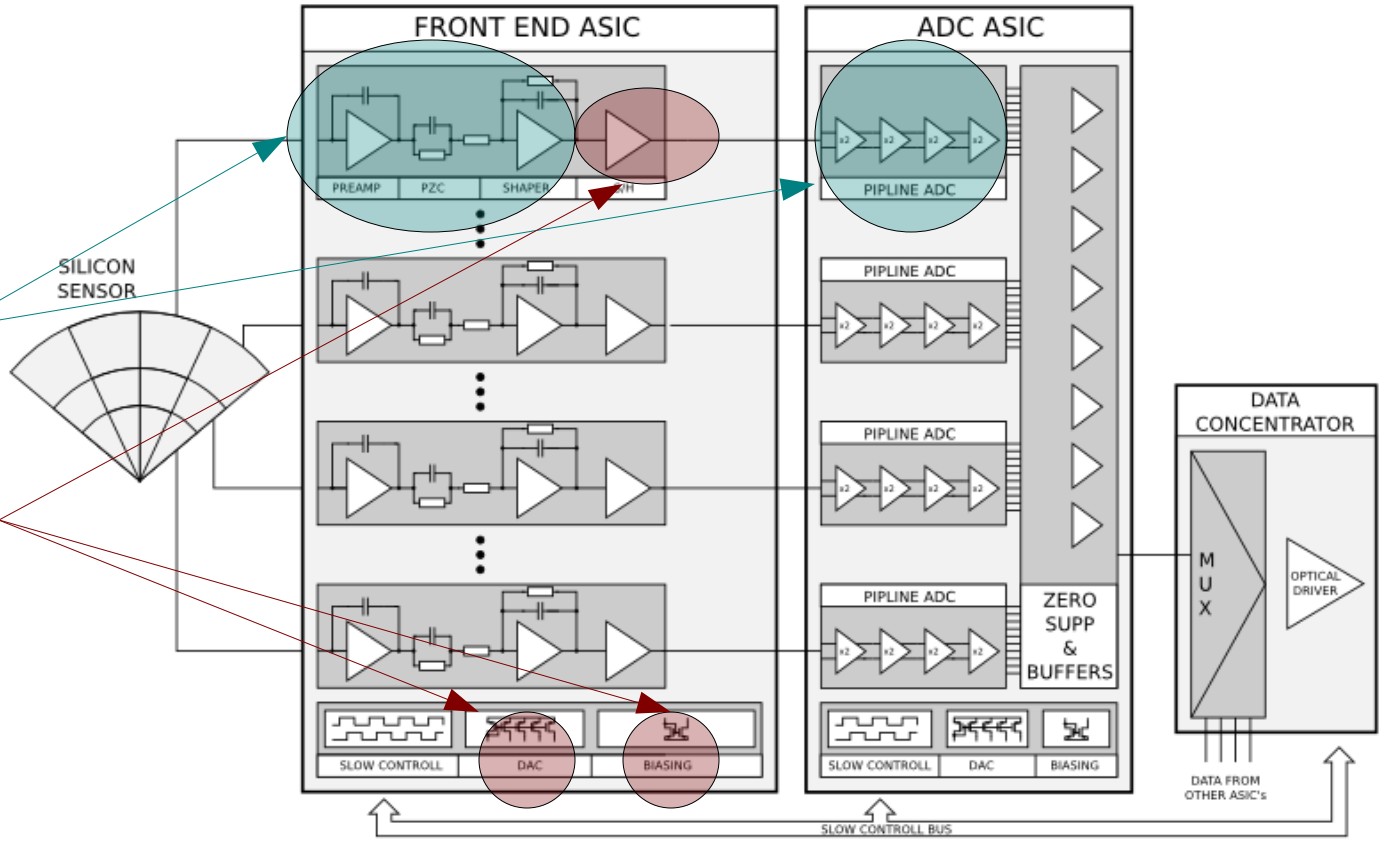
Outline

- LumiCal readout architecture & design
- Measurements of Front-end prototypes
- Measurements of ADC prototypes
- Summary & plans



LumiCal readout architecture

- Front-end (~32 channels) and ADC (? channels) ASIC
- First prototypes in AMS 0.35 μm
- Design in progress (S/H, DAC, Bias)



Challenges of LumiCal front-end

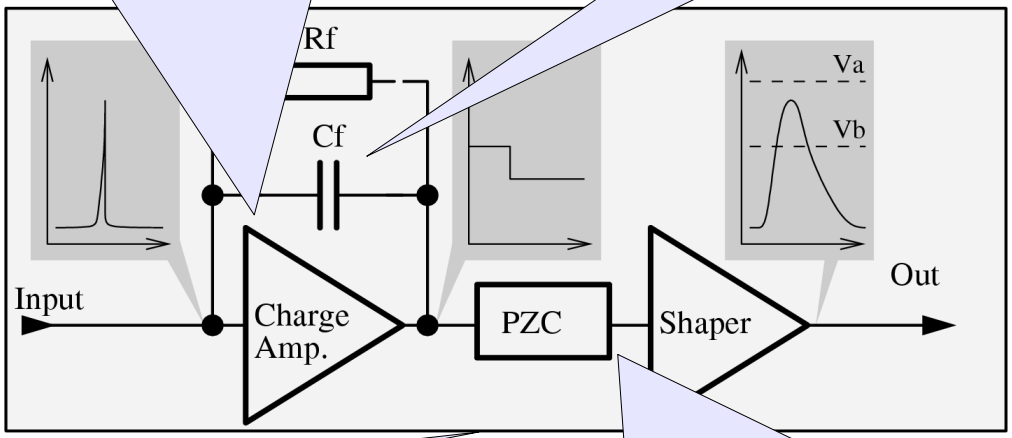
Large C_{det} range 10-100 pF

Calibration mode S/N~10 for MIP

Charge sensitive amplifier

Q_{max} ~ 10 pC

Cf ~ 10 pF



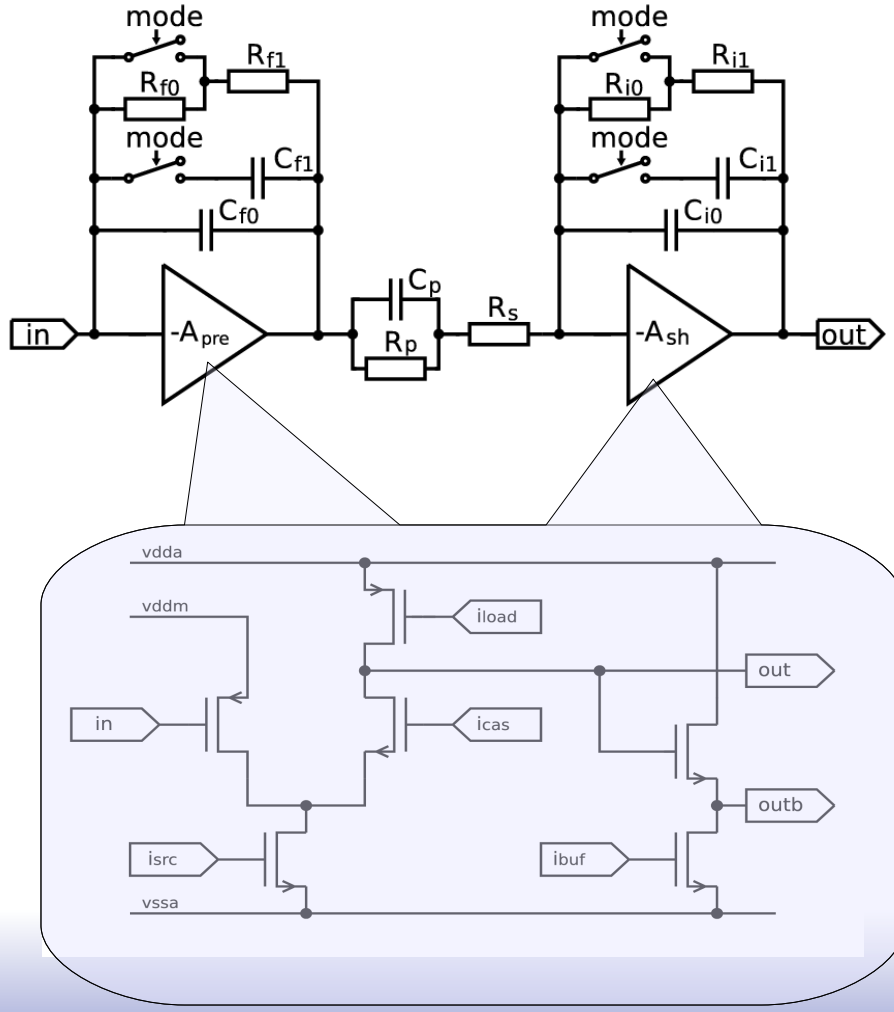
Calibration & Physics mode

Variable gain

Δt≃300 ns, high occupancy

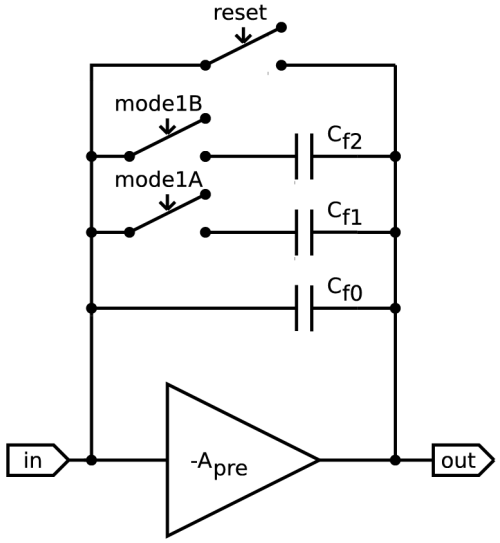
PZC +Shaper T_{peak} ~ 60ns

Front-end architecture

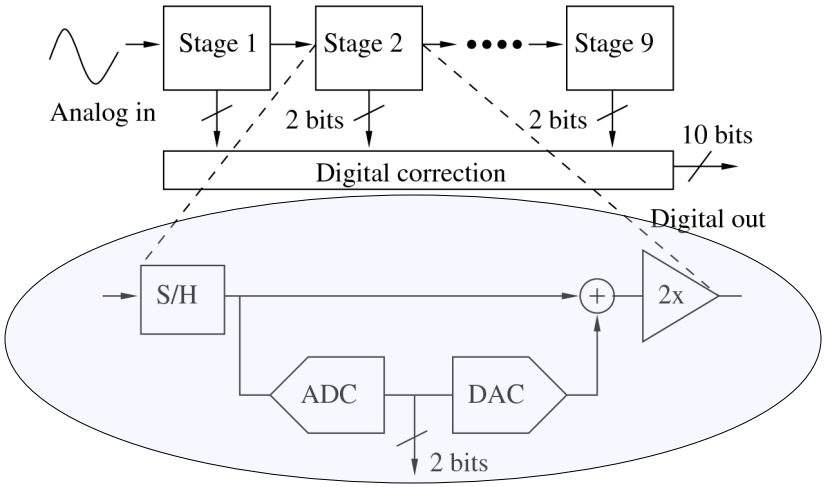


- Preamp. feedback: passive R_f or MOS
- Preamp: I_{pre}~2.5mA, PMOS input, Cf~10pF (physics), Cf~0.5pF (calibration)
- Shaper: 1st order, T_{peak}~60ns

Alternative configuration Gated-Reset



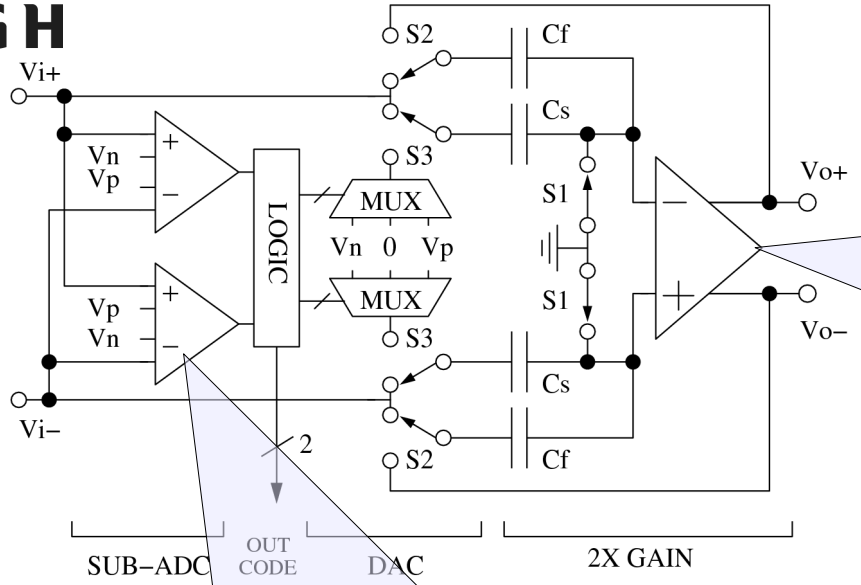
ADC architecture

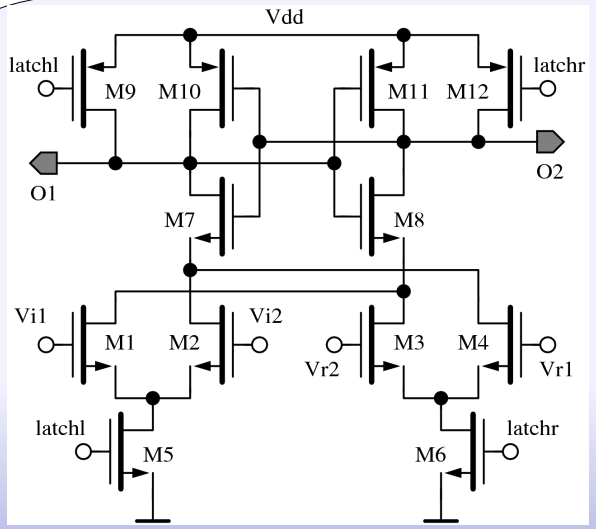


- Pipeline architecture
- 1.5 bit per stage
- Fully differential

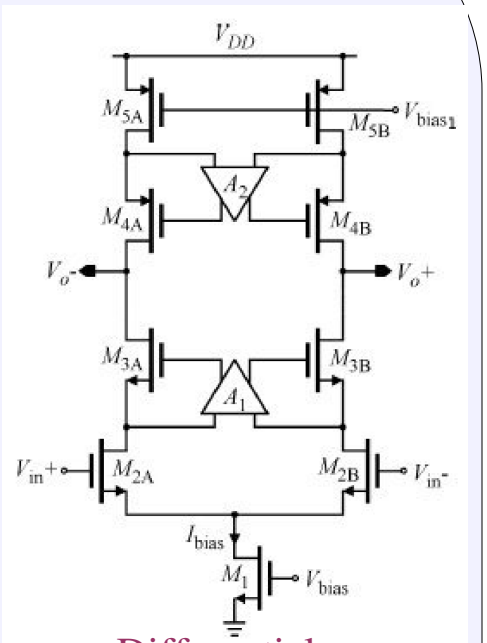
- 10 bits resolution
- Input dynamic range 2V
- Maximum sampling frequency 35 MHz
- Low power consumption

1.5 bit stage architecture





Dynamic latch comparators



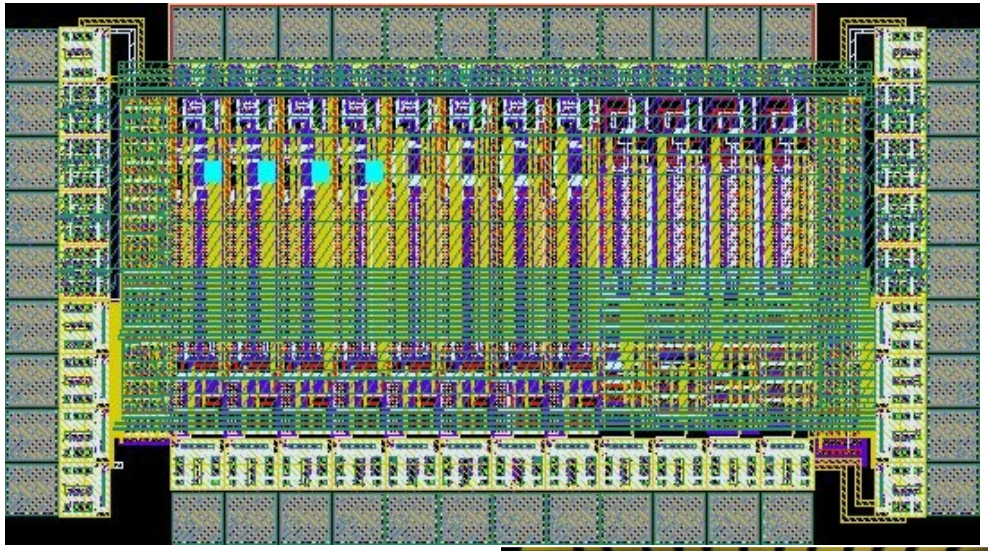
Differential amplifier with boosted gain

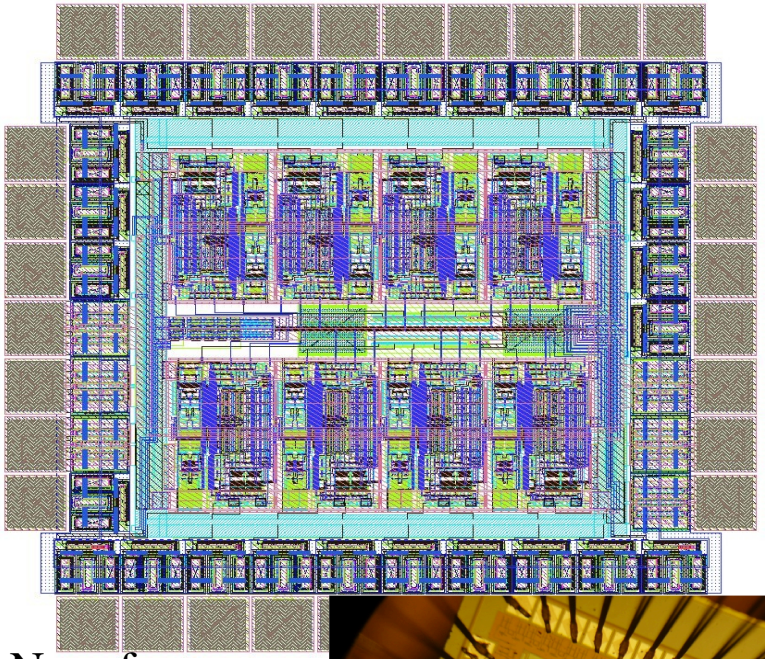
First prototypes

12 channels front-end ASIC

8 stages of pipeline ADC

submitted in June 2007



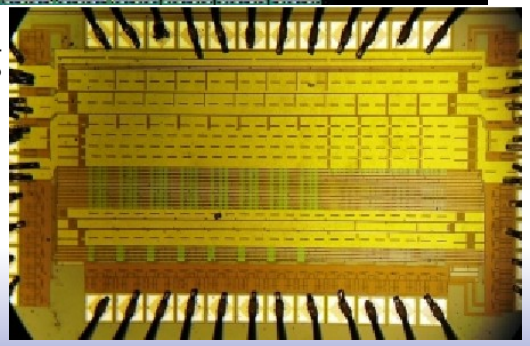


8 chan. - continuous shaping

4 passive Rf feedback

4 triode MOS feedback

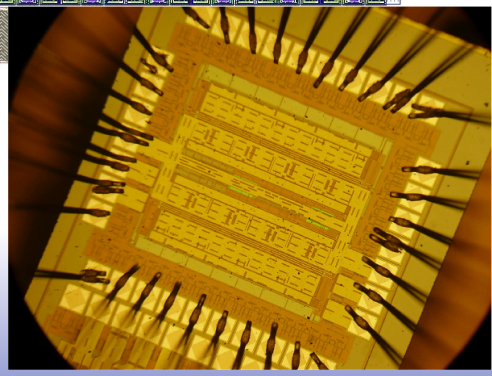
4 chan. - Gated-Reset



No reference voltages.

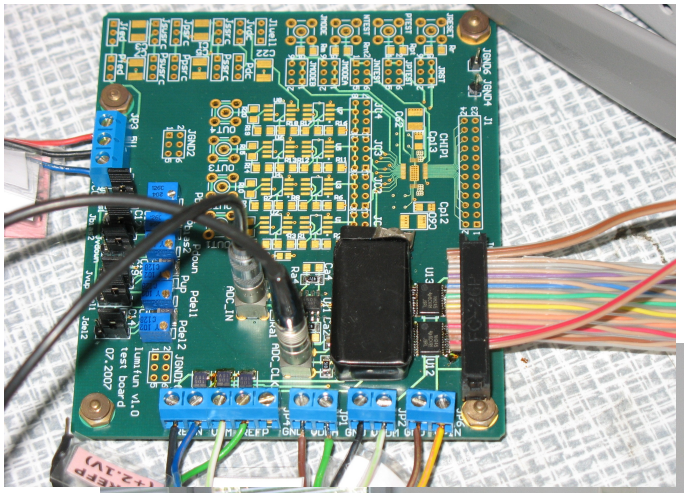
No digital correction.

No ...

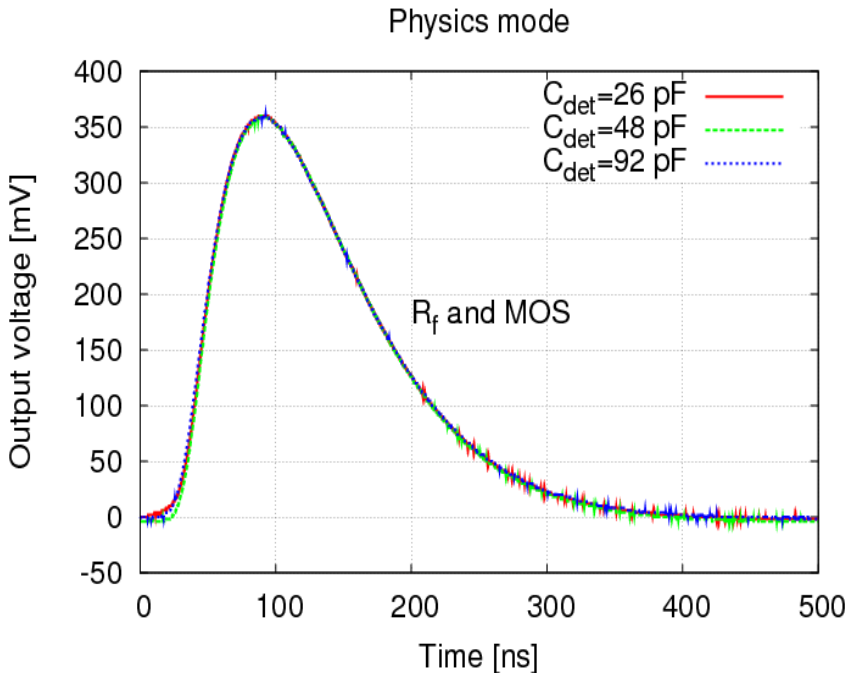


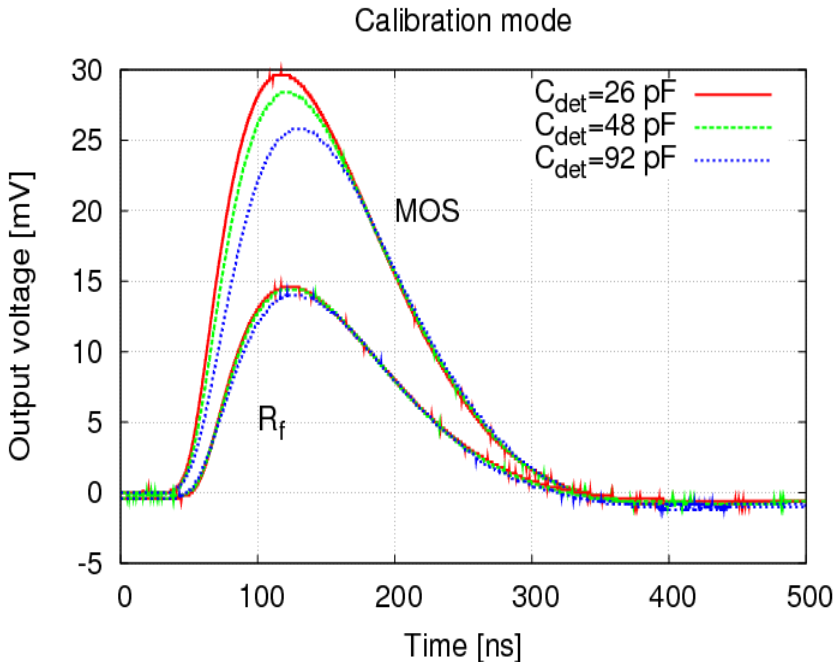
Front-end measurements

- 40 ASICs received
- PCB designed & produced
- Test Setup established
- Tests with generator and external capacitance. Tests with sensors just started at DESY
  - Pulse shape
  - Gain
  - Noise
  - Pulse rate
  - Crosstalk, Power consumption



Pulse shape

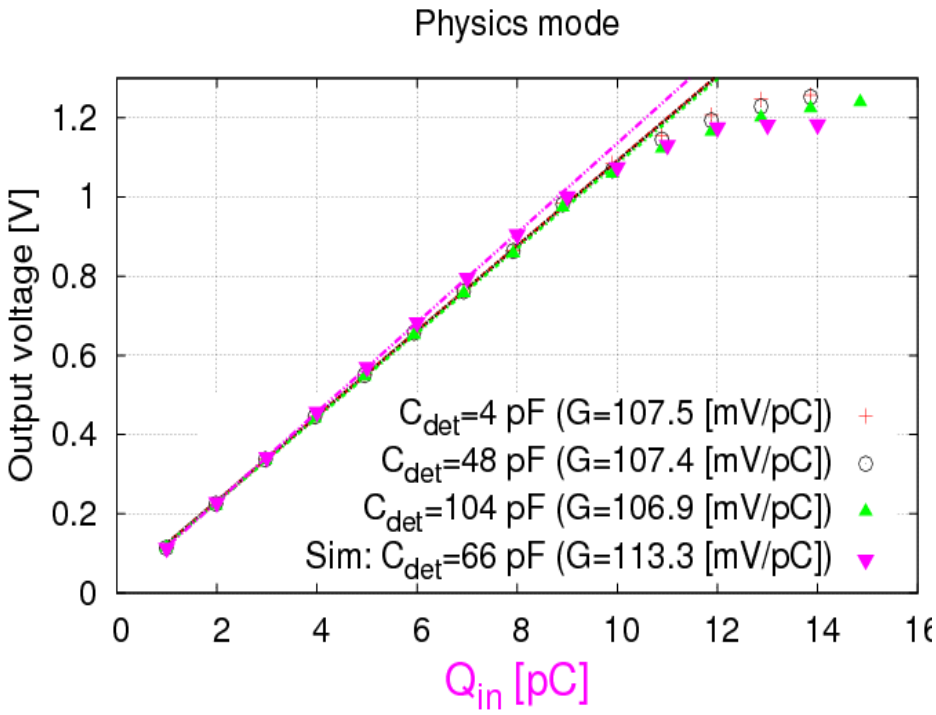


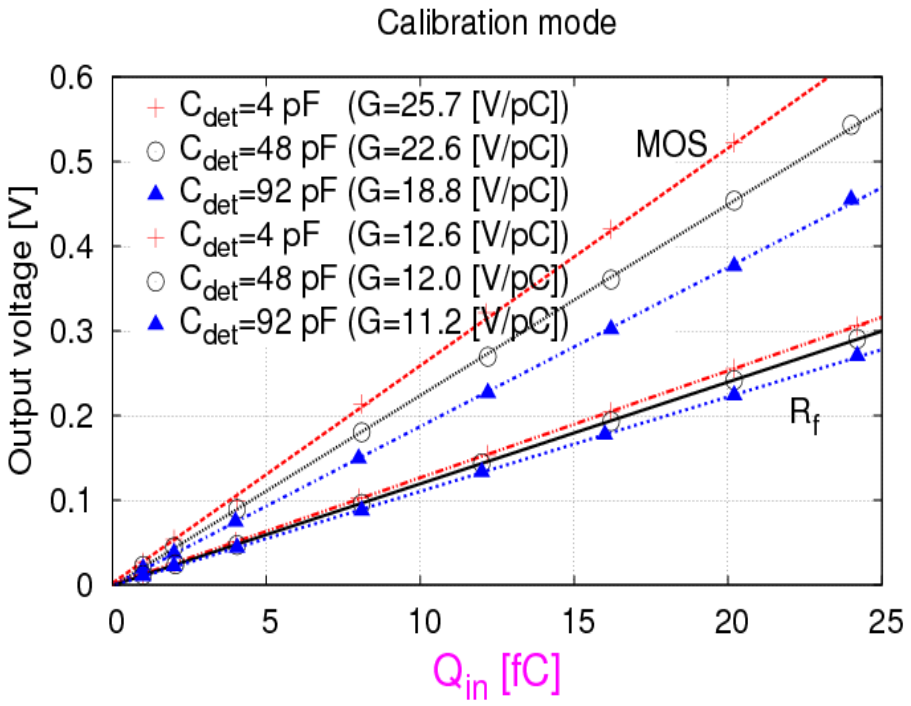


Very good charge sensitivity in physics mode (same for MOS and passive R_f feedback)

Slight sensor capacitance dependence in calibration mode (gain for MOS and R_f feedback different by design)

Gain

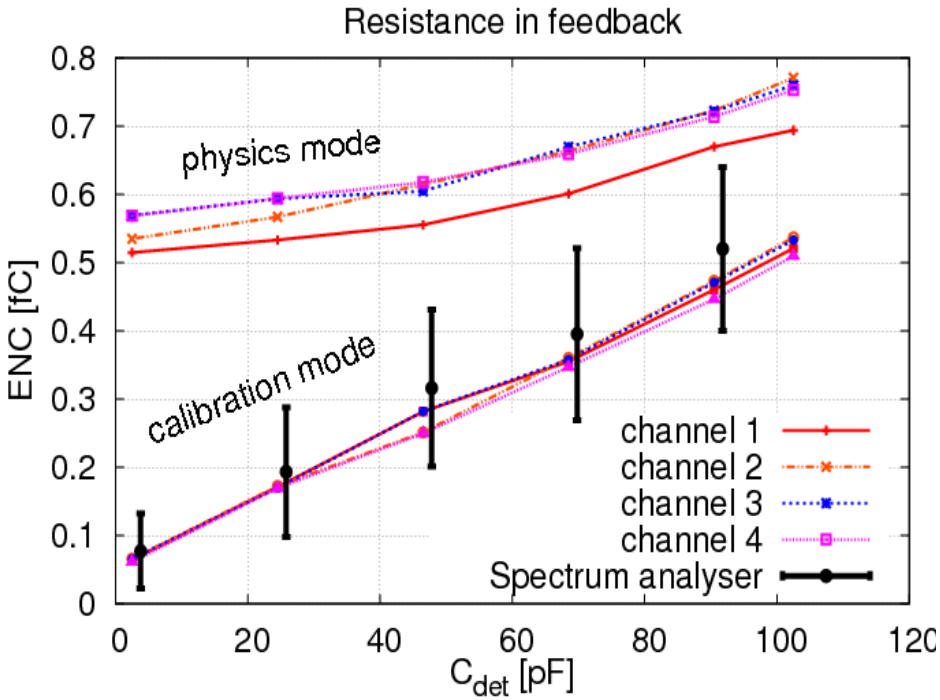


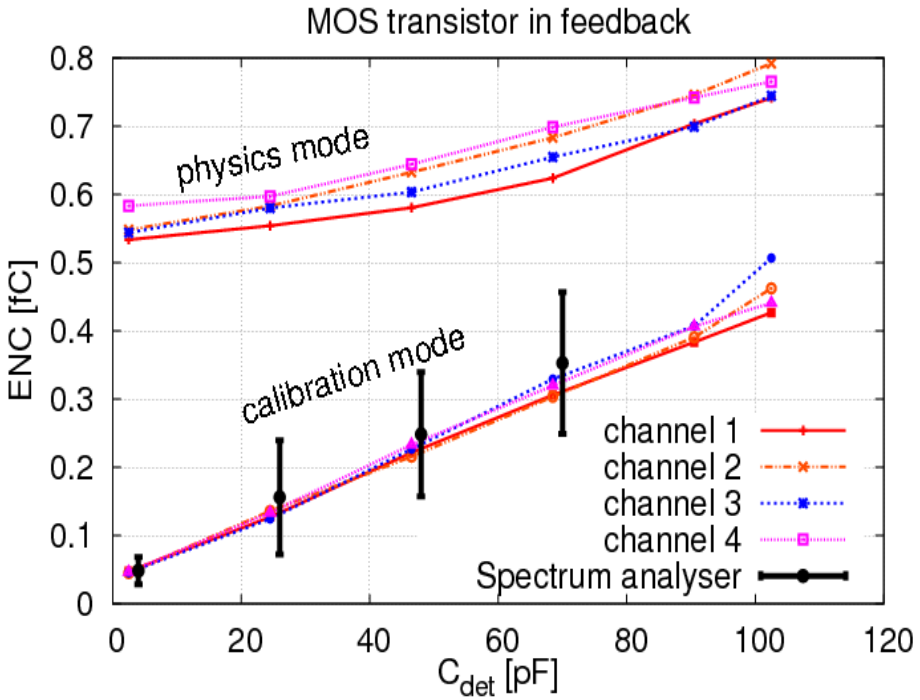


Constant gain in physics mode

Slight gain decrease with growing sensor capacitance in calibration mode

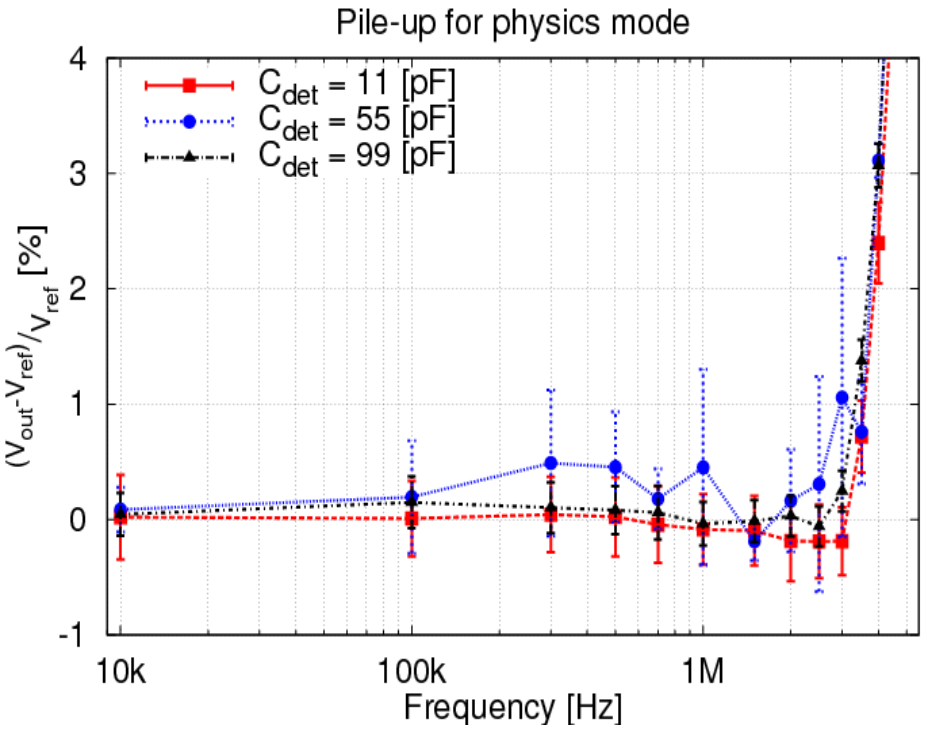
Noise

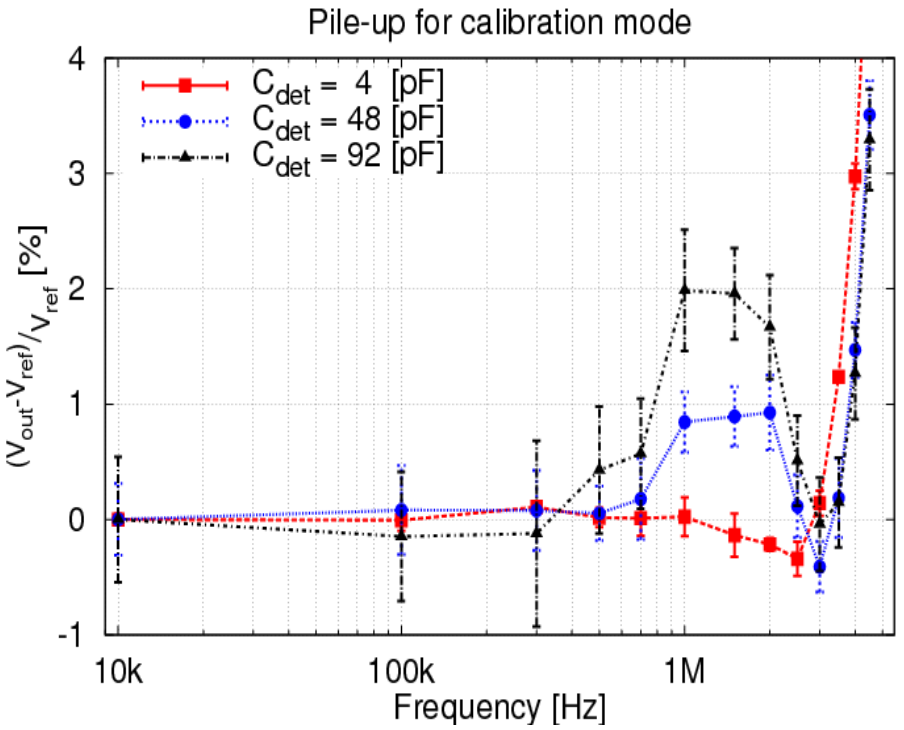




- *Measurements done with external capacitance. Need to be confirmed with sensor and particles*
- *In calibration mode noise below 0.4 fC - good MIP sensitivity (SNR > 10)*
- *Noise for MOS feedback similar to R_f Feedback*
- *Results with true RMS meter consistent with spectrum analyser*

Pulse rate





Front-end works well up to ~3 MHz continuous input rate. In calibration mode slight dependence on sensor capacitance – as expected from simulations

Crosstalk, Power

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Crosstalk measurements done with PIN photodiode and impinging laser light

Crosstalk		
Feedback:	**MOS**	**R_f**
Calibration	**0.08 %**	**0.25 %**
Physics	**0.95 %**	**1.5 %**

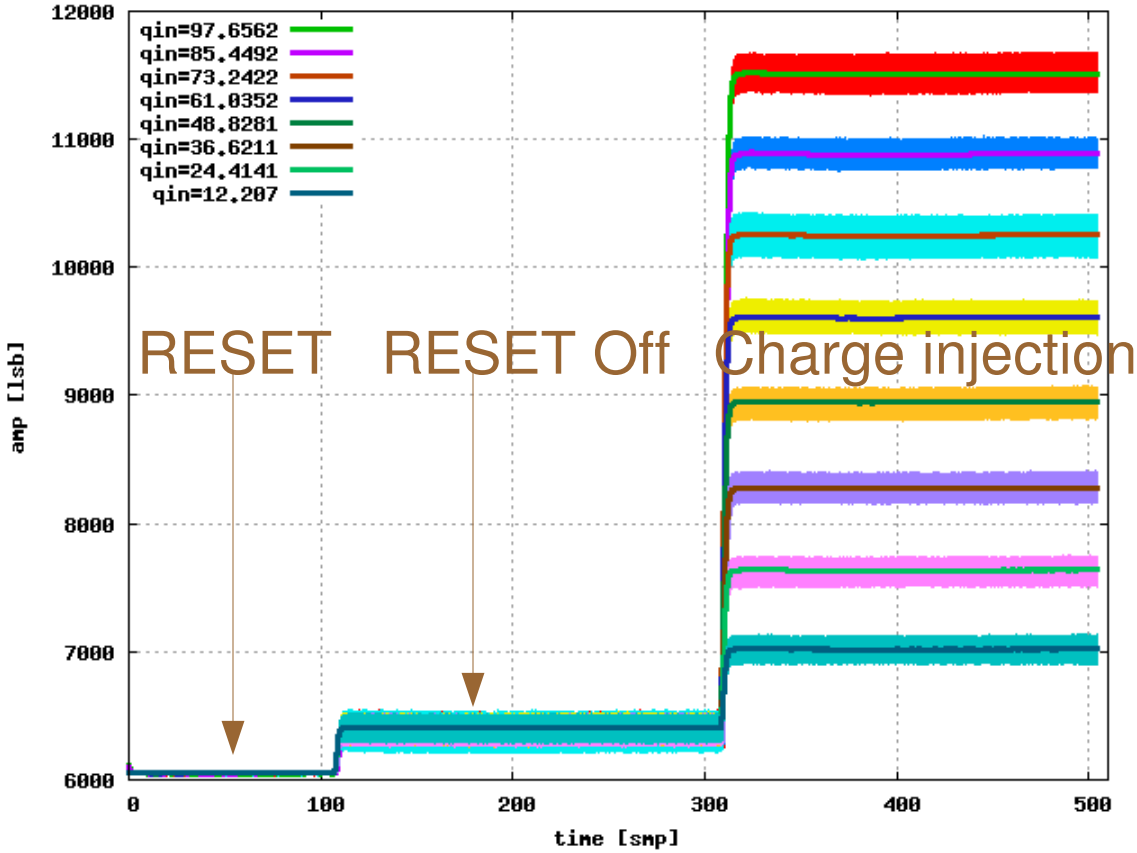
R_f area larger than MOS

Feedback capacitance area in physics mode larger than in calibration

Work on Layout needed

Power consumption about 8.9 $^{mW}/_{channel}$ consistent with simulations.

Gated-Reset prototype

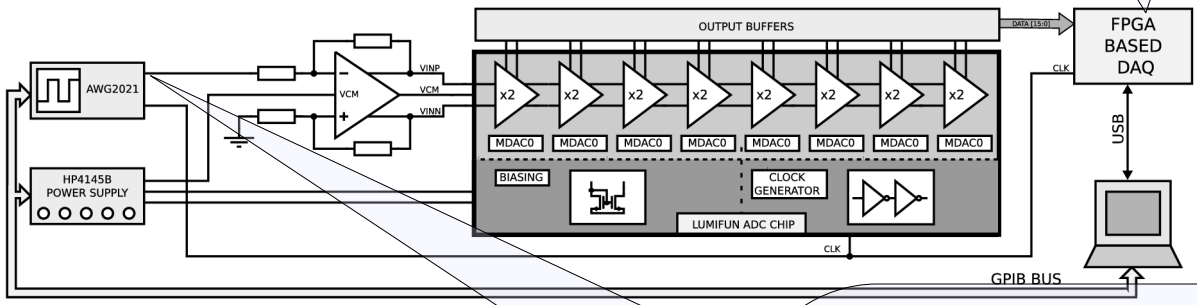


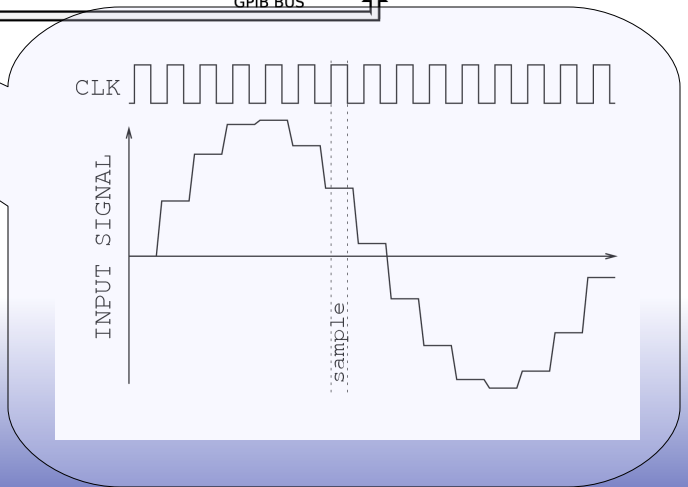
- Gated-Reset charge amplifier fully functional
- Measurements in progress...

ADC measurements

- 40 ASICs received
- PCB designed & produced
- FPGA based setup allowing full ADC characterization

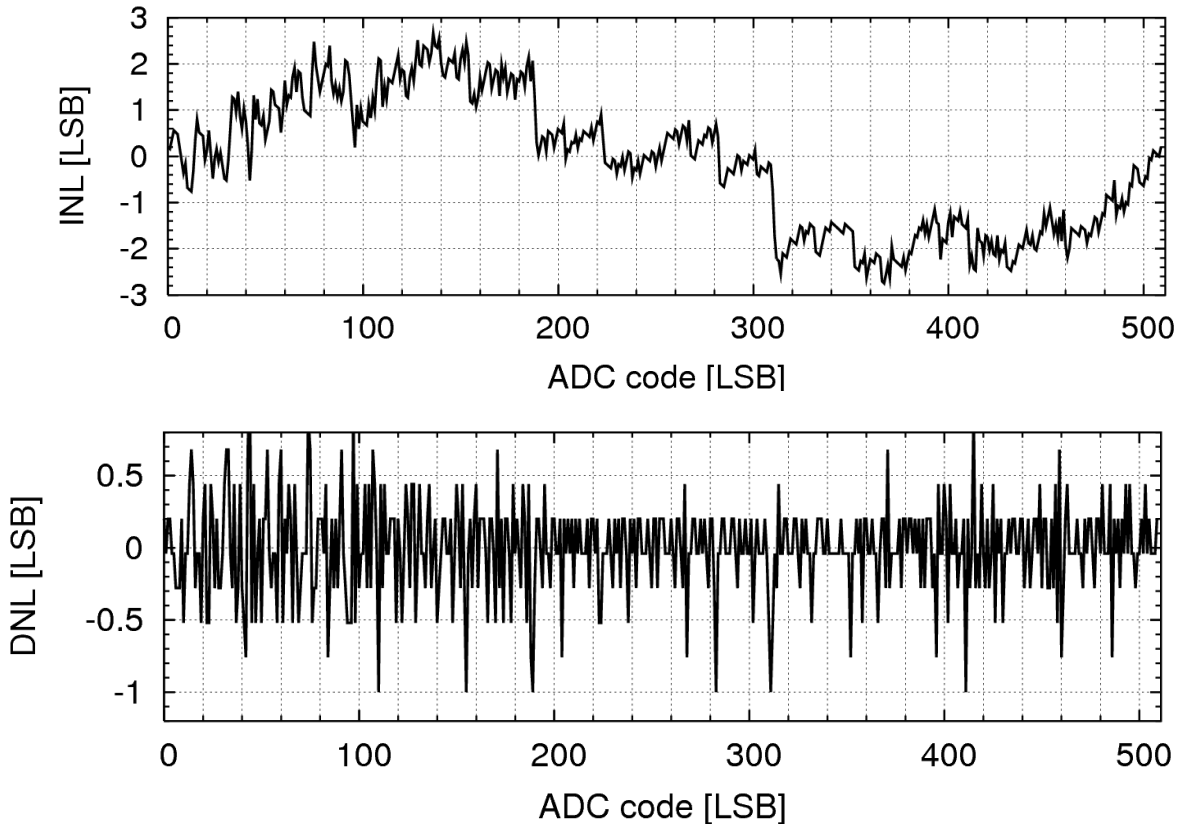
DAQ working up to ~120MHz sampling frequency





- Static measurements
  - INL, DNL, ENOB
- Dynamic FFT measurements
  - SNHR, THD, SFDR, SINAD, ENOB

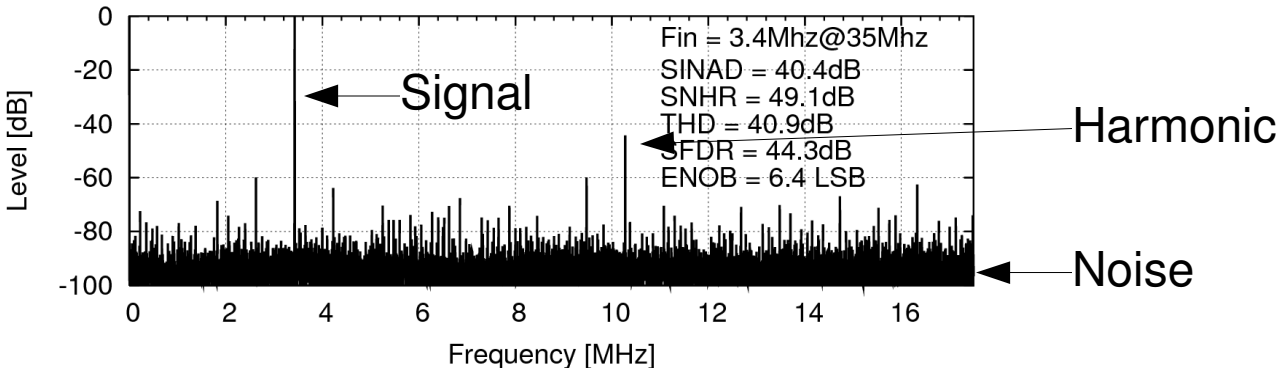
Static ADC tests



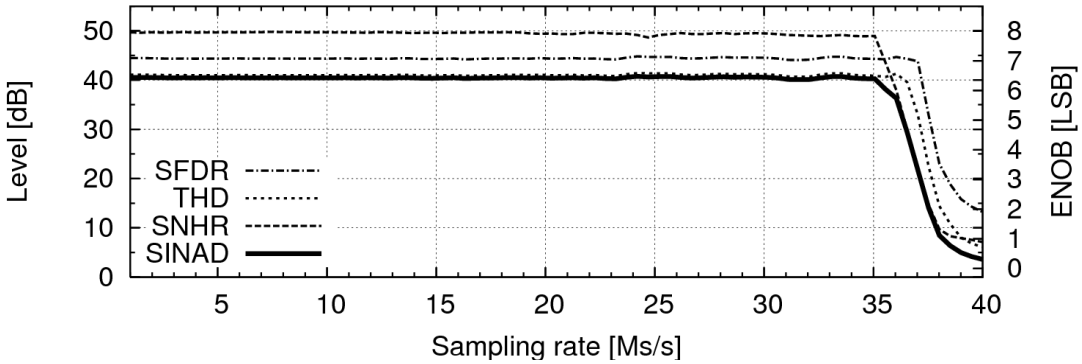
- Maximum Integral Nonlinearity found ± 2.5LSB, could be improved
- Differential Nonlinearity generally OK, but few missing codes found (DNL=-1) need to be corrected

Dynamic FFT ADC tests

Example of FFT spectra



Results



- Stable functionality up to 35 MHz in agreement with simulations
- Harmonic distortions (THD) limit the resolution, to be improved

Measurements status

- First prototypes of front-end channels and pipeline ADC stages designed, produced and found fully functional
- Front-end parameters measurements completed, in good agreement with simulations. Measurements with sensors and fanout still needed.
- Final front-end architecture not yet decided (continuous, gated...?)
- Setup for ADC measurements established
- Pipeline ADC stages measurements completed. Small nonlinearity errors found, their sources identified

Summary & milestones

- First front-end and ADC prototypes successfully tested
- Few months of delay according to initial schedule (partially because the sensors has not been produced yet)
- Improved ADC version being prepared for submission - design finished, layout in progress
- Track&Hold - design completed, layout started
- DACs - design almost completed
- Bandgap references - design almost completed
- Next submission – september 2008