# Silicon tracking DAQ

## Still preliminary thoughts on all DAQ parts but the first one (FEE)

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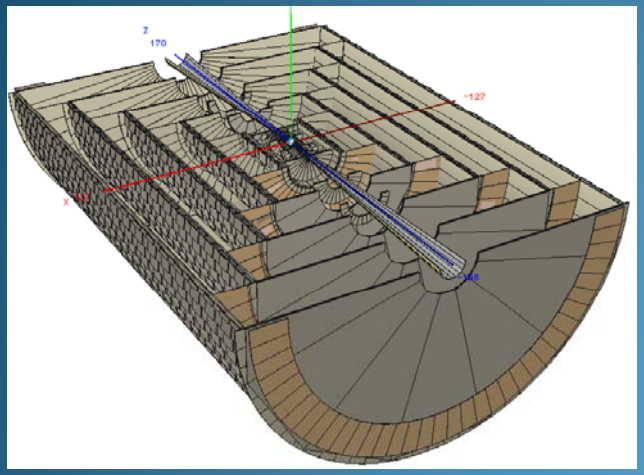
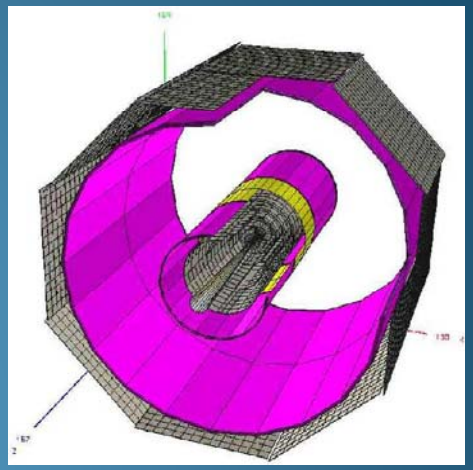
*This work is performed within the SiLC R&D collaboration and with partial support from E.U. I3-FP6 EUDET project support*

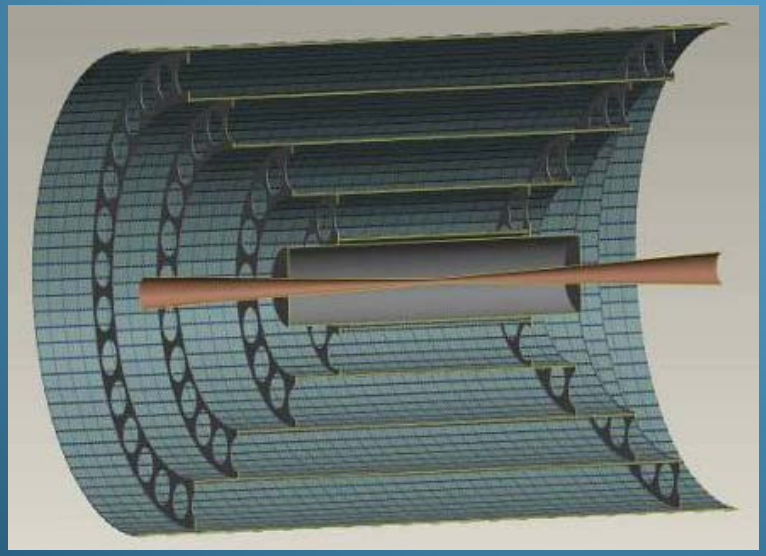
*ILC ECFA Workshop at Warsaw, June 11 2008*

# PRELIMINARY WARNING



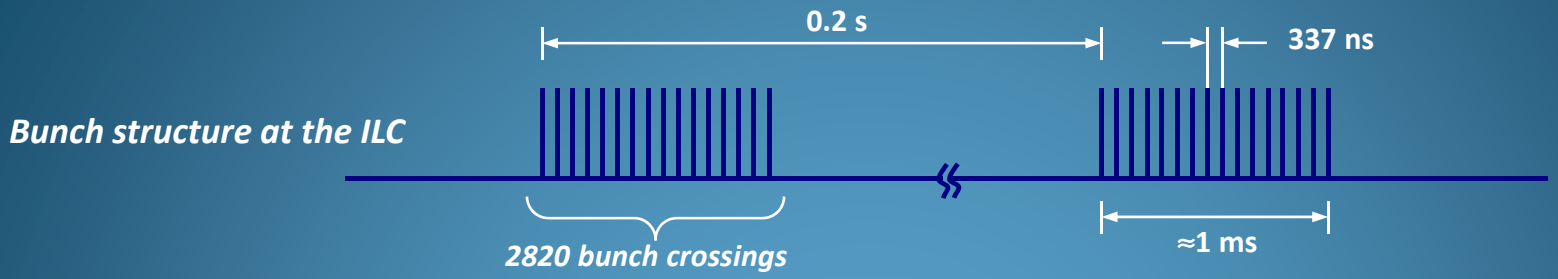
All what is presented here apply to any Si tracking system for ILC, made with strip sensors and representing a few 10**6 channels to be read out and processed





Not applied (yet)! to a all pixel large area Si tracking (30 x 10**9 pixel channels )

# THE TIME WE ARE GIVEN....




## HOW DO WE USE IT?

- numerical oscilloscopy
- storing
- zero suppressing

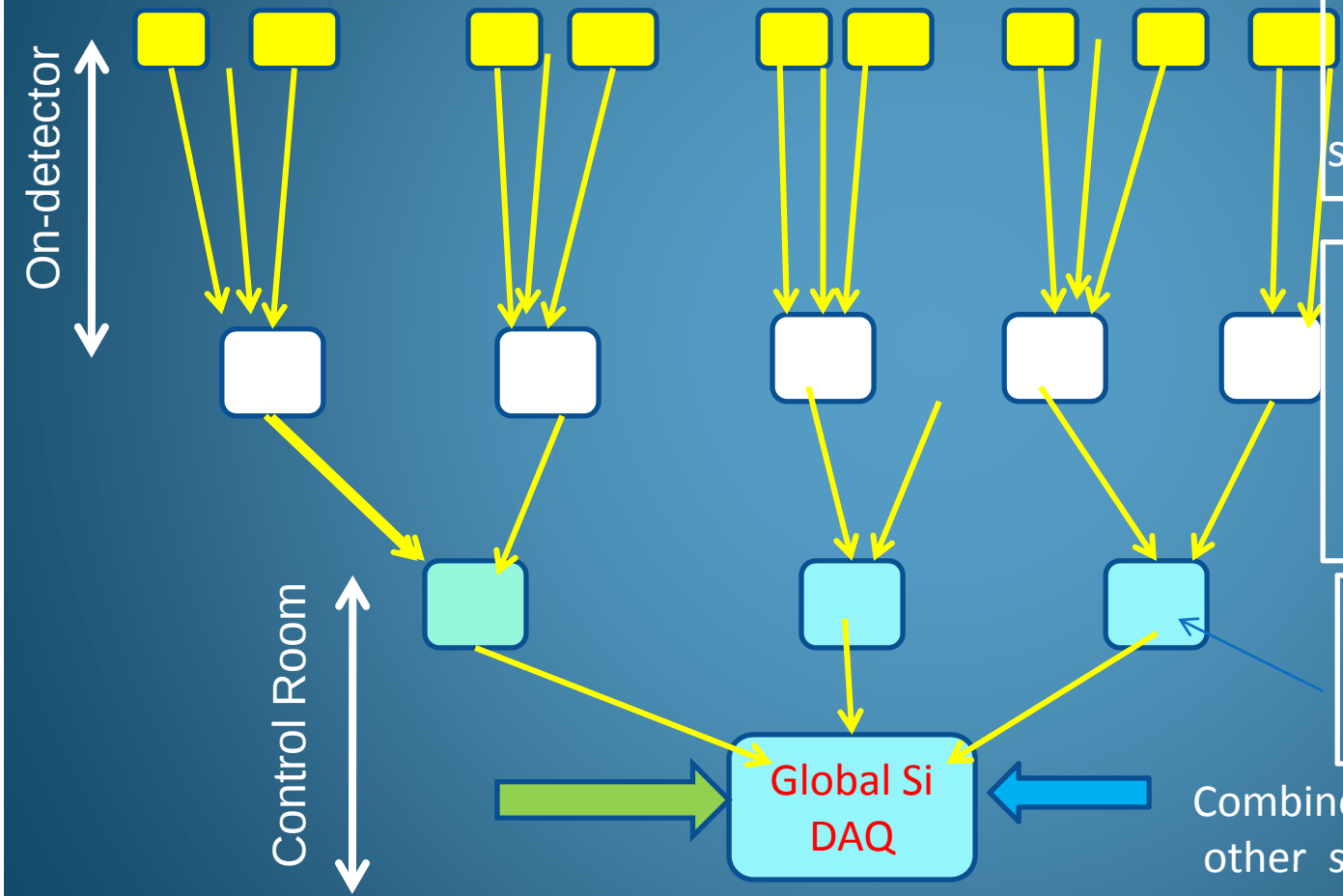
## THEN:

- A/D conversion
- power cycling
- calibrating (?)

# TOPICS

- SILICON TRACKING DAQ: 3 FLOORS
- FLOOR 1: on the chip
- FLOOR 2: on the detector sides
- FLOOR 3: in the Control Room
- Towards developing this DAQ architecture:
  the first steps

# Si Tracking DAQ architecture into 3 floors



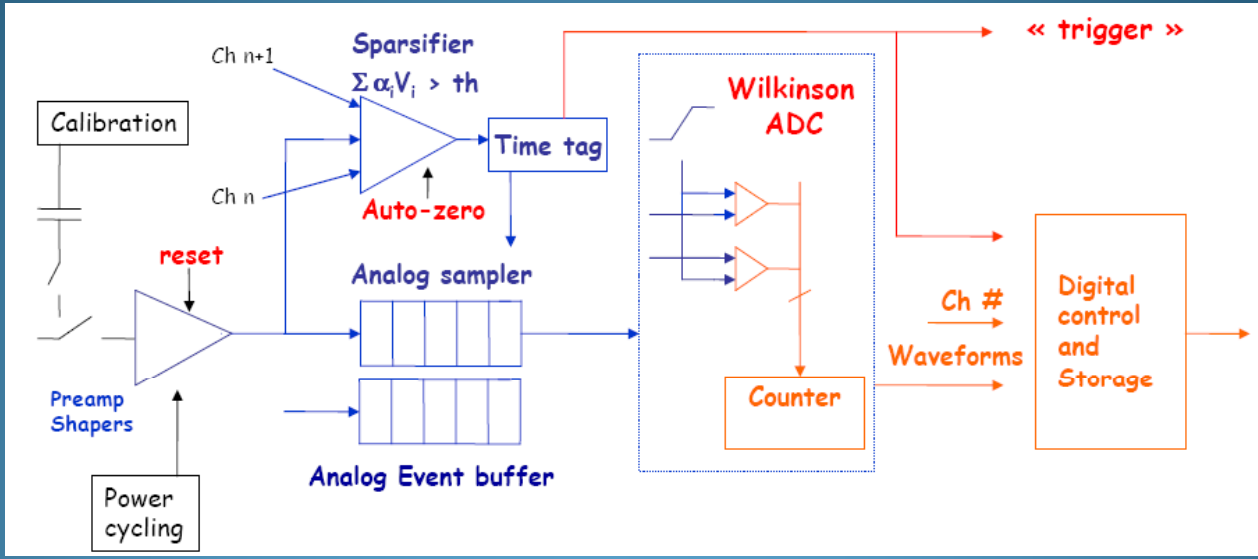

F 1: chip on sensor, Full read out chain in a single chip (A/D, zero suppress, multiplex, F.T.

F2: on detector sides, Daisy chaining chips information from chips, buffering, preprocess, interface/outside world

F3: in control room, processing /azimuthal sector, trk reconstruct.

Combine with Information from other sub-detectors, handling slow control for all Si TrK system

# Floor 1: FE chip on elementary module




***Full readout chain integration in a single chip, 512 or 1024 ch in 90nmCMOS***

- Preamp-shaper
- Sparsification Trigger decision on analogue sums (3 or 5 adjacent channels)
- Sampling 8-deep sampling analogue pipe-line
- Analogue event buffering: Occupancy: 8-16 deep event buffer
- On-chip digitization 12-bit ADC (highly multpiplexed)
- Buffering and pre-processing: Centroids, χ2 fits, lossless compression & error codes
- Calibration and calibration management

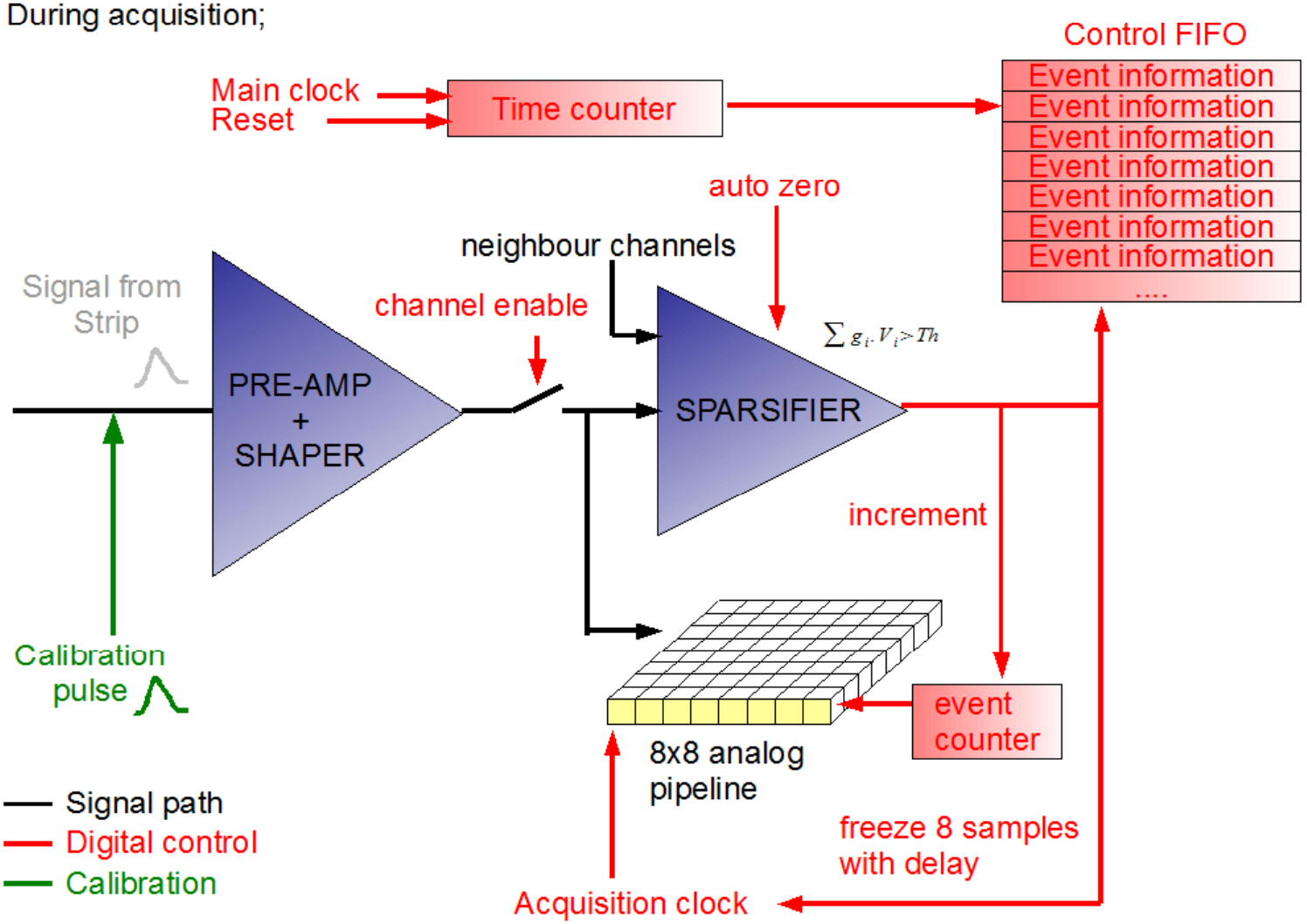
-Power switching (ILC duty cycle)

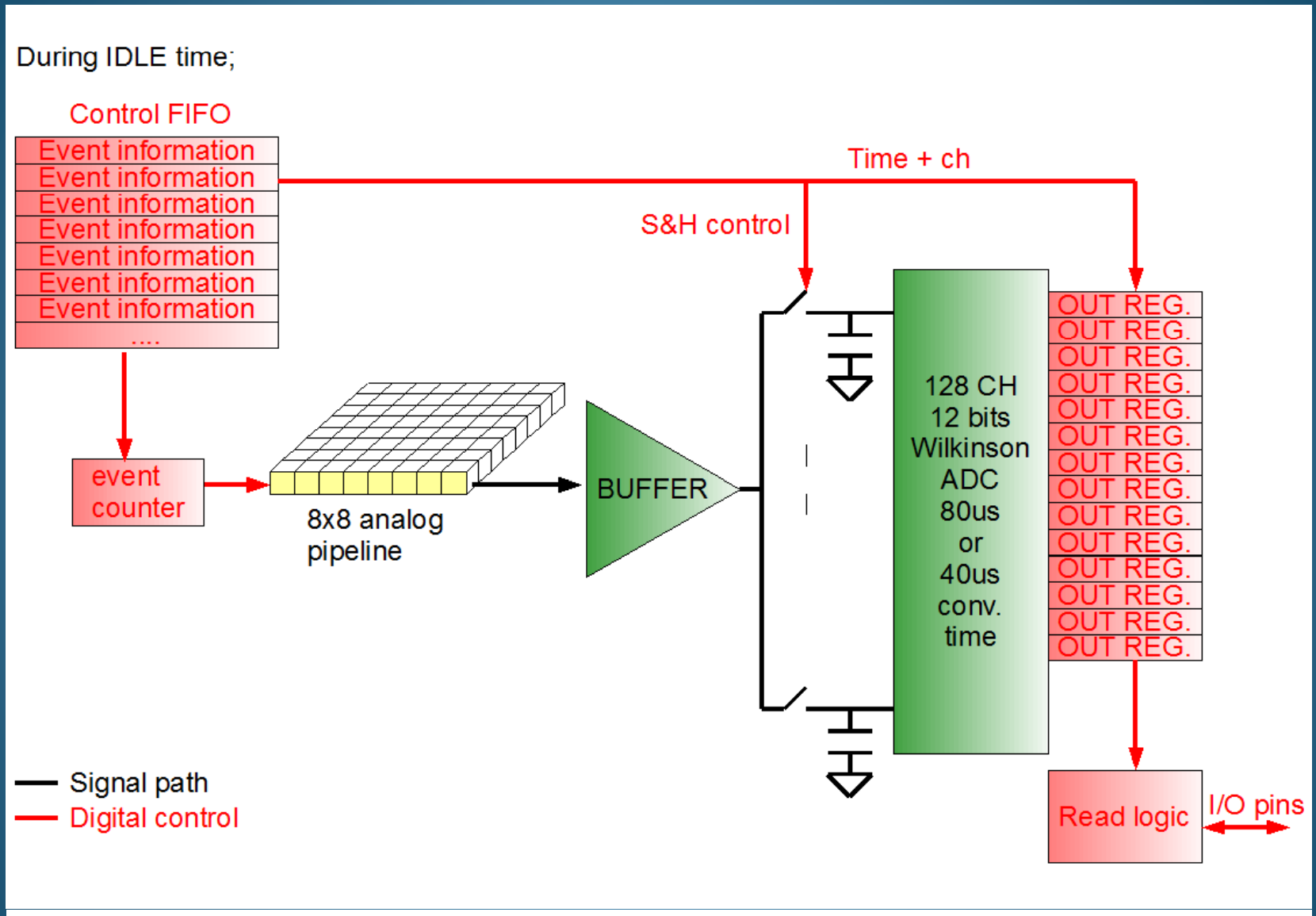
--Digital control: operation fully programmable (all settings of chip operations), fault tolerance, robustness, reliability, flexibility.

Operations during acquisition

- Operations on IDLE time
- Output registers block
- Output registers structure
- Writing data
- Reading data
- Output logic

During acquisition;

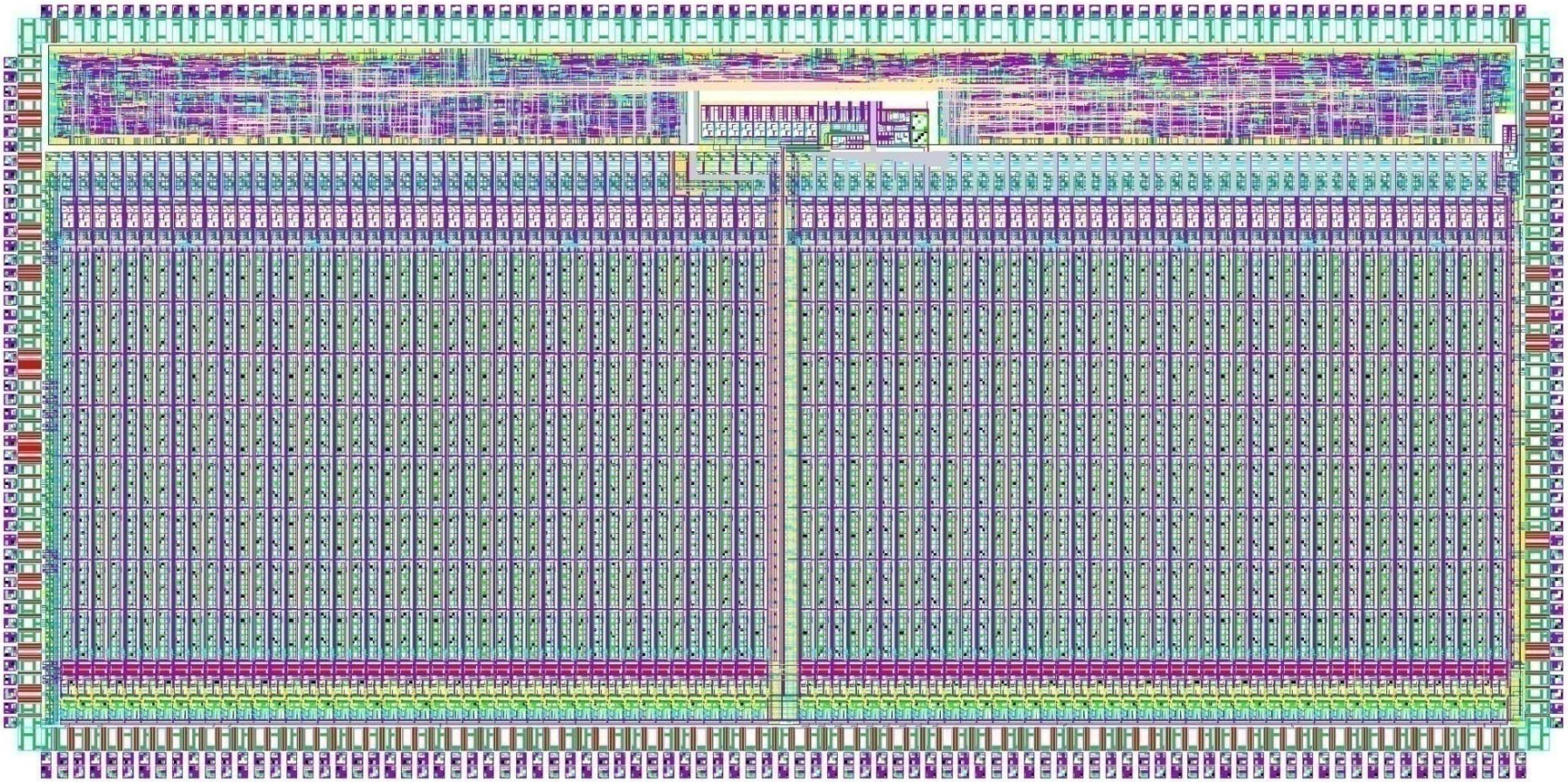



During IDLE time;
Control FIFO
Event information
Event information
Event information
Event information
Event information
Event information
Event information
....
Time + ch
S&H control
event counter
8x8 analog pipeline
BUFFER
128 CH 12 bits Wilkinson ADC 80us or 40us conv. time
OUT REG.
OUT REG.
OUT REG.
OUT REG.
OUT REG.
OUT REG.
OUT REG.
OUT REG.
OUT REG.
OUT REG.
OUT REG.
OUT REG.
OUT REG.
Read logic
I/O pins
Signal path
Digital control

# THE ELEMENTARY and CRUCIAL PIECE in DAQ Silicon Tracking, does it all (almost!!)

University of Barcelona and LPNHE-UPMC/IN2P3-CNRS

91 I/O digital (power supplies, clock, tests,serial I/O)



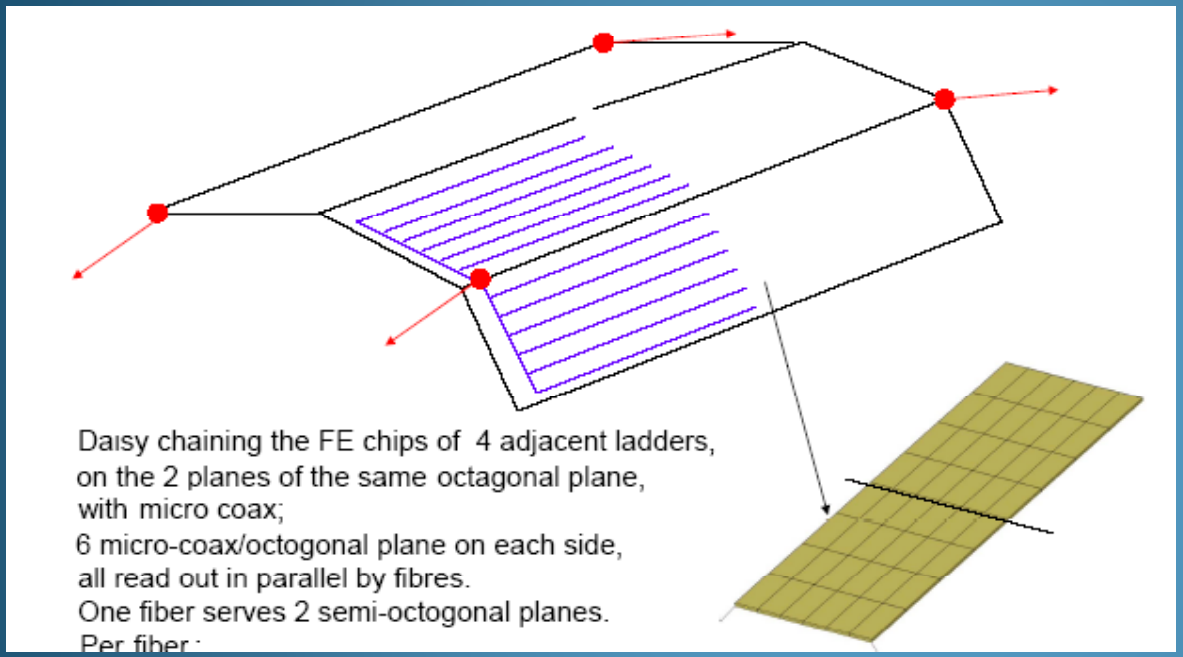
88 strip inputs +2 power suplies + one ground

THE PRESENT CHIP PROTOTYPE SiTR_130-88 includes all the feature (sent to foundry)

- FEE is full custom and DSM CMOS technology (now 130nm soon 90 nm will be tried)
- Crucial and novel solution for direct interconnection chip on detector now bump bonding for strips (as for pixels) very soon for both 3D vertical interconnect
- For the rest of the DAQ: look AMAP for solutions available on the market

# FLOOR 2: FE-on detector edges, interface detector with external world

Example

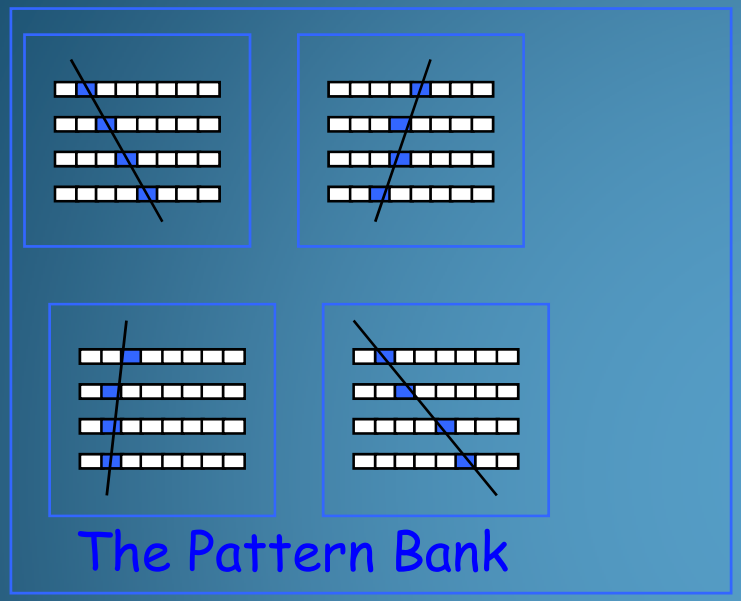


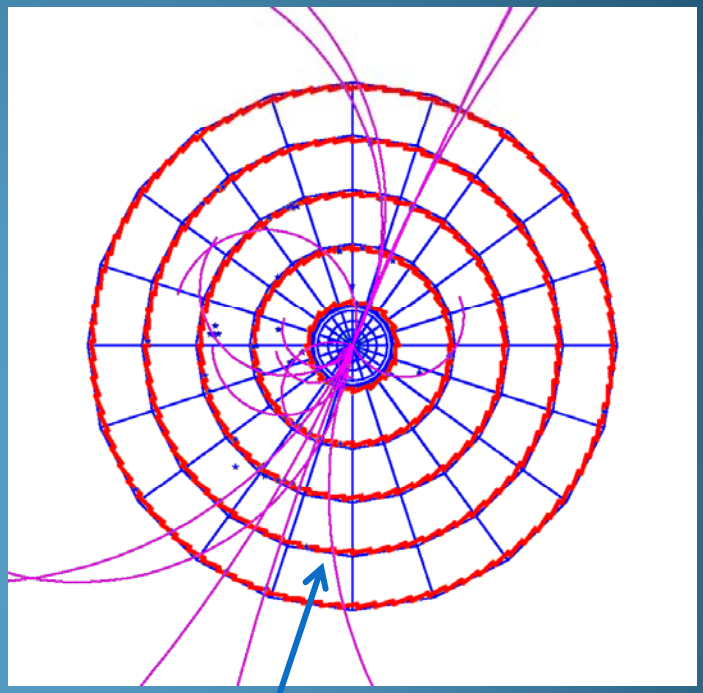

Cabling:
Floor 1 to Floor 2: microcoax
Floor 2 to Floor 3: digital fibers

Number of issues related to cabling:
Follow industrial advances
High rates and high speed, reliability, fault tolerance, robustness
Common for all sub detectors

Each red points = buffer + pre-processing 2 (re-ordering & compressing data), transceiver (digital fiber to external world = Control Room)
Sends predigested data at CR and get slow control and distributes it on detector

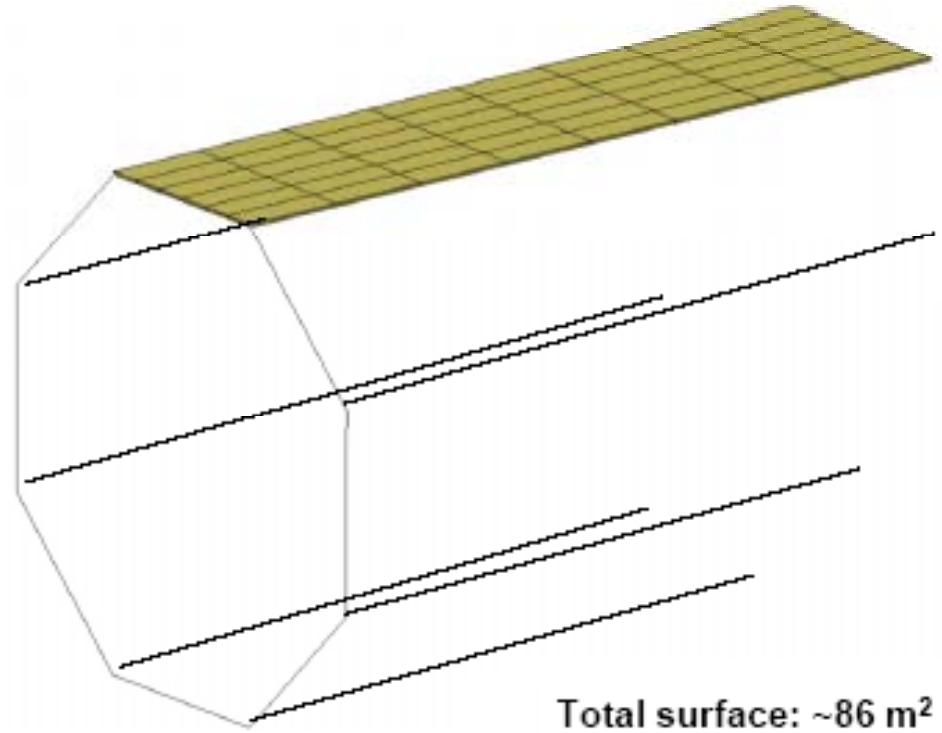
# Floor 3: Si TRK DAQ in the C.R., integration phase



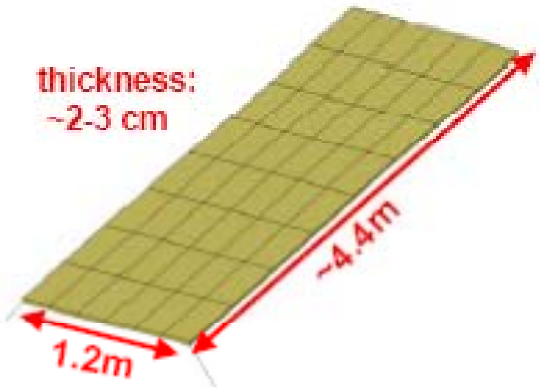



REAL TIME PROCESSING at floor3:
organize the processors for instance regrouping F2 elements belonging to a same azimuthal sector and perform tracking , a la CDF or FTK=FastTrack Finding (LHC).
SLOW CONTROL: synchronisation (Clock), power supplies, calibration signal, operation Parameters settings ....
COMBINE information from SiTracking wih other SUBDTECTORS

# Just an educated guess example



Total surface: ~86 m²
Nb channels: 1,572864
Nb of fibres: 8 per side




| | |
|---|---|
| # ladders/octagone | 96 |
| # sensors/octagone | 288 |
| # channels/octagone | 196608 |
| # µchips/octagone | 192 |
| # µcoax/octagone | 192 |
| # fibres/octagone | 2 |
| # µchips/fibre | 96 |
| # channels /fibre | 98304 |

Outer Silicon tracking layer : false double sided sensors

# Cabling and data flow transmission

Data Flow transmission: presently foreseen to use micro-coax Cables of typically 1'' diameter , 300 mW power dissipation at 1 GHz, can be power cycled. Kapton cables also under Consideration

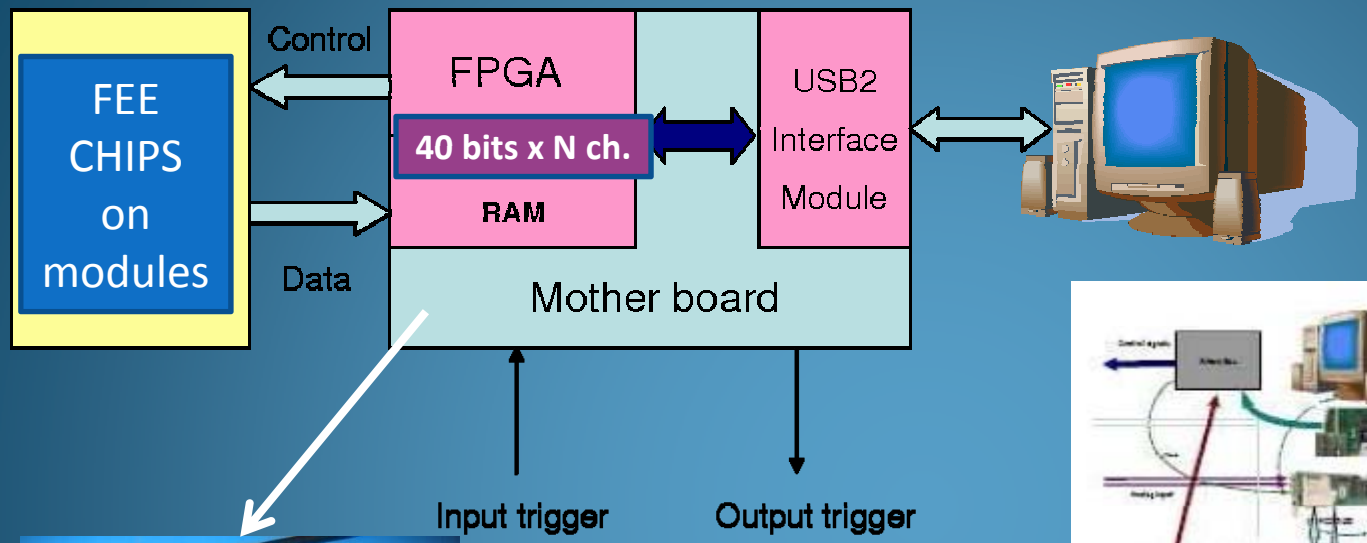
At a later stage: to transmit data from the edge of the detector to the outside, 6 GHz SCM digital optic links are presently considered

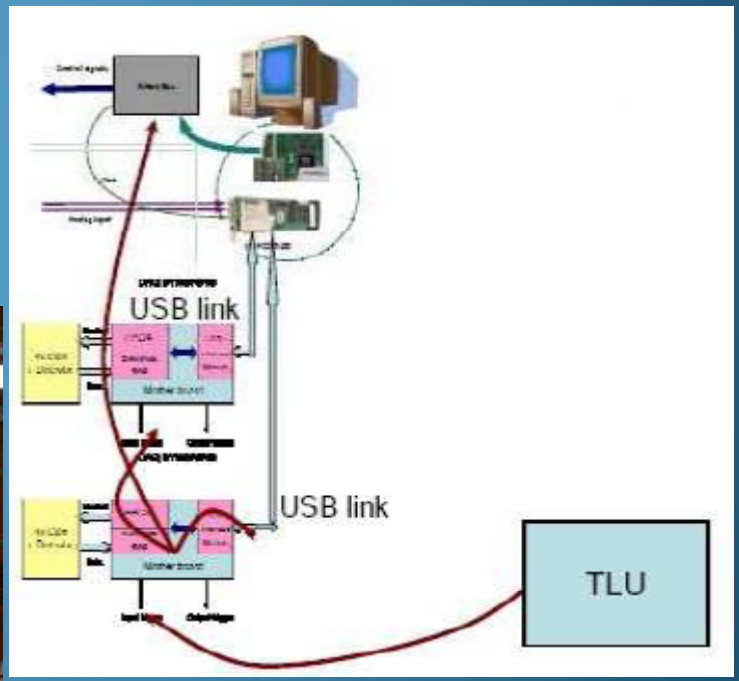
Related to this topic the data processing at all levels as described are a feature of our DAQ architecture.

DSP mounted as multichip modules would represent a very small amount of material (especially at the edge of the detector) and dissipate very little. We are starting to think on a real time track processing scenario

# First DAQ prototypes: test beam DAQ set-ups

(within also EUDET framework)



# Concluding remarks

- The first level of the Silicon DAQ in a ILC and micro strips detector based scenario is well in hand and is a crucial piece in the Si DAQ
- The strategy considered for the DAQ Si tracking upper levels is based on a early stage reconstruction of track segments, then full tracking
- Combining and thus uniformization with other sub detectors & global DAQ becomes a condition sine qua non to progress in the right direction
- Close contact with Industries are essentialin this field too in order to avoid useless and expensive R&D work and makes system becoming soon obsolete.
- Highly performing FEE with full readout capability, fault tolerance, fully programmable, high degree of processing already at early stage in the DAQ chain (with electronics wrt detector architecture)
- Last but not least: Cabling and data transmission / data processing
- Here also test beams are essential tool to develop DAQ