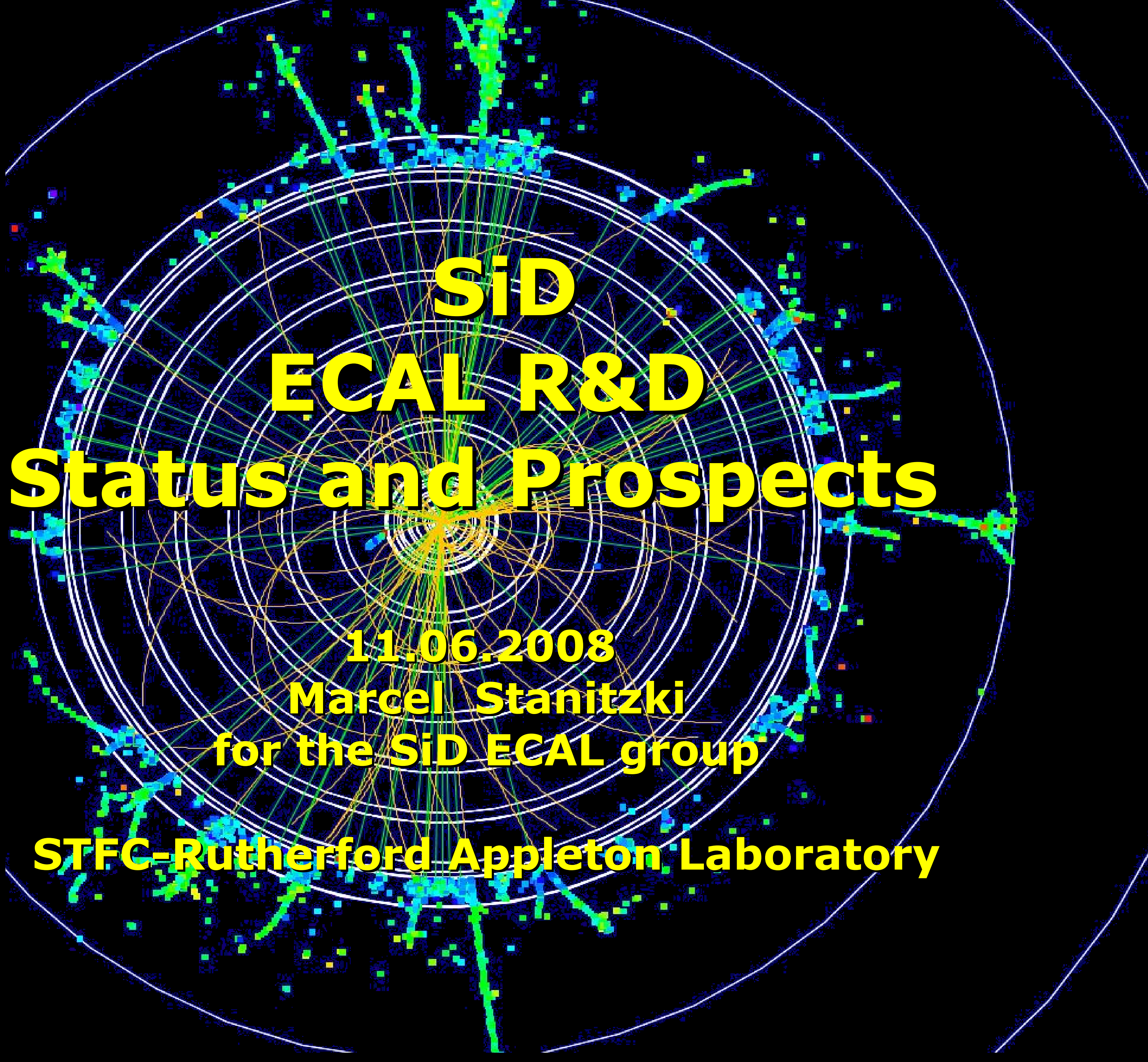

SiD ECAL R&D Status and Prospects

11.06.2008

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for the SiD ECAL group

STFC-Rutherford Appleton Laboratory

Introduction

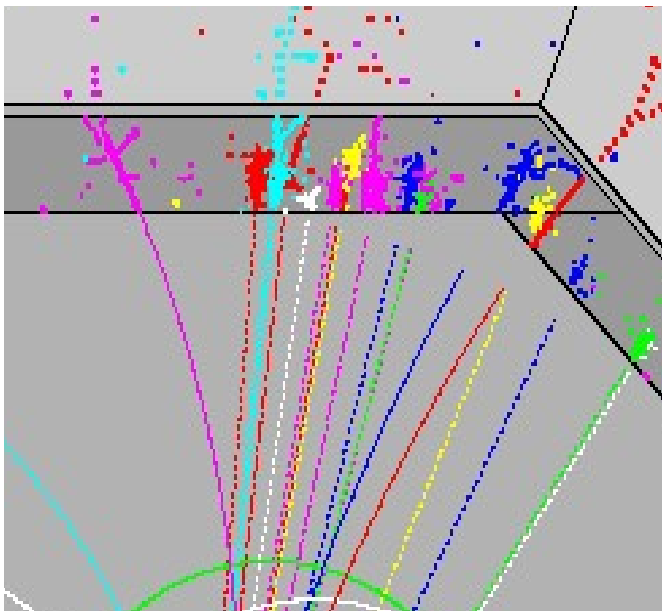
- The SiD Calorimetry System is build around the Particle Flow paradigm
  - High granularity
  - Located inside the solenoid
  - Well integrated with Tracking
- The ECAL is designed as ***Imaging ECAL***
  - Material of choice is Si+W
  - Sampling calorimeter
  - Good energy resolution
  - Compact
  - Segmentation smaller than $r_{Moliere}$

Physics with the ECAL

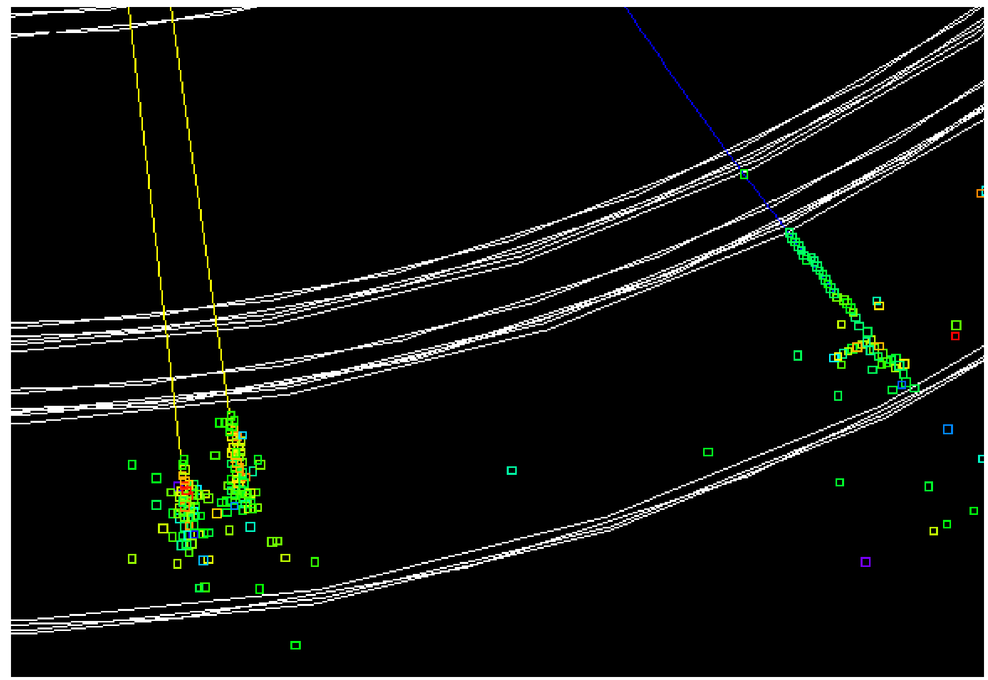
- Multi-jet final states (Higgs, Top ..)
  - π° measurement should not limit jet resolution
  - identify and measure hadronic showers
  - track charged particles
- τ id and analyses
- Photons
  - Energy resolution, e.g. $h \to \gamma\gamma$
  - Vertexing of photons ($\sigma_b \sim 1$ cm), e.g. for SUSY studies
- Electron ID
- Bhabhas and Bhabha acollinearity
- Hermiticity

$\Rightarrow$ Imaging ECAL can do all this

Some Examples



Jet Environment

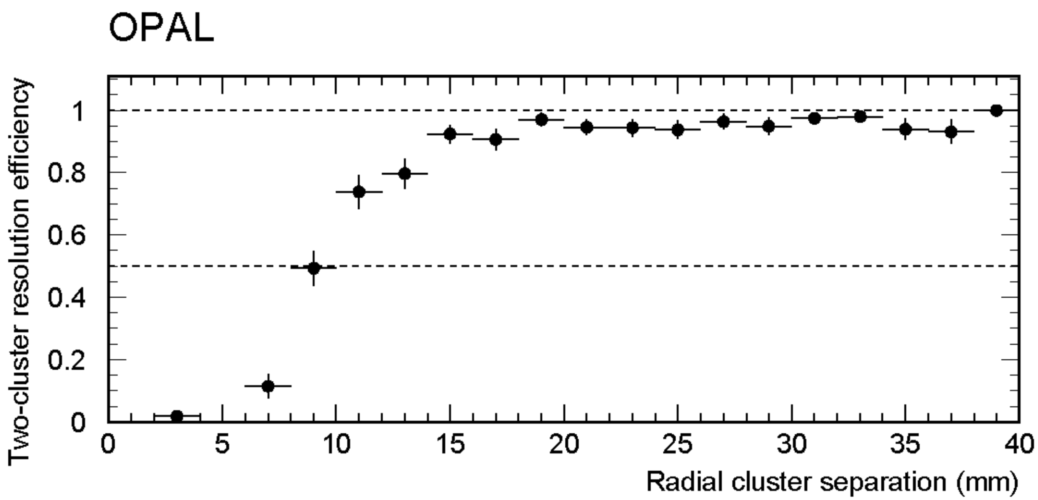


$\tau^+ \rightarrow \rho^+\nu \quad (\pi^+\pi^0\nu)$

Segmentation requirements

- The above benefit from a highly segmented (in 3D) ECAL
- The resolving power depends on and segmentation.
- We want segmentation significantly smaller than $r_{Moliere}$
  - how *much* smaller is an open question

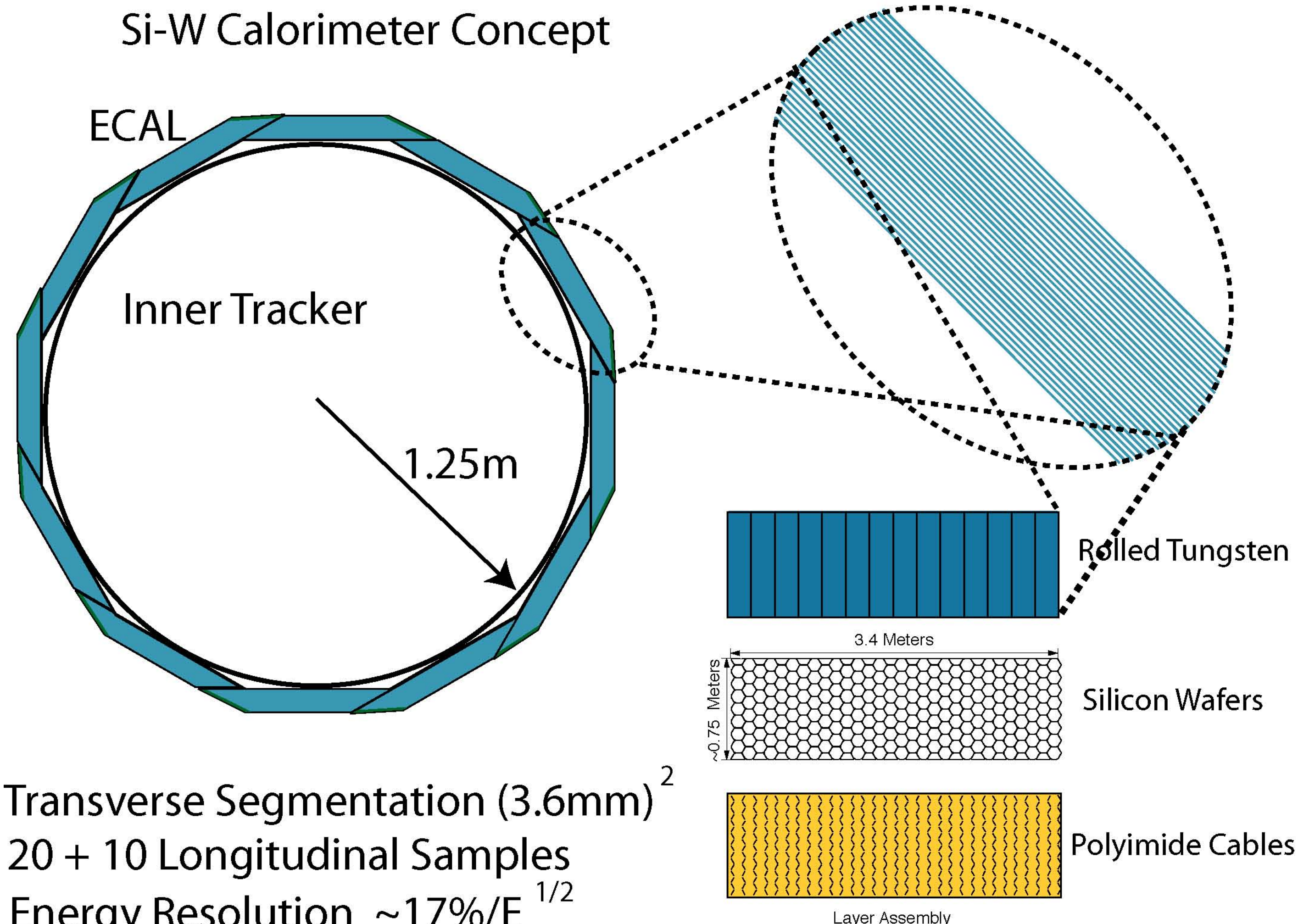
Two EM-shower separability in LEP data with the OPAL Si-W LumCal :



$$f_E \simeq \frac{R_{cal}}{\sqrt{R_M^2 + (4d_{pad})^2}}$$

$$d = 2.5\text{mm} \ , \ R_M \sim 17\text{mm}$$

Mechanical layout



Transverse Segmentation $(3.6\text{mm})^2$
20 + 10 Longitudinal Samples
Energy Resolution $\sim 17\%/E^{1/2}$

__Baseline configuration:__

- longitudinal: $(20 \times 5/7\ X_0) + (10 \times 10/7\ X_0) \Rightarrow 17\%/\mathrm{sqrt}(E)$
- 1 mm readout gaps $\Rightarrow$ 13 mm effective $r_{Moliere}$

Two ECAL options

Si+W

Common Mechanical Design

Traditional Silicon Diodes

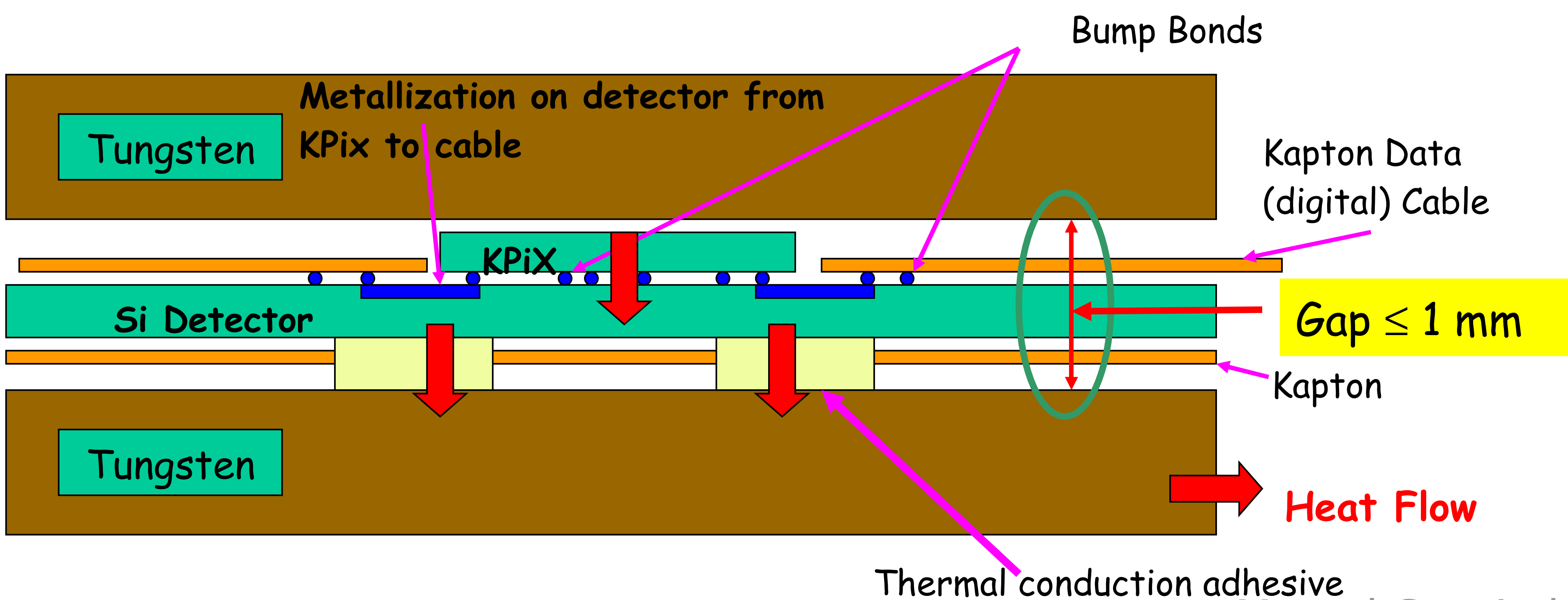
- HEP-style silicon
- 13 mm^2 hexagons
- Analog readout
- KPiX readout chip
- SiD *baseline*

TeraPixel Option

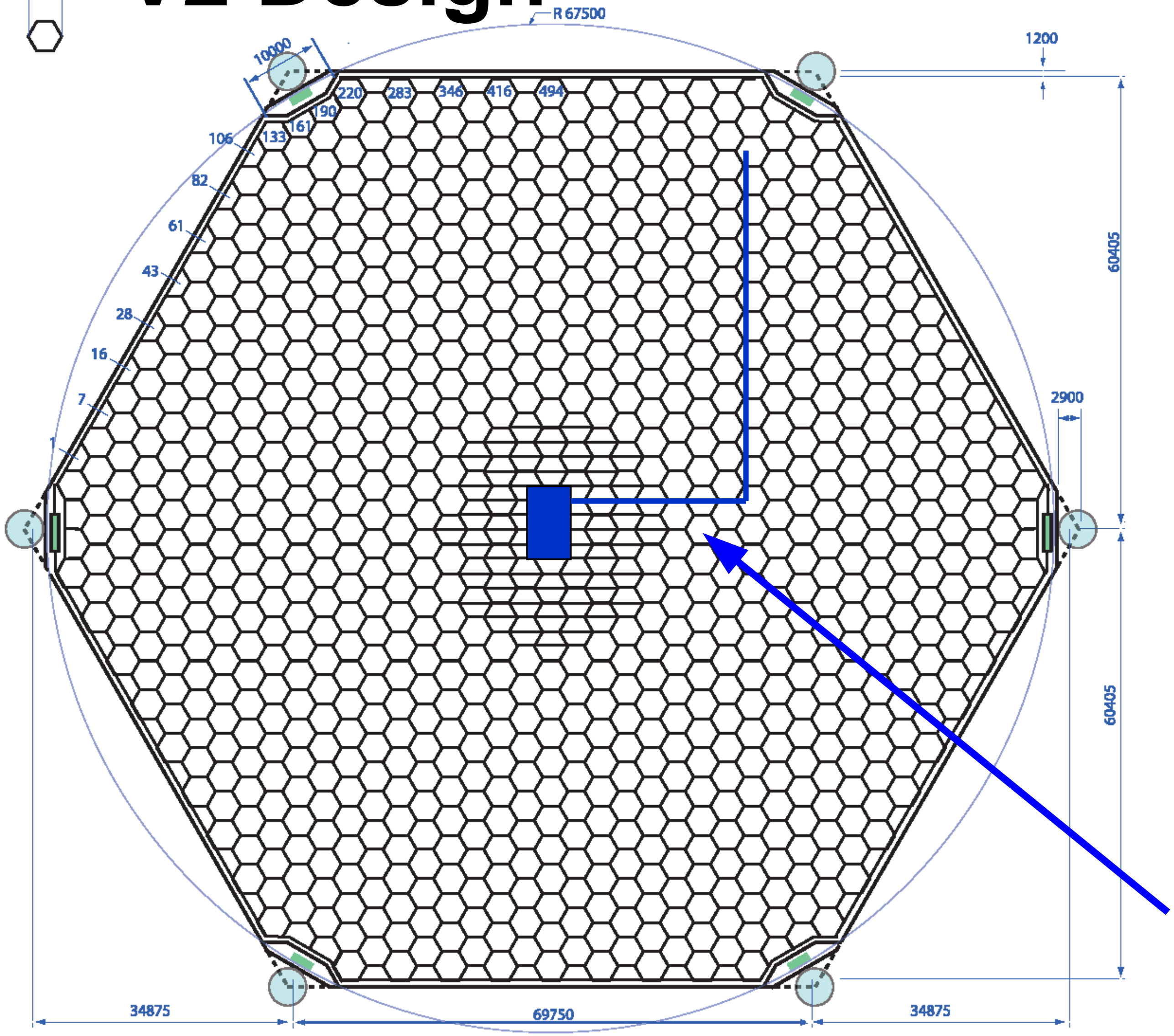
- CMOS MAPS
- 50 x 50 µm pixel size
- Digital readout
- readout integrated in pixel
- *Alternate* option

SiD Requirements

- Fit in common mechanical structure
- Power pulsing (1 % duty cycle)
  - passive cooling
  - Requires < 40 mW/channel
- Single Bunch Time stamping



V2 Design



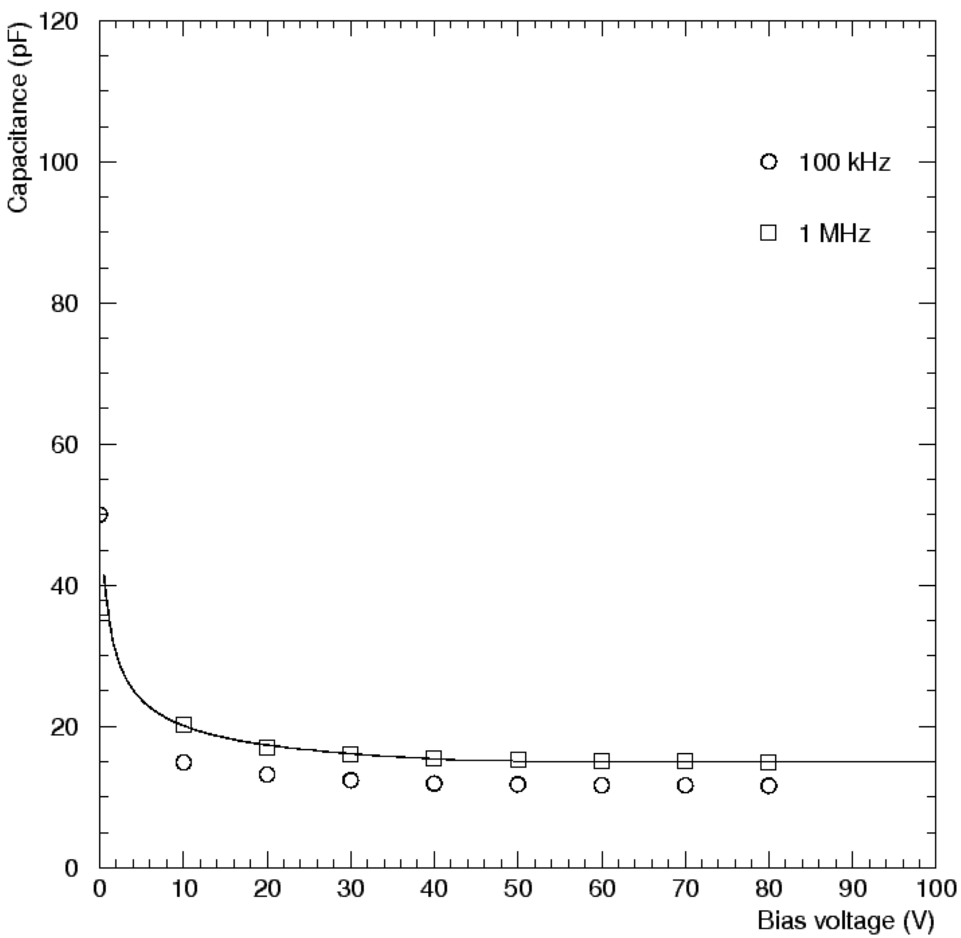
- 6 inch wafers
- 1024 13 mm² pixels
- improved trace layout near KPiX to reduce capacitance
- 30 Wafers from Hamamatsu delivered

KPiX ASIC and sample trace

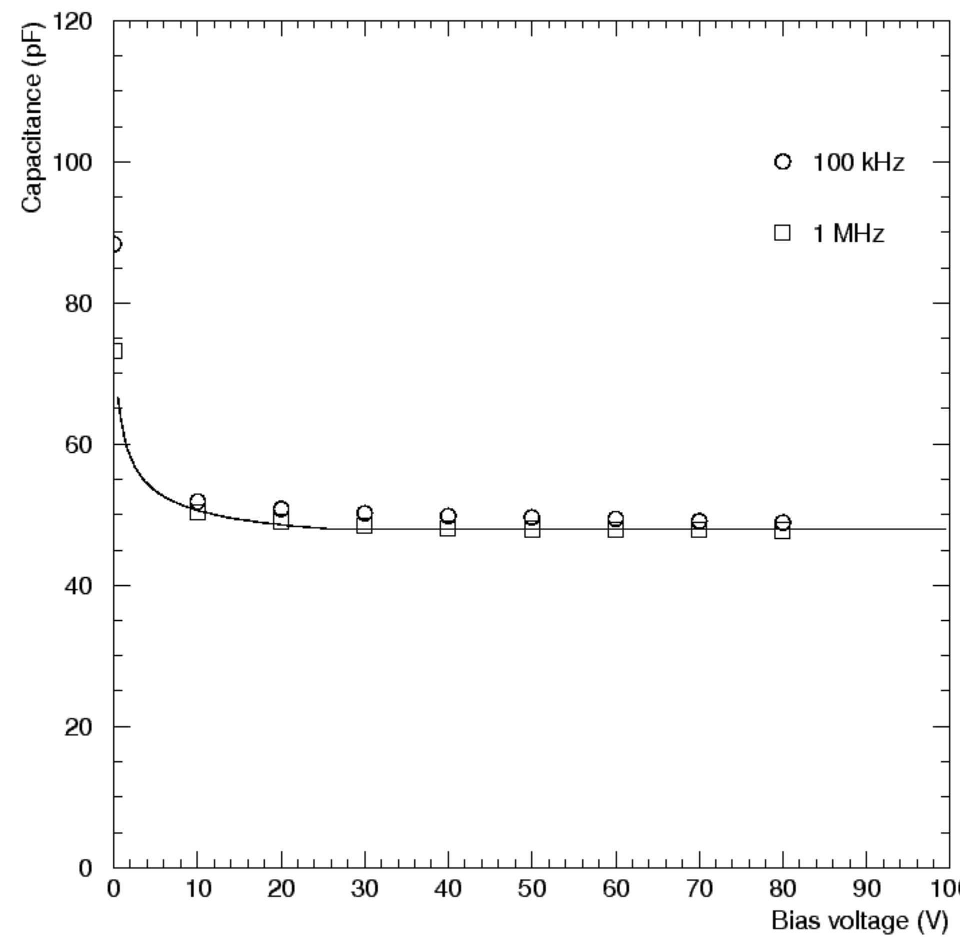
Improvements in v2

- Thinner traces
  - 2 times less stray capacitance
  - 2 times larger resistance
- Split pixels at center
  - 2 times less stray capacitance
- Series resistance for longest traces is 1 k
- Upper limit on irreducible noise
  - $C_{tot}\sqrt{4kTRB}/e$ 500 electrons – longest trace
  - 400 electrons – congested area
  - Assumes 0.5μs shaping time, bandwidth B = 106 Hz

CV curves



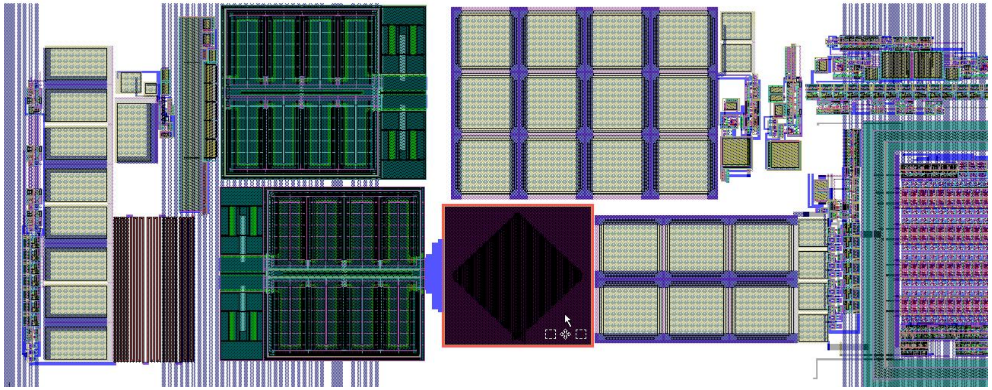
CV-curve for longest trace
Capacitance < 20 pF

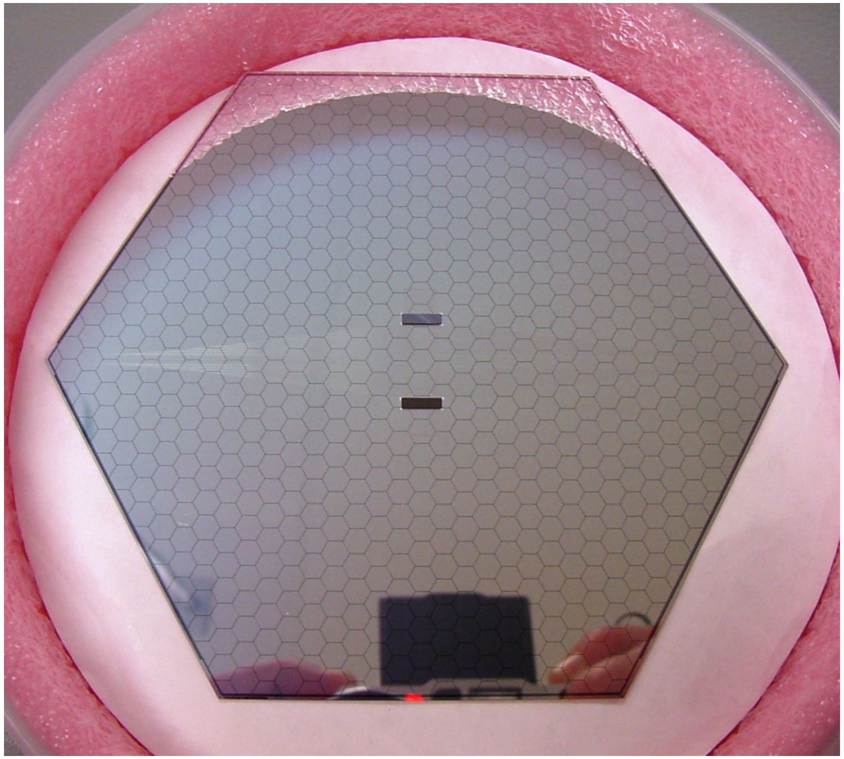


CV curve for congested area
(near KPIX) Capacitance 50 pF

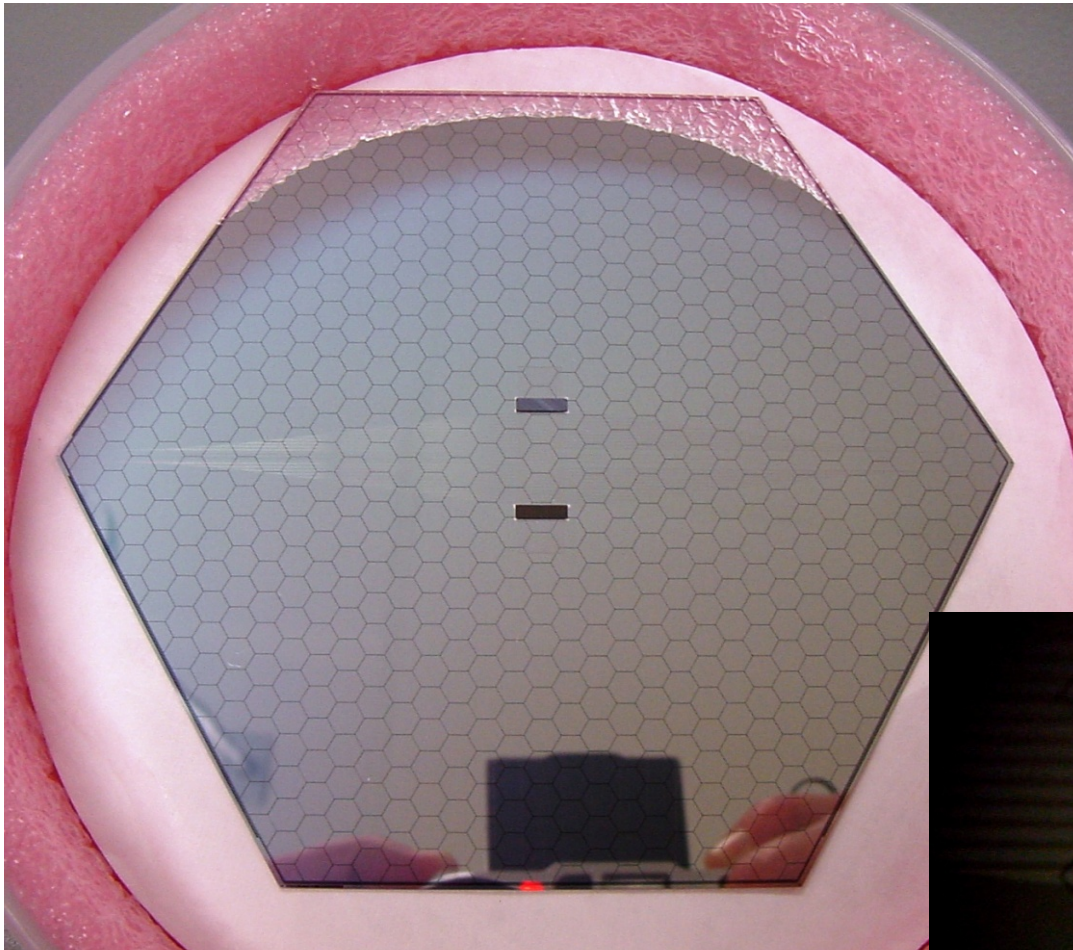
KPix readout chip

- 1024 channels
  - prototypes have 64 channels
- bump-bondable
- 13 bit ADC and Dynamic Gain selection
- 0.25 micron CMOS
- ~ 20 mW/channel
- KPiX is also foreseen to be used in
  - Tracker
  - HCAL
  - Muon chambers



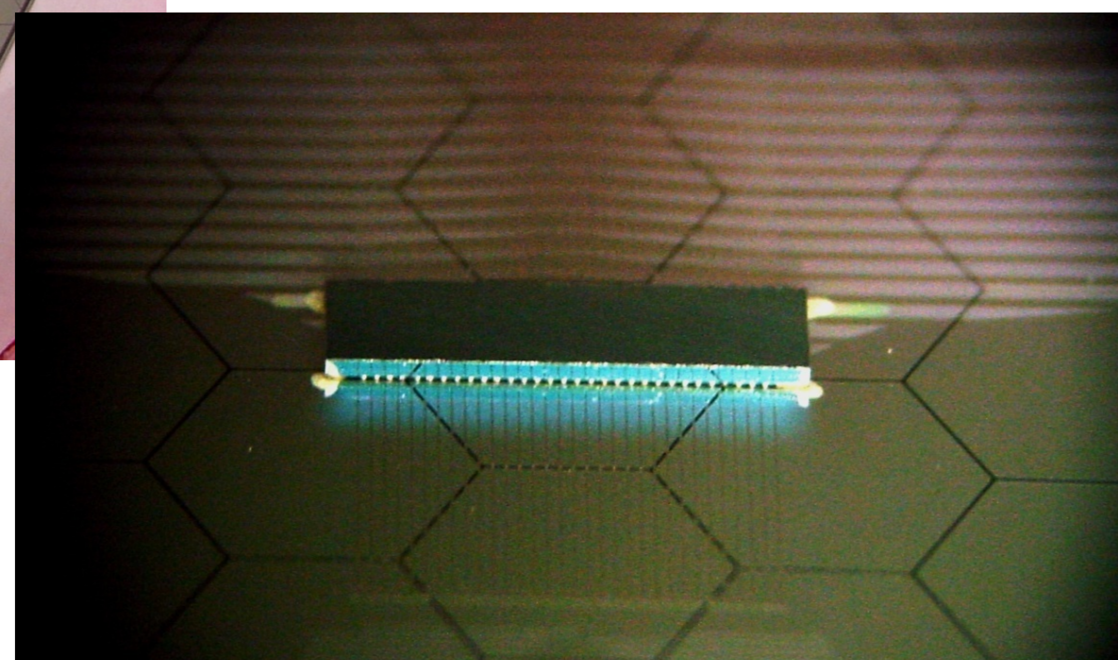


KPiX-v6 gold-stud bonded to v1 sensors

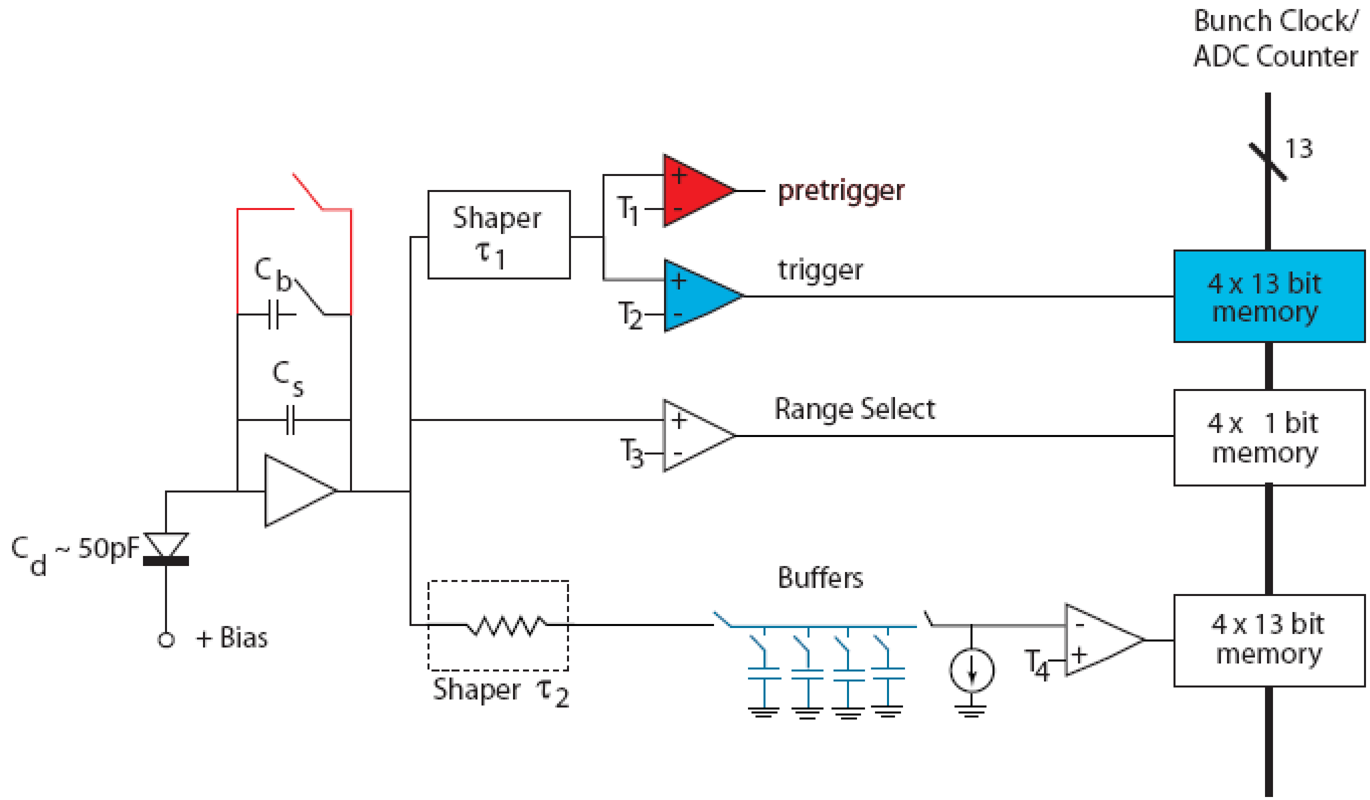


Initial test results (1/25/08, UO) of first attempt (Palomar Tech.):

one open / 24 connections tested



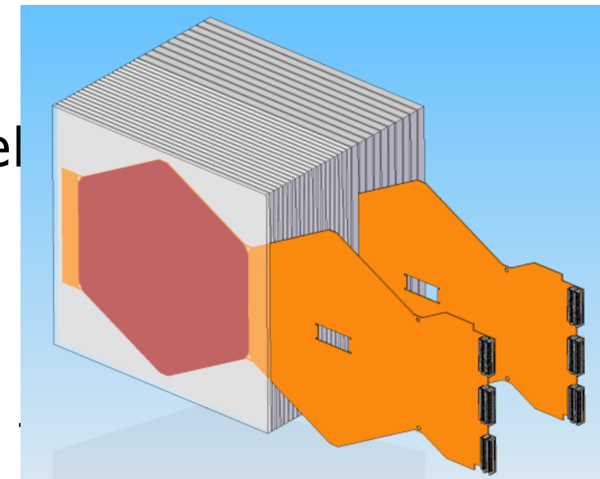
KPiX in Detail



- Threshold T_1 is used to inhibit resets (set at 2 $\times$ noise)
- Threshold T_2 is used to enable data storage (set at 4 $\times$ noise)
- Bunch clock (time) is stored in SRAM (13 bit precision)
- Analog charge is stored on capacitors (13 bit precision)

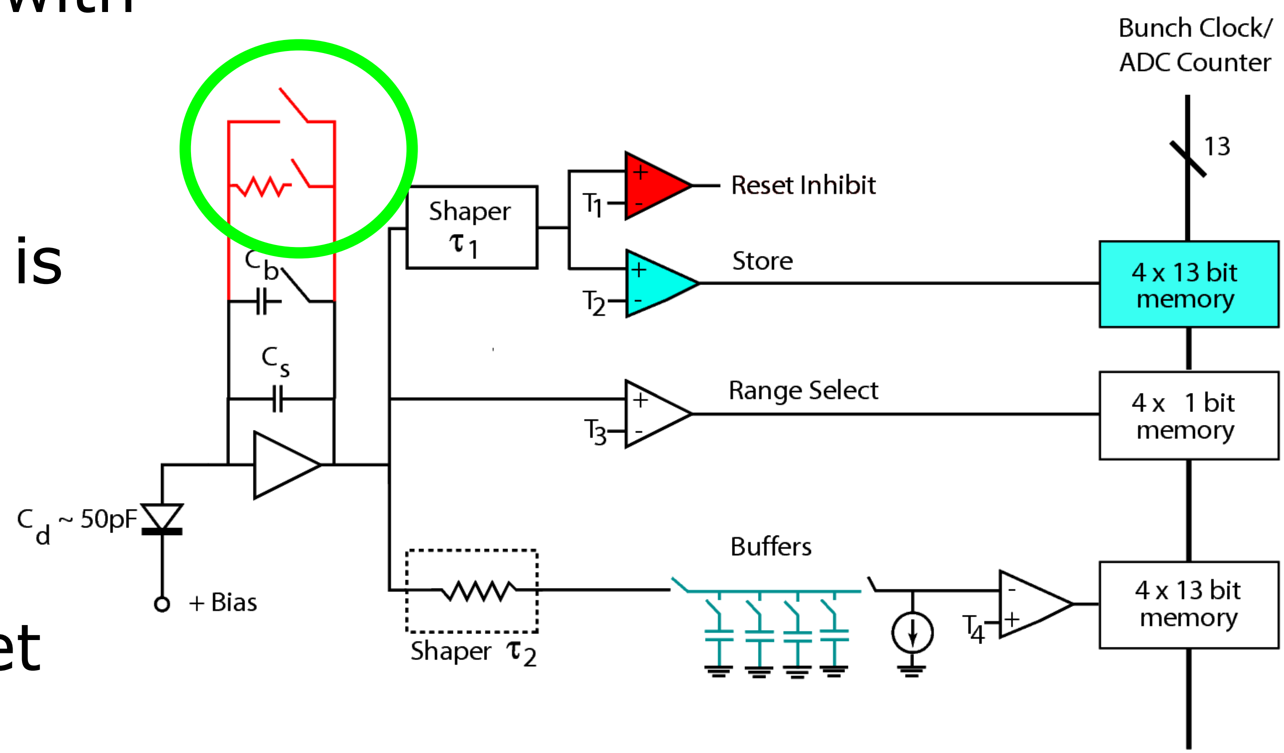
Current Status

- Working on first 1024 channel version
  - 64 channel prototypes are tested extensivel
  - 7th generation prototype available
  - Improved Noise performance
  - One intermediate 256/512 channel version
- Demonstrate Bump-bonding of KPiX
- Build Test beam module (30 layers)
  - Design of stack has started
  - Wafers have been delivered

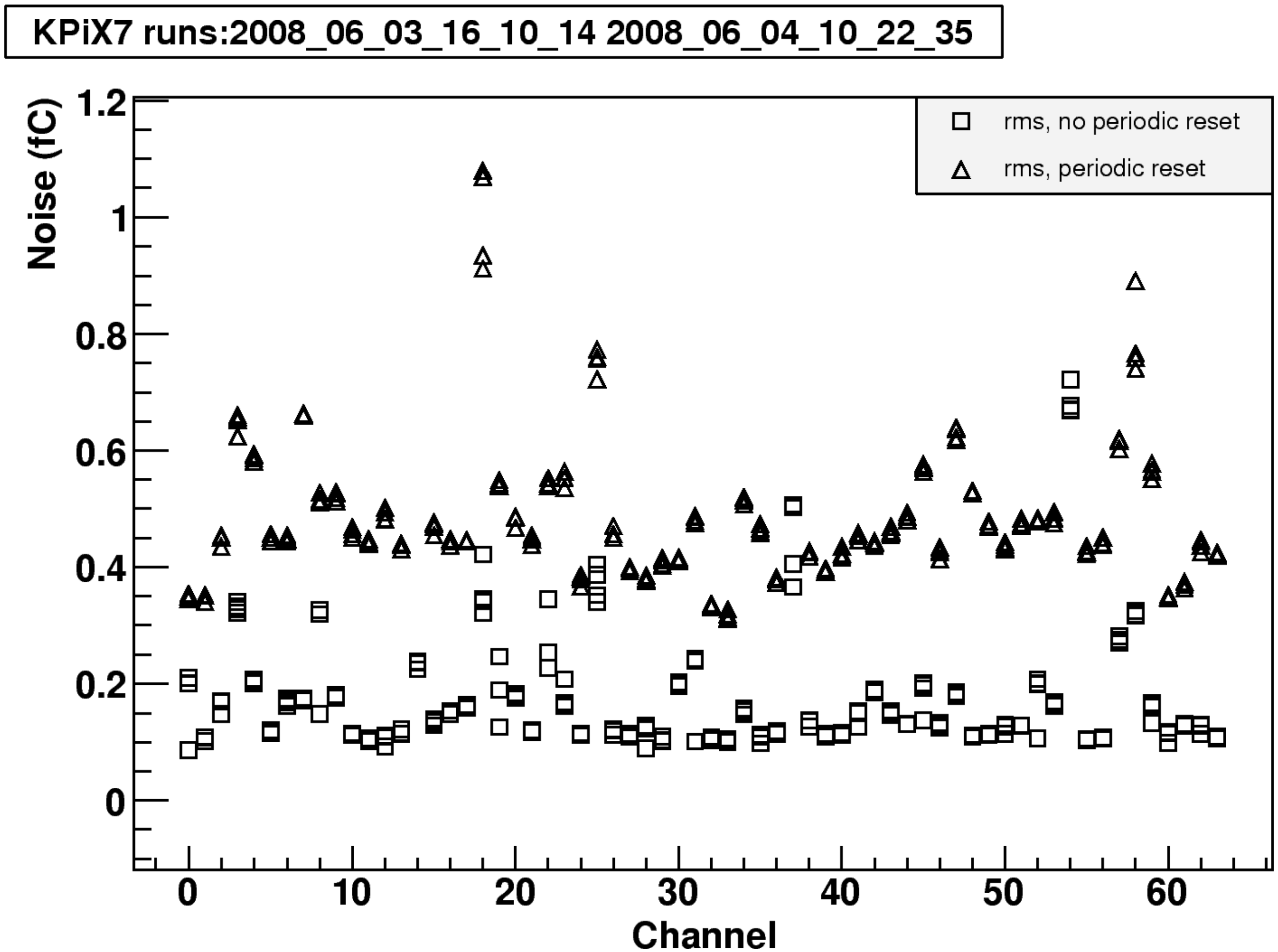


KPiX V7 new reset mode

- The switch in series with the reset is normally closed and it
- Opens when a signal is sensed.
- Supports range switching
- The old periodic reset can also be selected

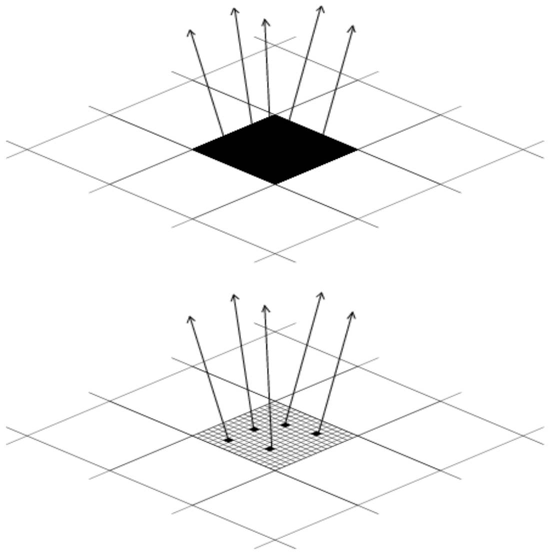


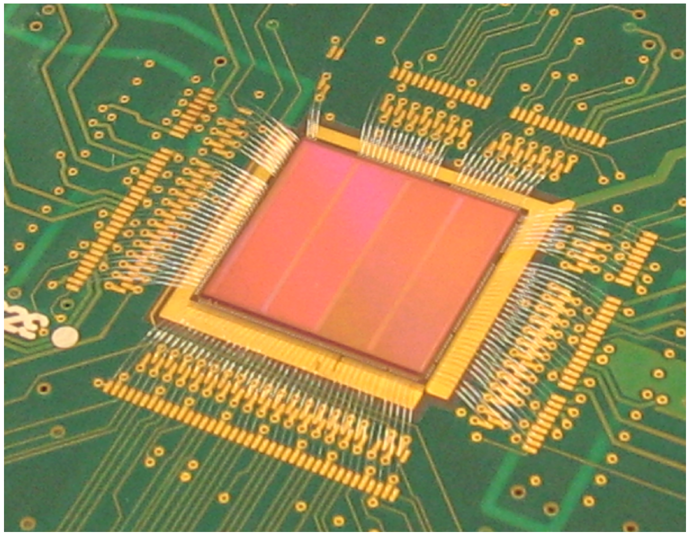
KPiX V7 first results



TeraPixel Option

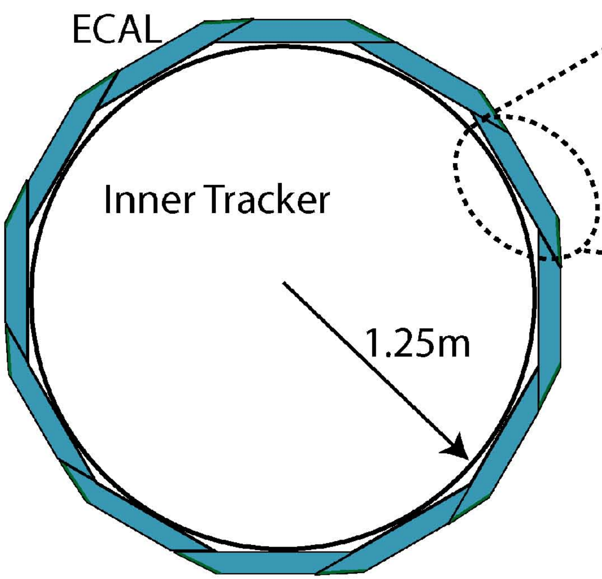
- Digital ECAL
  - Operates as a shower particle counter
- Based on MAPS technology
  - Using Deep p-well INMAPS process
  - 50 x50 micron pixels
- First generation sensor TPAC1 has been manufactured
  - 168x168 pixels, 8.2 million transistors
  - First test results encouraging
- TPAC1.1 to be submitted in July
- See Talk by John Wilson

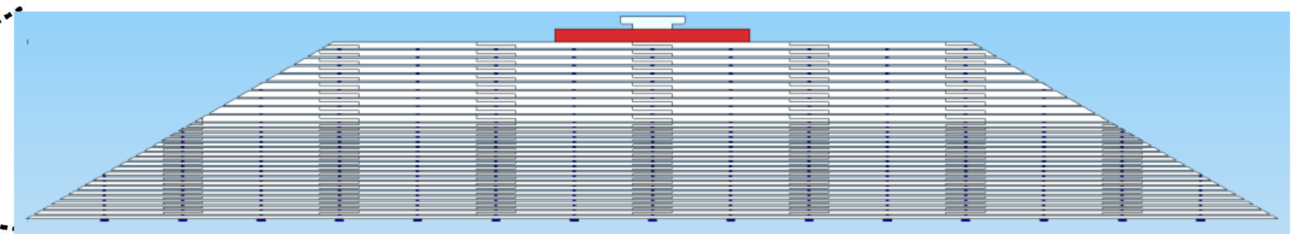




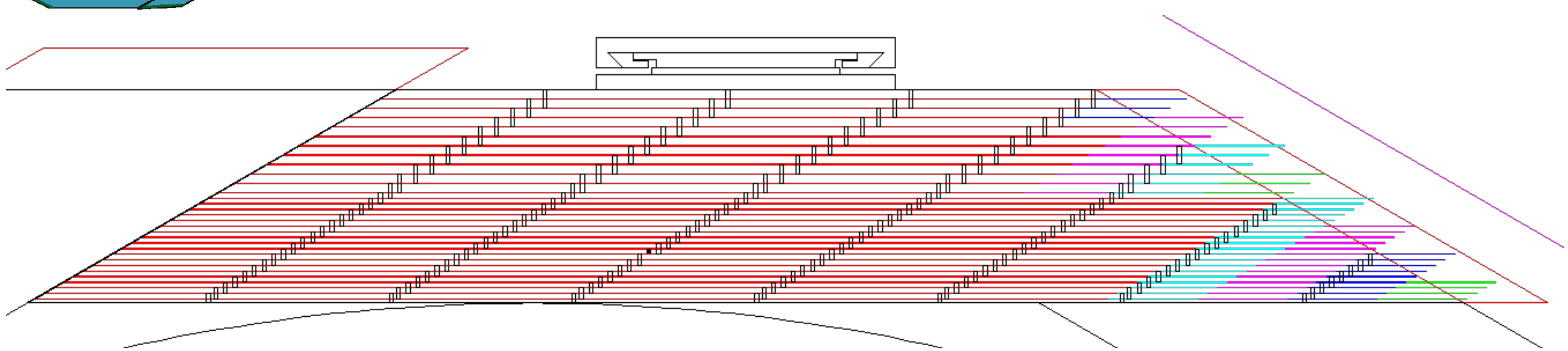
First mechanical design

Si-W Calorimeter Concept



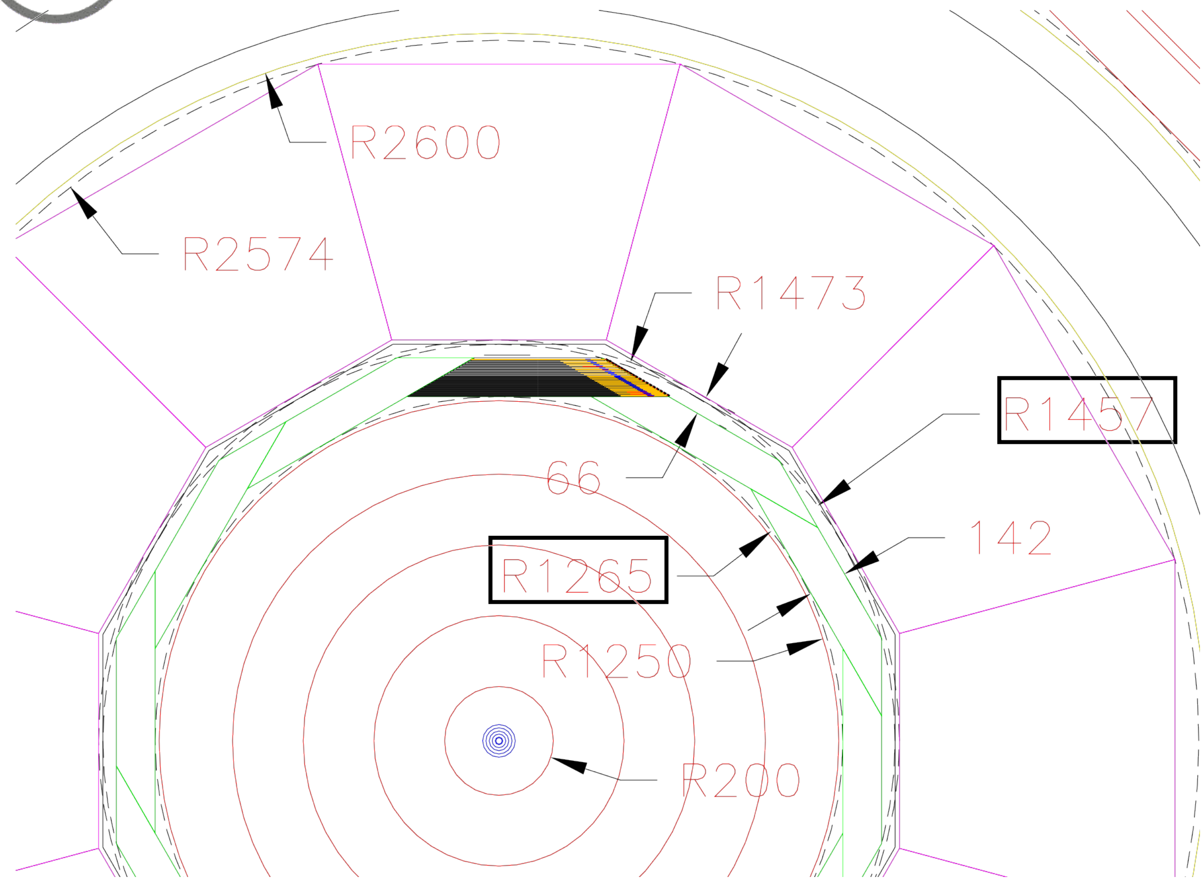


Marco Oriunno, SLAC



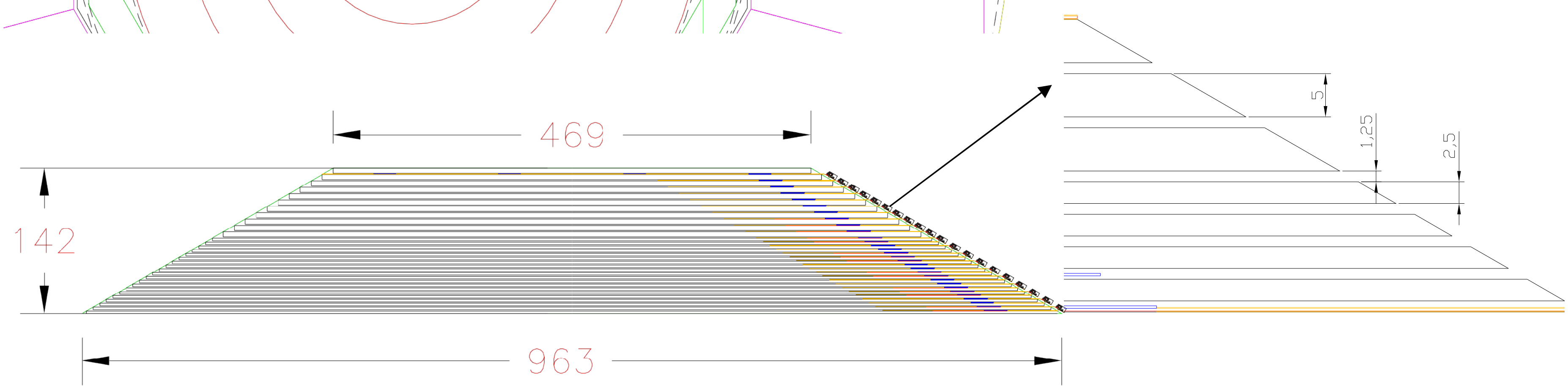
Only 2 Si sensor mask-sets required

ECAL Parameters

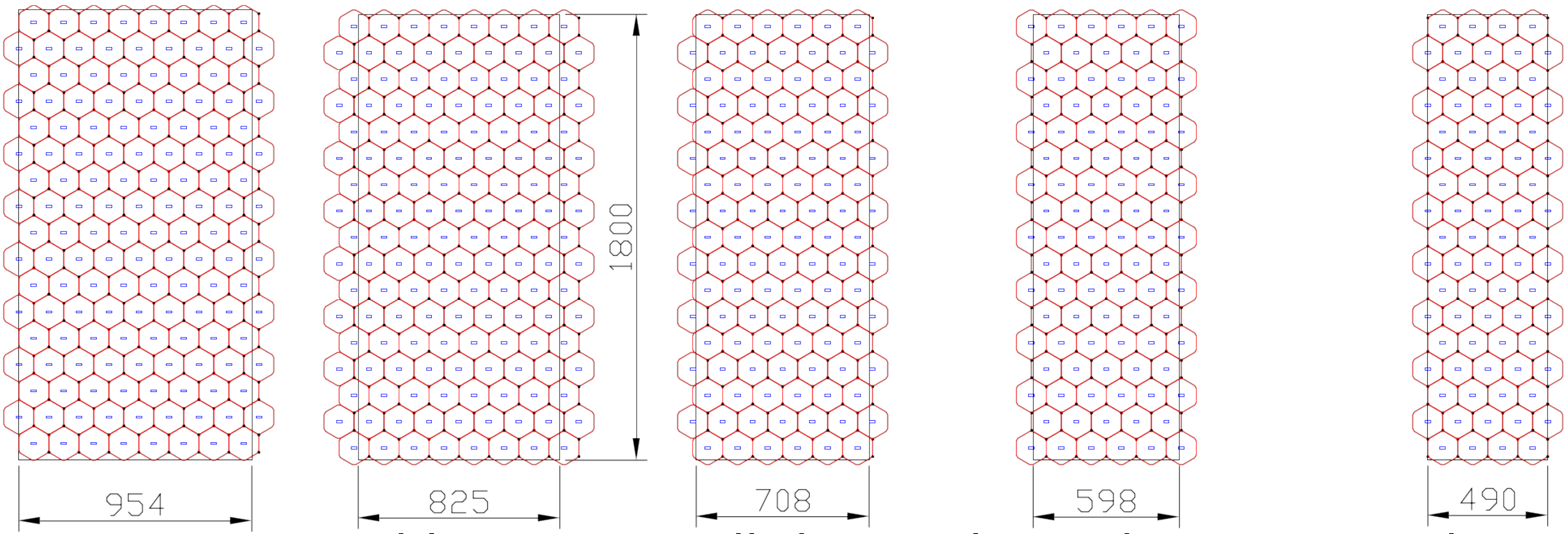


Requirement

- Radial envelope: 1265 mm to 1473 mm
- 12 wedges over 2п
- 20 tungsten layers of 2.5 mm
- 10 tungsten layers of 5 mm
- Instrumented gap 1.25 mm. i.e. shortest Moliere radius
- Z length: 3600 mm
- Wedge mass 4900 Kg

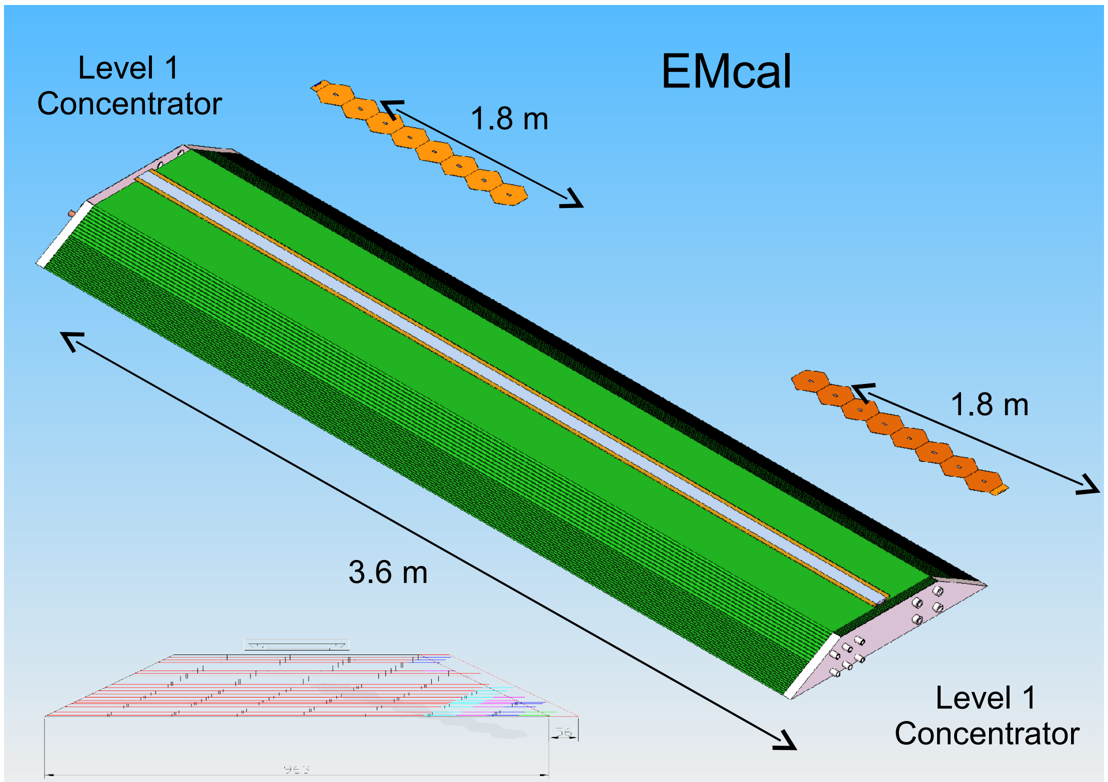


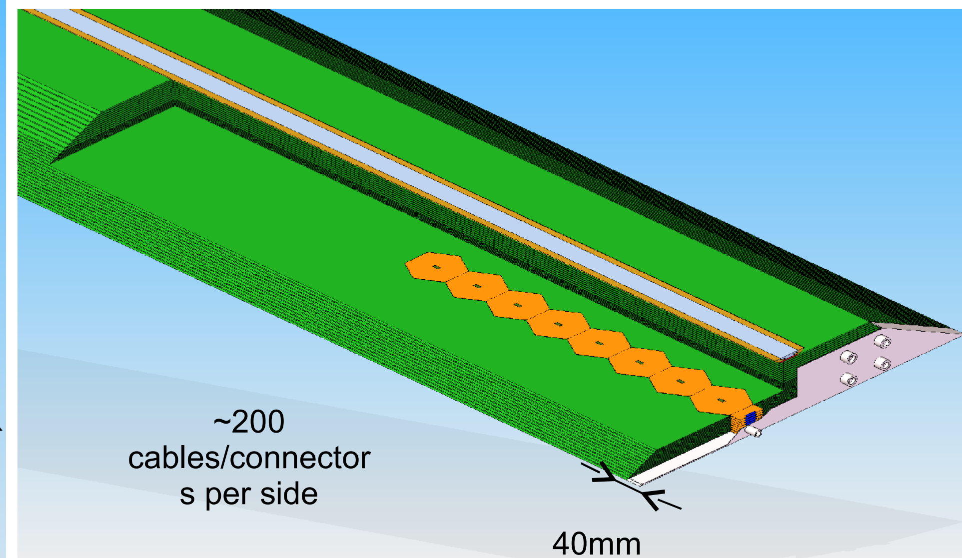
Sensor Integration



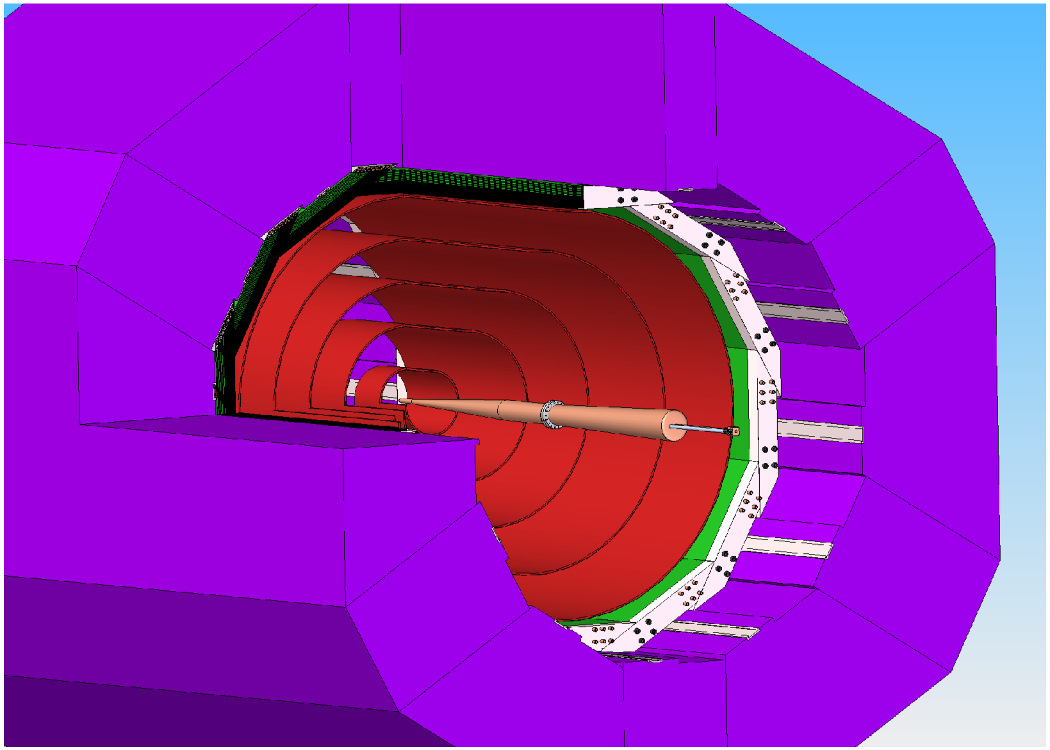
- It is not possible to cover all the W plates dimension with the same silicon sensor size.
- Increased number of masks for the edges
- Hexagon geometry is an ideal tiling pattern, but doesn't make life easier : pins, overlap, cables

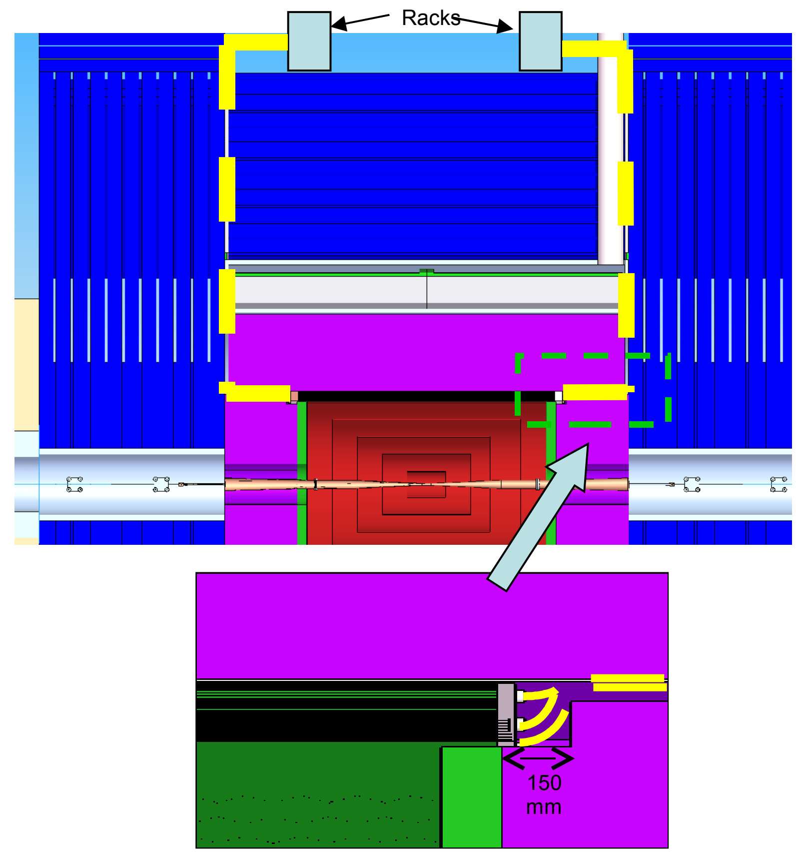
ECAL Wedges


Level 1
Concentrator
EMcal
1.8 m
1.8 m
3.6 m
Level 1
Concentrator


~200
cables/connector
s per side
40mm

Integration into SiD





Summary

- From Ray Frey:
  - *The recent political choices in the U.S. and U.K. have thrown a monkey wrench in the works.*
- But still making good steady progress ...
- Still going strong for the LoI
- Always open for interested people
- Thanks to Ray Frey, John Jaros, Marco Oriunno, David Strom, Mani Tripathi for comments & material