Silicon microstrip sensor R&D for the ILC Experiments

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for the SiLC R&D collaboration

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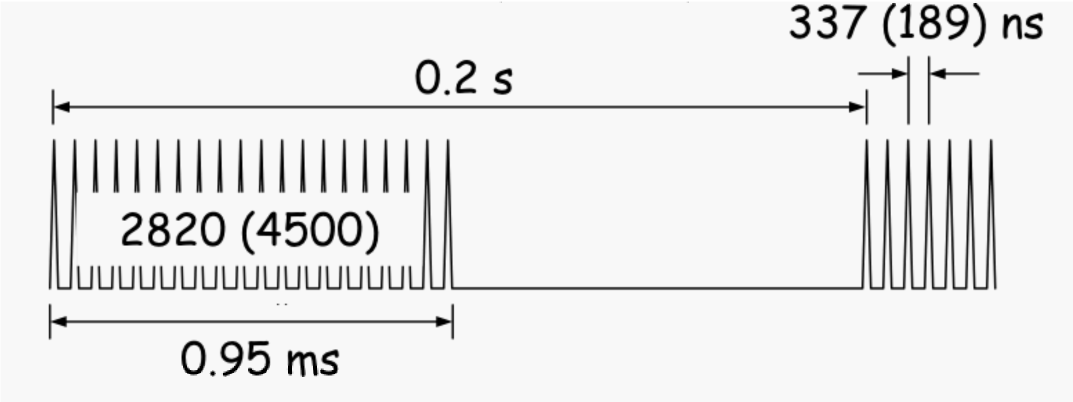
Linear Collider Constraints

- Future Linear Collider Experiment will have a large number of silicon sensors, even when using TPC-based main tracker
- Radiation damage in Silicon almost non-existent in contrast to LHC
- Concept for strip tracker:
  - long strips (10-60cm)
  - low material budget: avoid too many cables, cooling, support
    Therefore:
  - No active cooling only due to power cycling of FE electronics (1/100ms duty cycle)
  - Time structure of beam:



SiIC Silicon Sensor Baseline

- **SiIC sensor baseline**
  - FZ p-on-n sensors: n-bulk material, p+ implants for strips
  - high resistivity (5-10 kOhm cm)
  - Readout strip pitch of 50µm
    - Possibly intermediate strips in between (resulting 25µm pitch)
    - Smaller pitch becomes very complicated (Pitch adapter, bonding, charge sharing,…)
  - Thickness around 100-300µm
    - mostly limited by readout chip capabilities (S/N ratio)
  - **Low current:** <1nA per strip

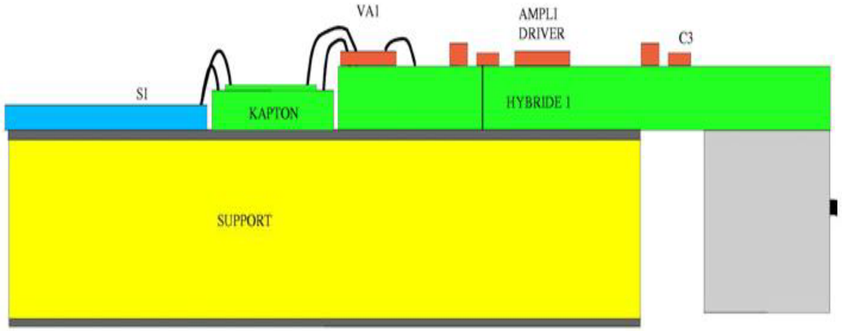
  (Due to long integration time noise mostly defined by current and resistors)

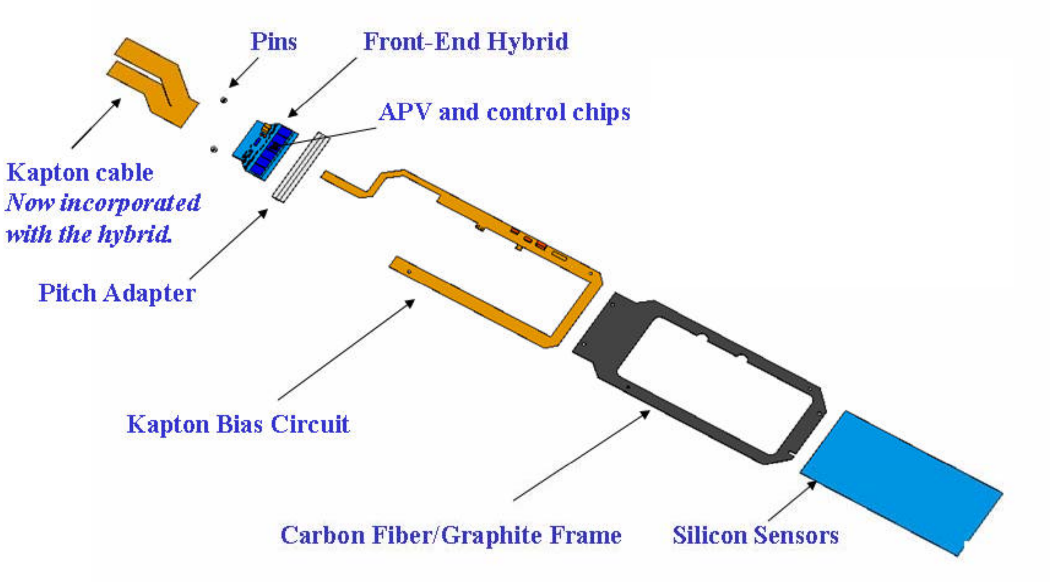
- **Baseline for inner layers:**
  - 6” inch, Double sided, AC coupled

- **Baseline for outer layers:**
  - 8” (12”?) inch, Single sided, Preferably DC coupled (cheaper)

Minimize material budget

- Multiple scattering is crucial point for high-precision LC experiment
- Minimize multiple scattering by reducing material budget of detector modules itself
- Old-fashioned module design:
  - Silicon sensor
  - pitch adapter
  - FE hybrid
  - readout chip
- **Long-term goal: Integrate pitch adapter into sensor**
  - Connectivity of strips to readout chip made by an additional oxide layer plus metal layer for signal routing
  - Readout chip bump-bonded to sensor like for pixels





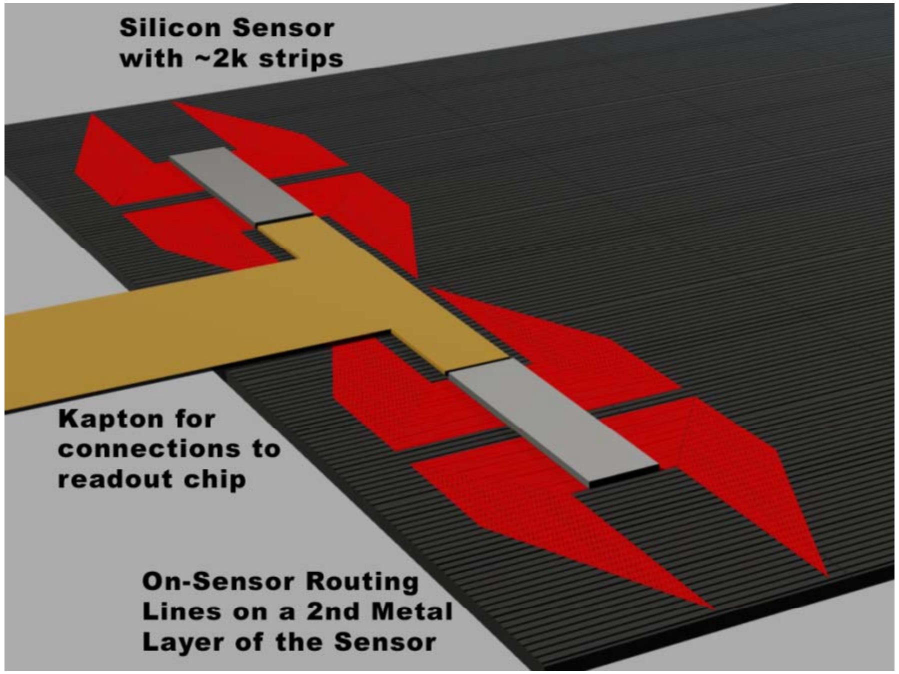
In-sensor routing and bump-bonded chip

Concept Design

- Connection between readout chips and sensor in additional metal layer on the sensor *(red lines)*
  → **No pitch adapter necessary**

- Readout chips bump bonded on the sensor *(grey chips)*
  → **No hybrid necessary**

- Supply lines and data link to readout chips via kapton *(brown T-piece)*

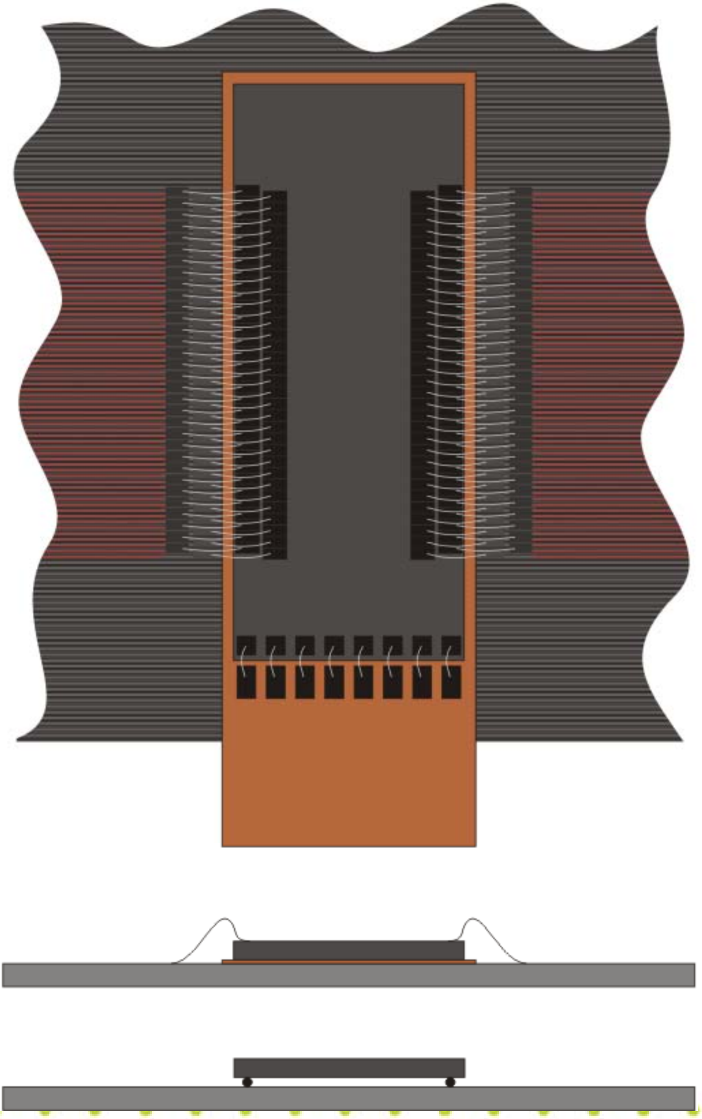


Additional Benefits:

- Assembly process less complicated
  → fewer parts
- Modules are more robust
  → no delicate microbonds

Bump-/Stud- bonding

- Readout chip needs to be connected upside down onto sensor (flip-chip bonding)
- Two methods:
  - Indium Bump-bonding needs treatment of both chip and sensor with indium
    - Advantage: fine pitch
  - Stud-bonding doesn’t need special treatment
    - Minimum pitch: ~80um
- 1st step: Design to allow both, wire and stud-bonding with same chips and sensors

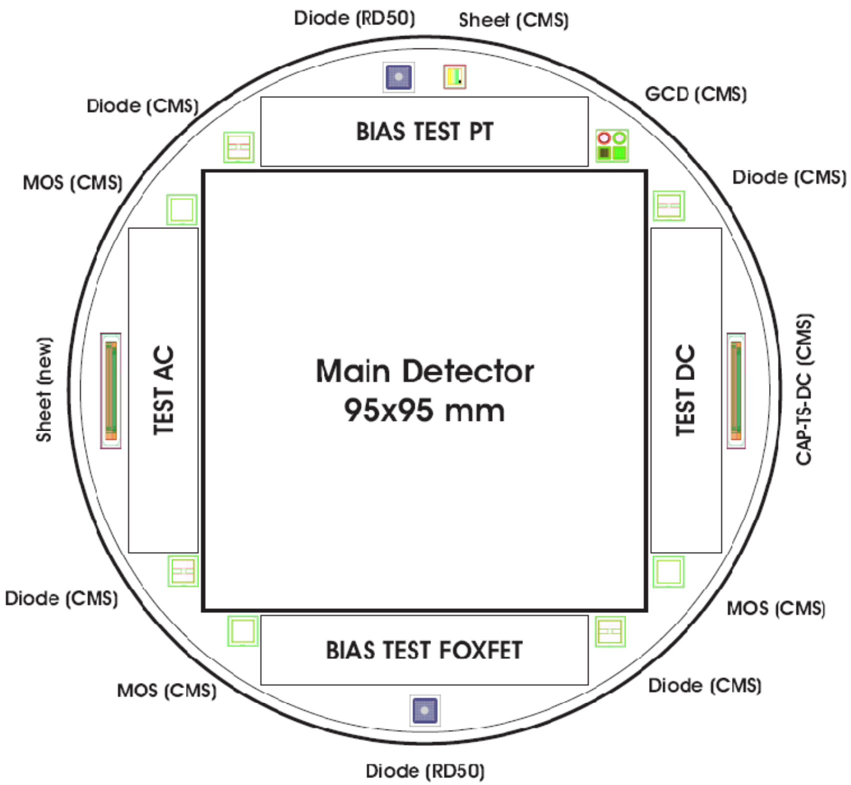


HPK Sensor Order

- Single-sided AC coupled SSD
- **Sensor size:** 91,5 x 91,5 mm² (± 0,04 mm)
- **Wafer thickness**: approx. 320 µm
- **Resistivity**: such that depletion voltage: 50 V < Vdepl < 100 Volt
- **Biasing scheme**: poly-Silicon Resistor with 20 MΩ (± 5 MΩ)
- **Number of strips:** 1792 (= 14 x 128)
- **Strip pitch:** 50 um pitch, without intermediate strips
- **Strip width:** 12.5 um

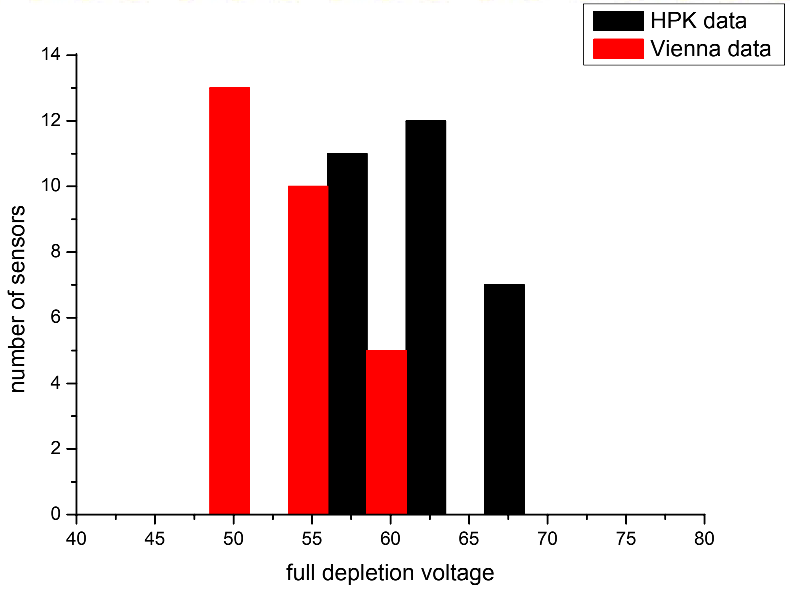
- Main detector have been/will be used to
  - Build prototype modules to test new readout chip (Testbeam took place in Oct '07 at SPS@CERN)
  - Build modules for LC-TPC project
  - Build long ladders

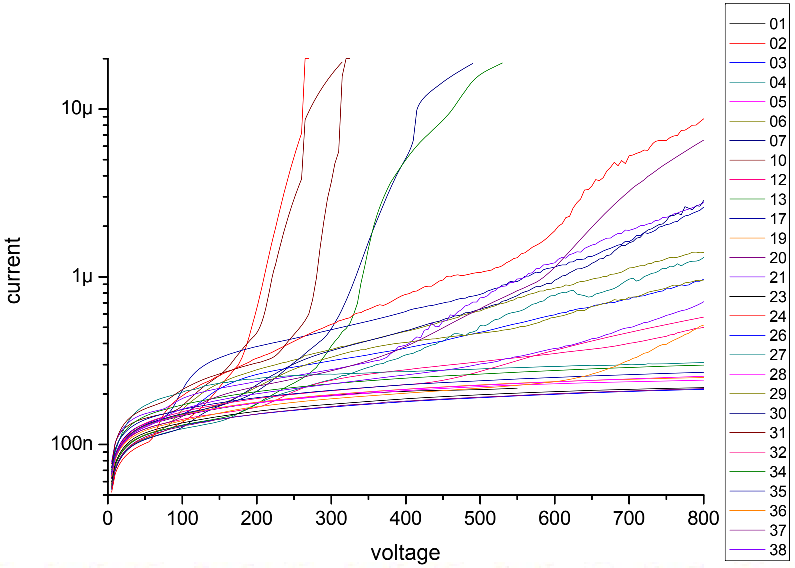
- **We ordered 35 HPK Sensors**
  - 30 “normal sensors”
  - 5 “alignment sensors”
- **Have been delivered Oct ‘07**



IV and CV Results

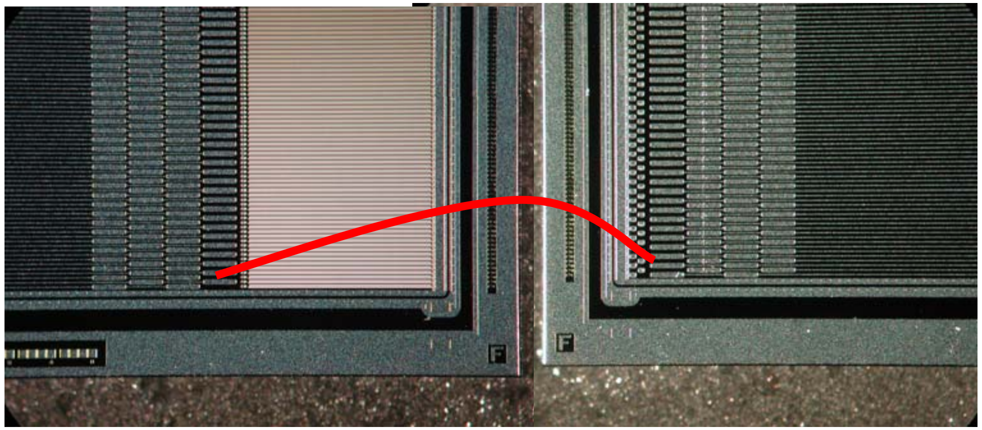
- We requested a resistivity such that depletion voltage is between 50 and 100V
- All sensors fully deplete between 47-58V, average at 52.5V
  - Resistivity is **6.7 kOhmcm** (rough estimate since more exact measurement on TS diode possible)
  - Safe operating voltage: 70-90V
- IV measurements up to 800V show some breakthroughs around 200-300 V

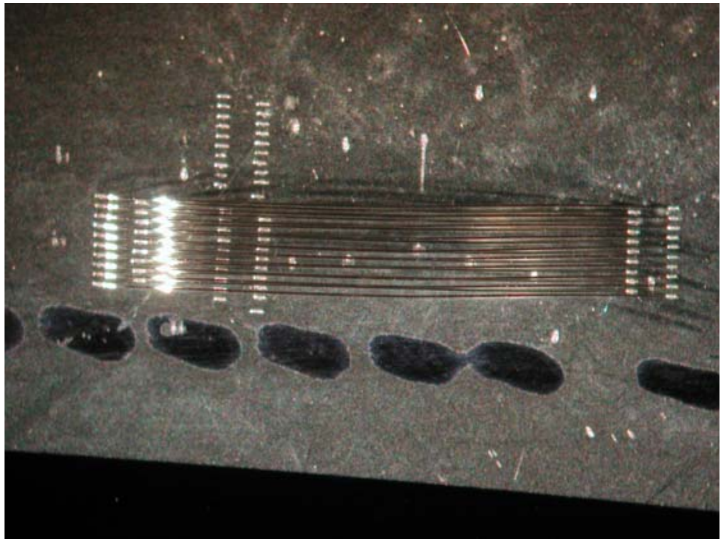




What we learned already: poly-Si

- Bonding problem for daisy-chained sensors (long ladders)
  - Because of the length of the poly-resistor the wire bonds connecting both sensors must be **5mm** long (at 50um pitch)
- We did some bonding tests and this seems to be a problem.
  - Bonds bend and touch each other
- Flipped sensors
  - No alternative since “near” sensor needs to be bonded on both sides
- Other alternative: use punch-through or FOXFEST biasing, since it requires less space (achievable resistor value still unclear)





HPK Multi geometry mini sensor

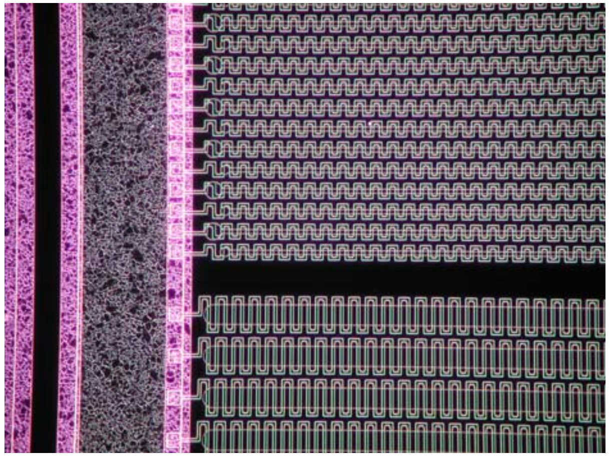
Sensor order at HPK contains several smaller sensors as well:

1. **Mini sensors to test FOXFET and punch-through biassing to circumvent problem with large poly-resistors**

   128 channels with pitch=50um with different biasing schemes

2. **A multi-geometry mini sensor:**

- 256 strips with 50um pitch
- 16 zones with 16 strips each
- Layout constant within each zone
- **Strip width** and **number of intermediate strips** vary between the zones



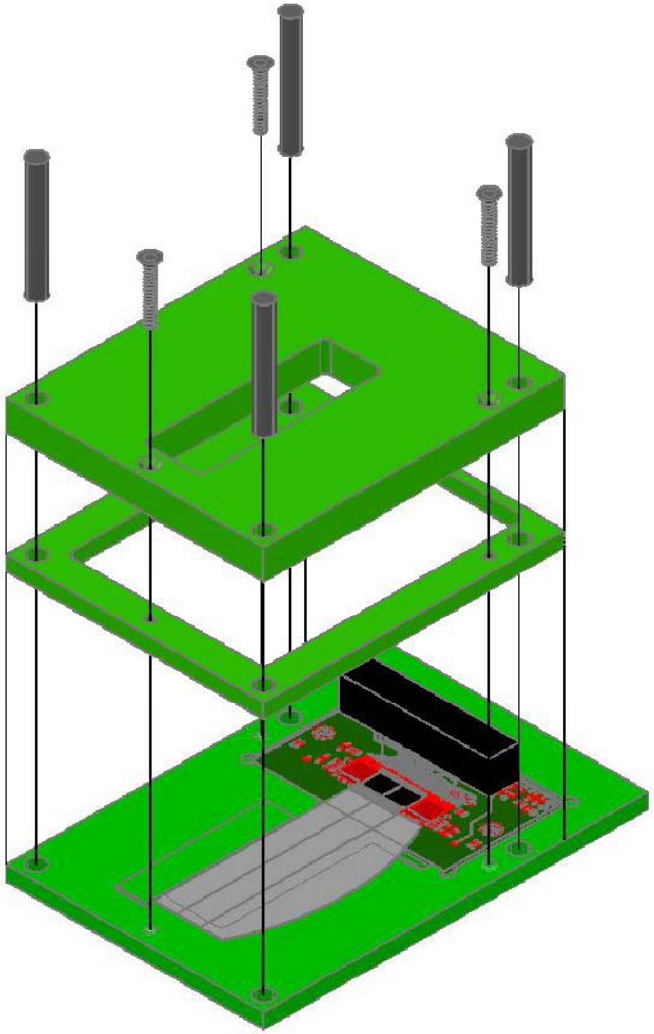
strip width [µm]	intermediate strips
5	no
10	no
12.5	no
15	no
20	no
25	no
5	single
7.5	single
10	single
12.5	single
15	single
17.5	single
5	double
7.5	double
10	double
12.5	double

Testbeam with multi-geometry mini sensor

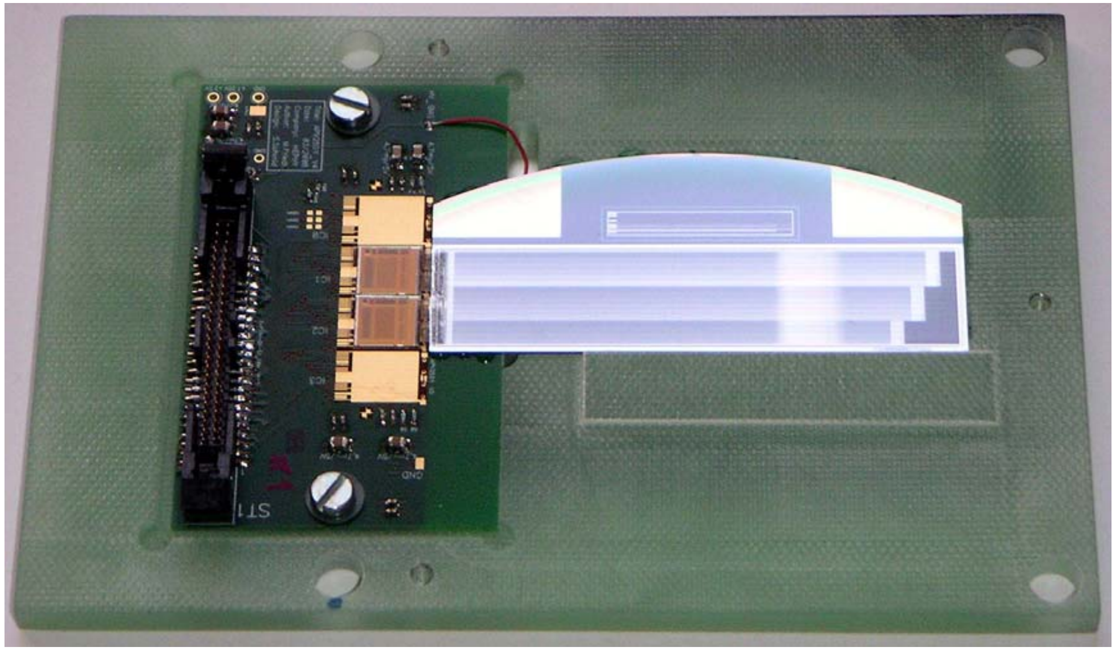
- 120GeV Pions from CERN SPS accelerator
- Took place last and this week (until June 4th)

- The goal of this testbeam:
  - Evaluate the best strip geometry of silicon strip sensors with 50 micron pitch to achieve the highest possible spatial resolution
  - For this purpose we are using a dedicated mini sensor with different zones, each with a different strip geometry:
    - Different strip widths
    - 0, 1 or 2 intermediate strips
  - We are using the fine resolution of the EUDET pixel telescope to get high precision tracks to determine the residuals for our DUTs [Devices under Test]

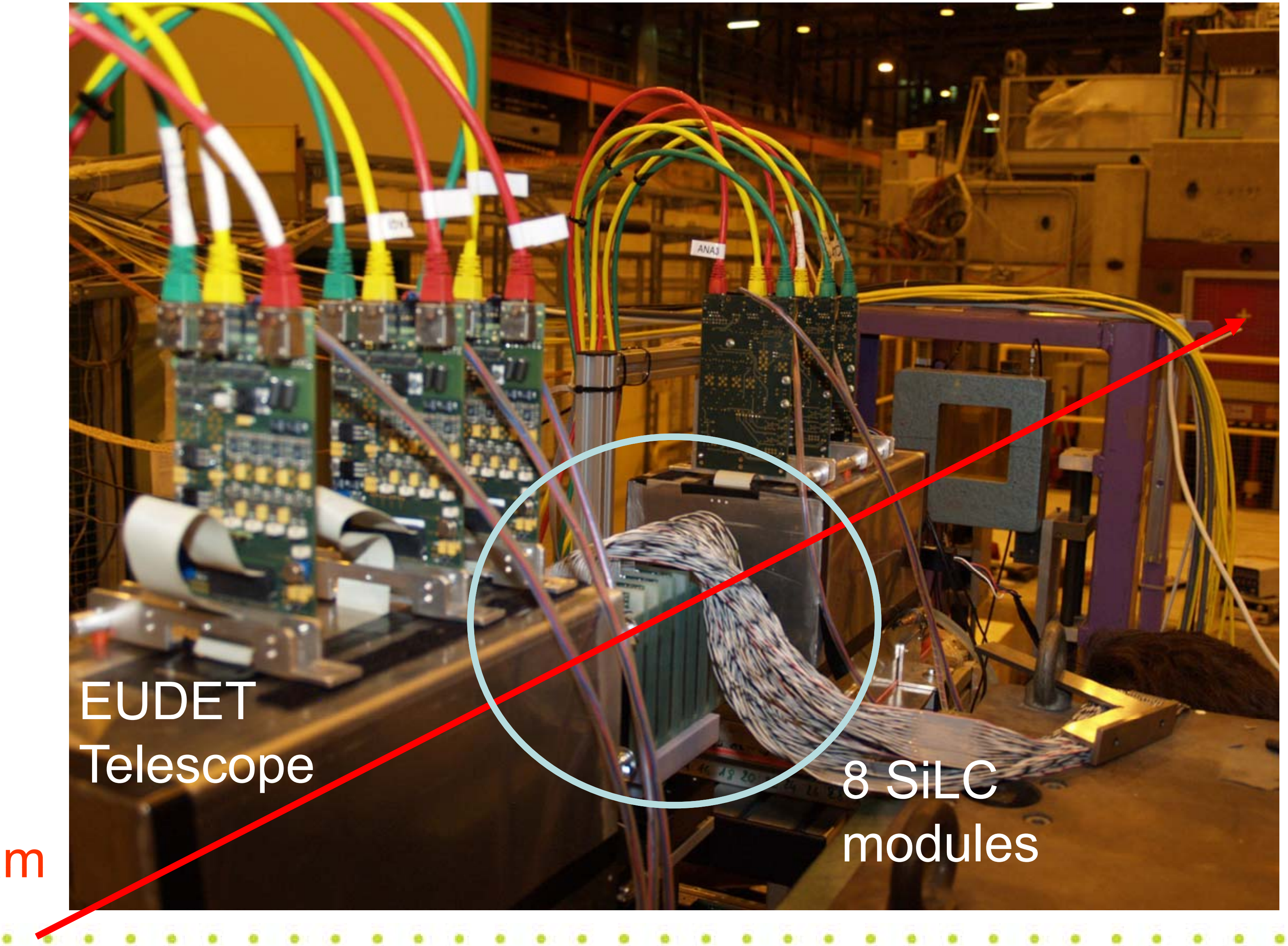
DUT Module



9 modules have been built in Vienna:



8 Modules together in the Testbeam Setup

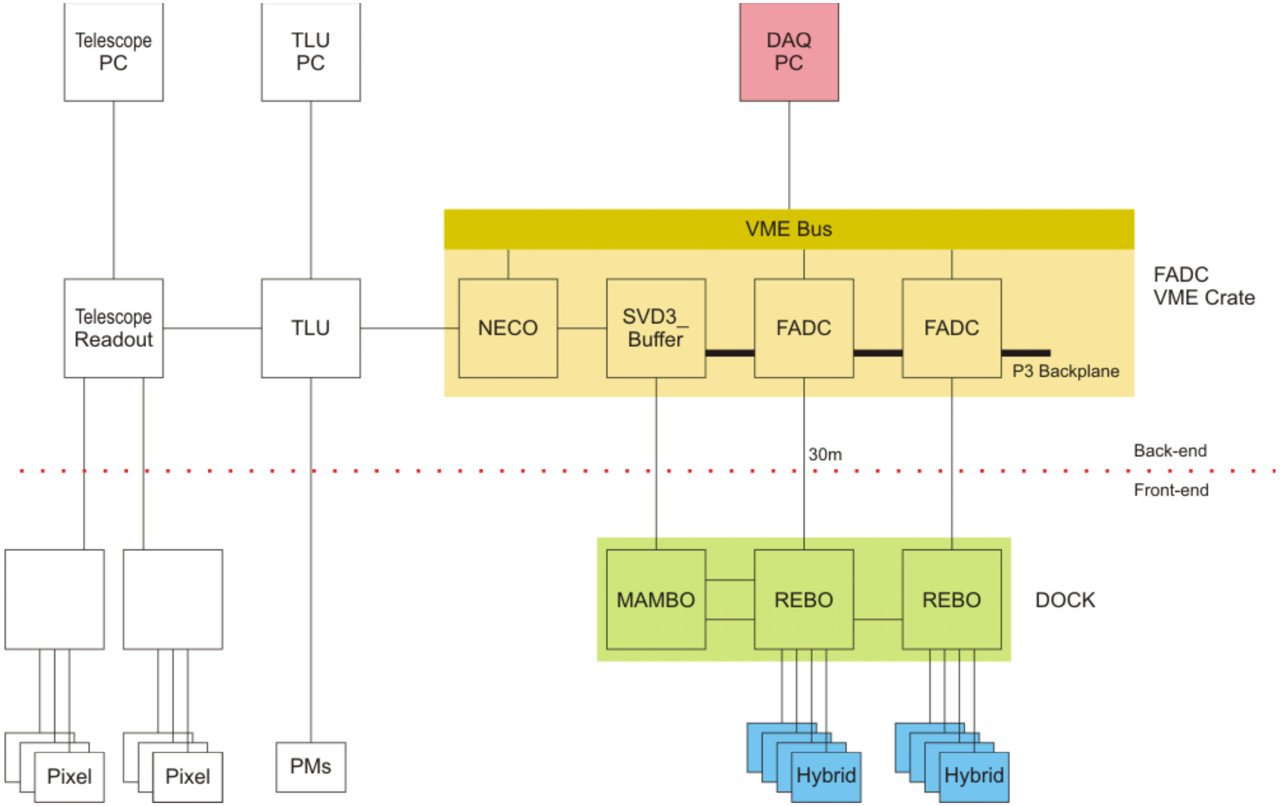


DAQ is using APV25 chip

- APV25 is readout chip of CMS Silicon Tracker

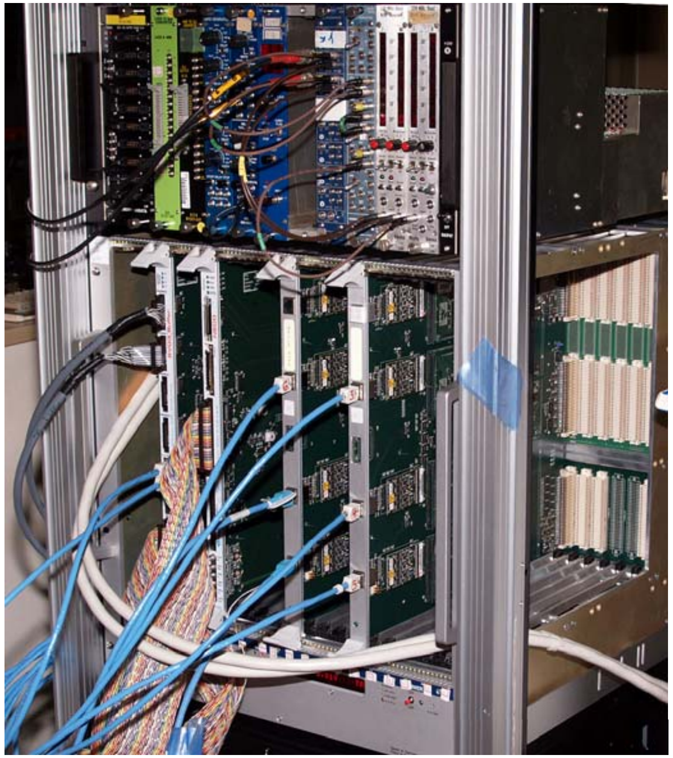
- Frontend (FE) Hybrids are connected to Repeater Boards (REBO)
- Two 9U VME Boards with FADCs are reading data and digitalize them
- PC running CVI (LabWindows) is used for online monitoring and to store data

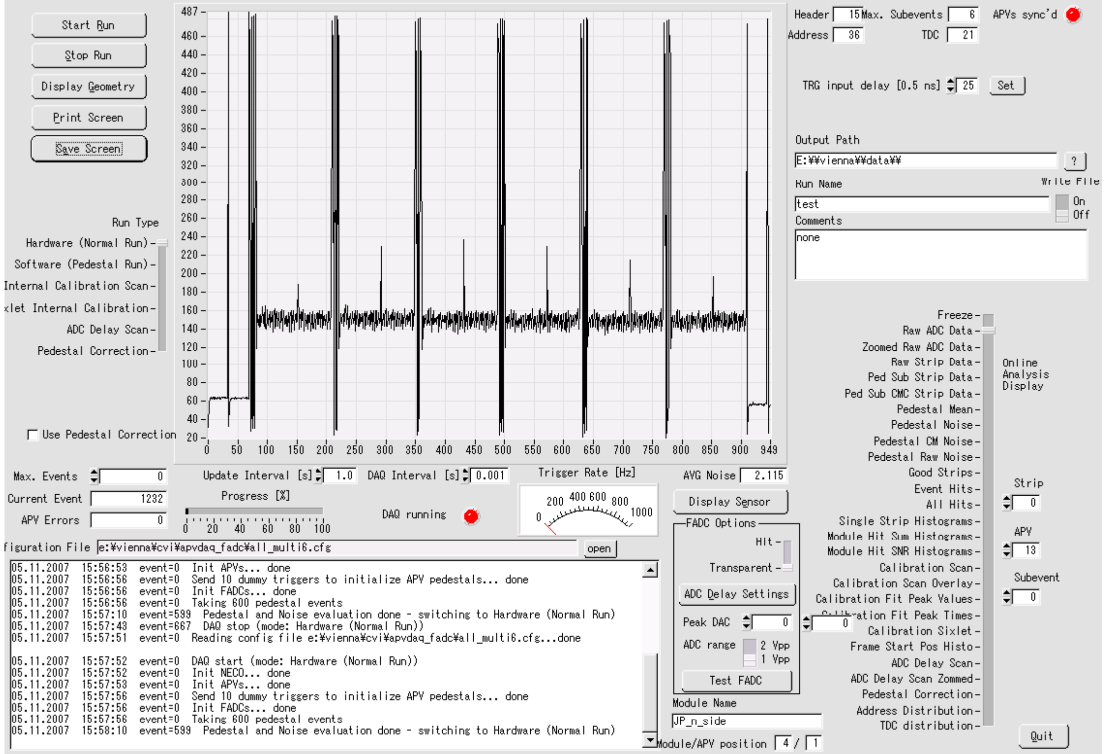
Controller board has LVDS I/O to directly read trigger and timestamp data from TLU box



DAQ Hardware and Software

- DAQ Hard- and Software (including predecessors) has already been used for more than 10 testbeams in the past.
- Thus, everything is pretty stable.





☐ Use Pedestal Correction

Header 15 Max. Subevents 6 APVs sync'd ●
Address 36 TDC 21
TRG input delay [0.5 ns] 25
Output Path E:¥¥vienna¥¥data¥¥
Run Name test
Comments none
Max. Events 0
Current Event 1232
APV Errors 0
Update Interval [s] 1.0
DAQ Interval [s] 0.001
Progress [%]
AVG Noise 2.115
Peak DAC 0
ADC range 2 Vpp 1 Vpp
Module Name JP_n_side
Module/APV position 4 / 1
Strip 0
APV 13
Subevent 0
figuration File e:¥vienna¥cvi¥apvdaq_fadc¥all_multi6.cfg

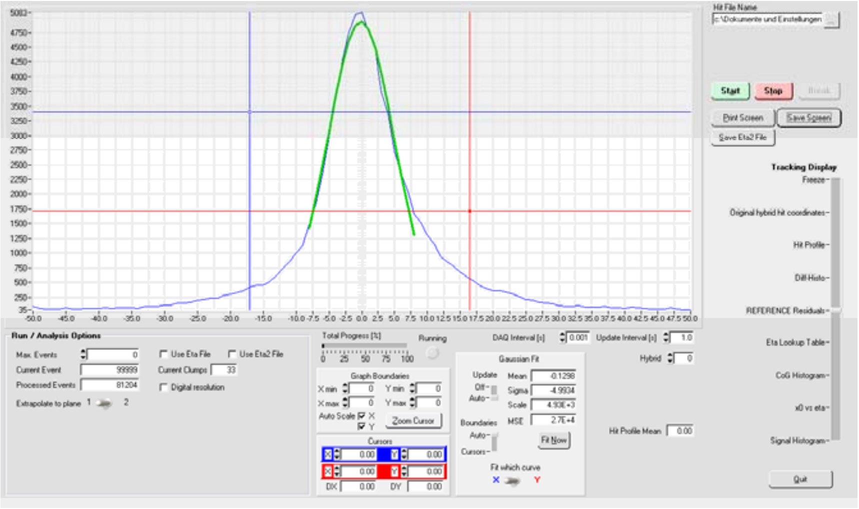
```
05.11.2007  15:56:53  event=0  Init APVs... done
05.11.2007  15:56:56  event=0  Send 10 dummy triggers to initialize APV pedestals... done
05.11.2007  15:56:56  event=0  Init FADCs... done
05.11.2007  15:56:56  event=0  Taking 600 pedestal events
05.11.2007  15:57:10  event=599  Pedestal and Noise evaluation done - switching to Hardware (Normal Run)
05.11.2007  15:57:43  event=667  DAQ stop (mode: Hardware (Normal Run))
05.11.2007  15:57:51  event=0  Reading config file e:¥vienna¥cvi¥apvdaq_fadc¥all_multi6.cfg...done

05.11.2007  15:57:52  event=0  DAQ start (mode: Hardware (Normal Run))
05.11.2007  15:57:52  event=0  Init NECO... done
05.11.2007  15:57:53  event=0  Init APVs... done
05.11.2007  15:57:56  event=0  Send 10 dummy triggers to initialize APV pedestals... done
05.11.2007  15:57:56  event=0  Init FADCs... done
05.11.2007  15:57:56  event=0  Taking 600 pedestal events
05.11.2007  15:58:10  event=599  Pedestal and Noise evaluation done - switching to Hardware (Normal Run)
```

Preliminary Results

Resolution across all zones:

(without telescope data)

- Residual RMS = 4.99 um (against neighbor layers 2+4 only)
- Residual RMS = 6.35 um (REFERENCE against all 7 other layers) -> needs more sophisticated alignment



Hit File Name: c:\Dokumente und Einstellungen

Run / Analysis Options

Max. Events: 0
Current Event: 99999
Processed Events: 81204
Extrapolate to plane 1 2
☐ Use Eta File
☐ Use Eta2 File
Current Clumps: 33
☐ Digital resolution

Graph Boundaries
X min: 0
X max: 0
Y min: 0
Y max: 0
Auto Scale ☑ X ☑ Y

Cursors
X: 0.00 Y: 0.00
X: 0.00 Y: 0.00
DX: 0.00 DY: 0.00

DAQ Interval [s]: 0.001
Update Interval [s]: 1.0
Hybrid: 0

Gaussian Fit
Update Off – Auto –
Mean: -0.1298
Sigma: 4.9934
Scale: 4.93E+3
MSE: 2.7E+4
Boundaries Auto – Cursors –

Hit Profile Mean: 0.00

Data Analysis

Offline data analysis of DUT data:

- Pedestal subtraction
- Common mode correction
- Hit finding, Clustering
- Peak time reconstruction
- Track Reconstruction (non existing)

Existing Vienna analysis software

We have three possibilities for tracking:

- Use EUDET software as proposed by Ingrid
  - Need to transfer our data into LCIO format
- Use SiLC (Prague group) analysis software written in ROOT
  - Transfer data from telescope and DUT to ROOT files
- Include tracking algorithms in Vienna Analysis code
  - Transfer data from telescope into proprietary ROOT files

Summary

- Sensor baseline established:
  - FZ, p-on-n, high resistivity, 100-300um thick, 50um pitch
  - preferably DC coupled, otherwise biasing via PolySi, PT or FOXFET

- SiLC Goals:
  - Establish companies to deliver silicon detectors for future HEP experiments
  - First batch with HPK designed and successfully tested by SiLC Collab.

- Outlook / Future plan
  - Develop design, build and test detectors with fine pitch for ILC
  - Dual metal layer structure for in-sensor routing
  - Develop cheap, industrial bump-bonding technology
  - Detector thinning
  - 6” Double sided sensors
  - 8” (12”?) single sided DC sensors