Report from the Data Acquisition Session

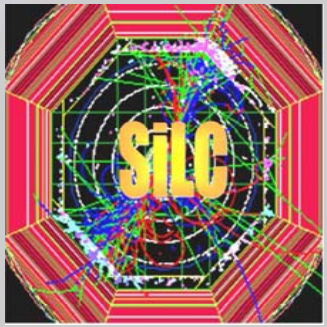
ECFA Study
Physics and Detectors for a Linear Collider

G. Eckerlin

ILC-ECFA Workshop,
Warsaw, June 11th 2008

Current DAQ R&D

Summary



Agenda

ECFA Study
Physics and Detectors for a Linear Collider

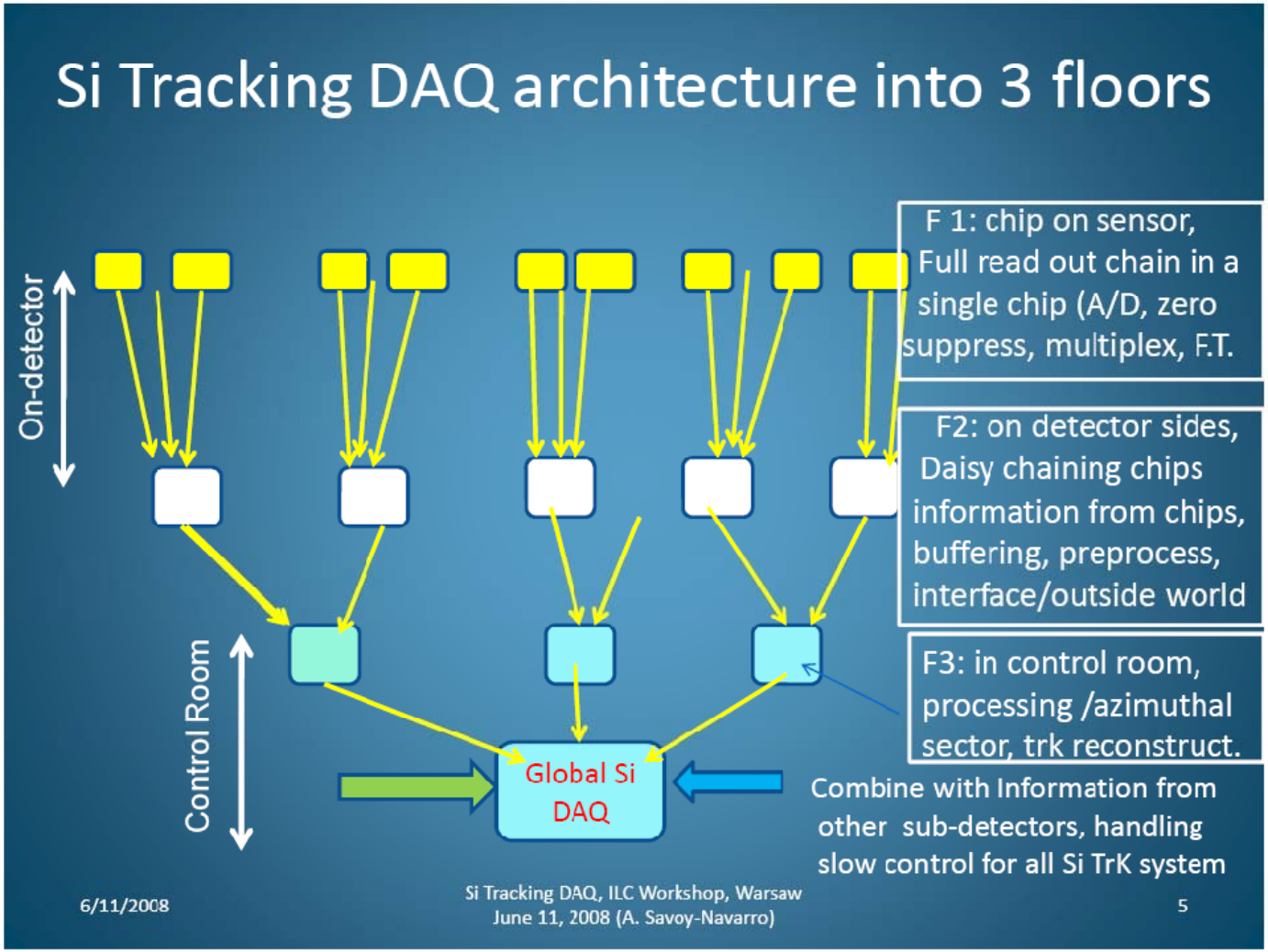
5. DAQ Calo/Tracking/VTX - room B (10:50-12:40)

joint detector session on DAQ

- Conveners: Caccia, Massimo; Winter, Marc; Timmermans, Jan; Vos, Marcel; Eckerlin, Gunter; Le Du, Patrick

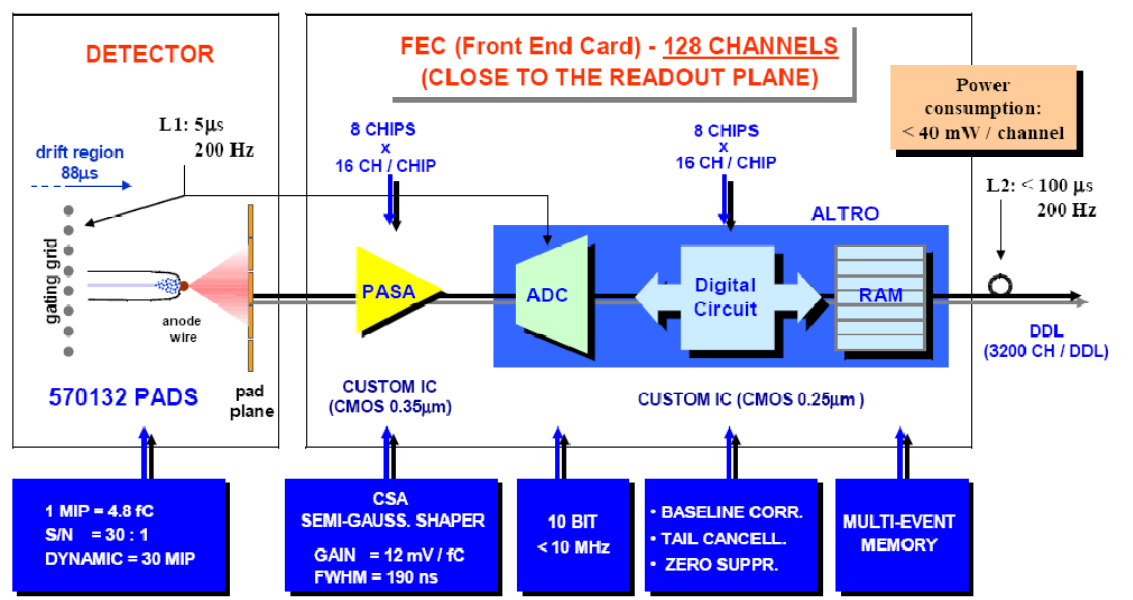
time	title	presenter
10:50	Silicon tracking DAQ	SAVOY-NAVARRO, Aurore
11:10	TPC read-out	JANSSEN, Xavier
11:30	The front end ASIC for CALICE	SEFKOW, Felix
11:50	On- and near-detector DAQ work for the EUDET calorimeters	BARTSCH, Valeria
12:10	Off-detector DAQ work for the EUDET calorimeters	WU, Tao

Silicon tracking DAQ (A.Savoy-Navarro)



3 stage DAQ approach for silicon strip trackers

LC TPC Front End Cards (X. Janssen)



Brussels, Lund, Bonn

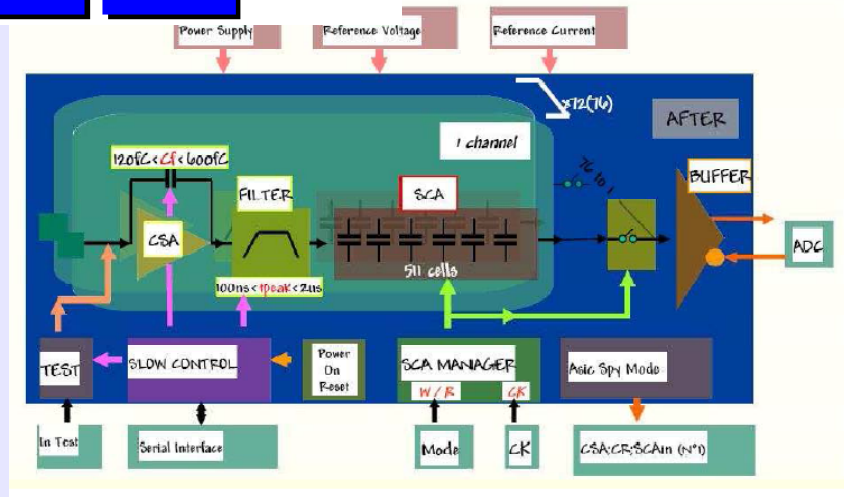
ALICE front end readout (ALTRO)

Digitizing on FE, digital buffers

CEA-Saclay

T2K front end readout (AFTER)

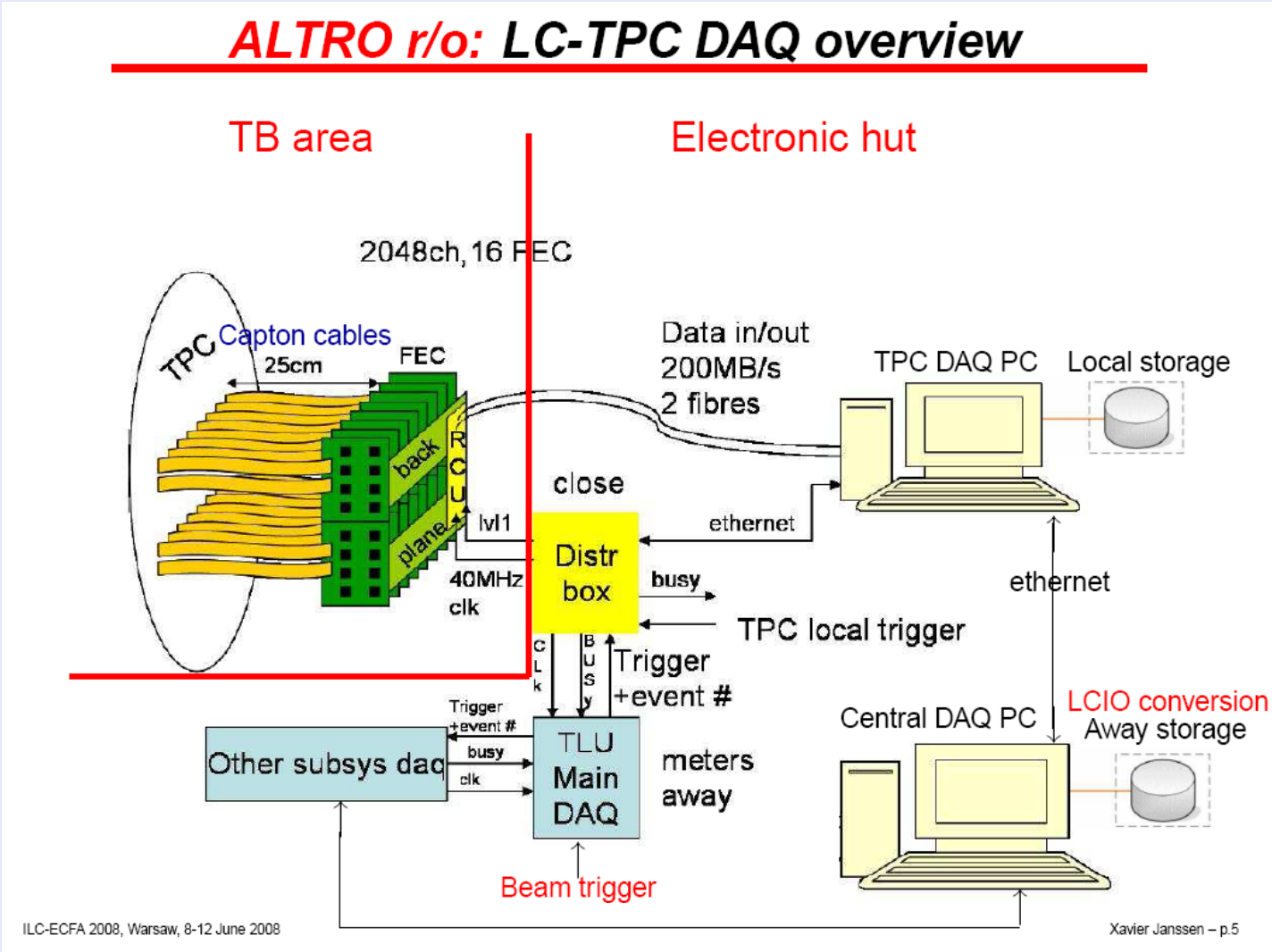
Analog pipeline, ADC off detector



AFTER ASICS:

- 72 Analog channels
- 2 input polarities
- 4 gains: 120, 240, 360 and 600 fC
- 16 peaking times: from 100 ns to 2 ps
- 511 analog memory cells / channel

LC TPC Testbeam DAQ (X.Janssen)



Test beam DAQ based on ALICE DAQ

+ EUDET TLU

+ Distribution box for trigger/event signal distribution

+ local/common DAQ

ILC Calorimeter DAQ (Valeria Bartsch)

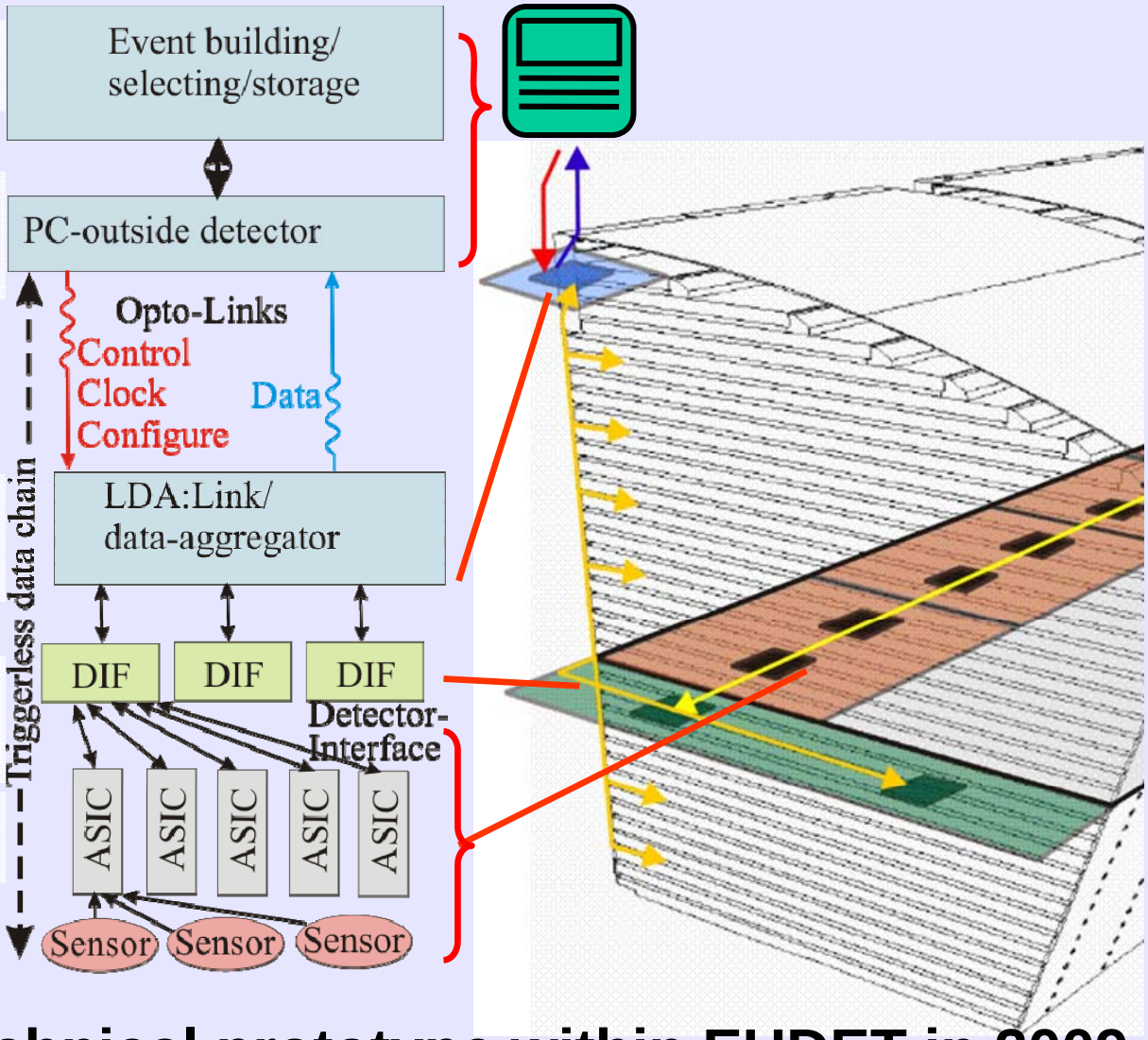
DAQ software

Off Detector Receiver (ODR)

Link Data Aggregator (LDA)

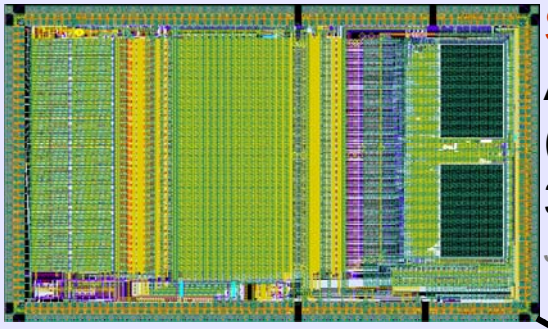
Detector Interface (DIF)

Detector Unit



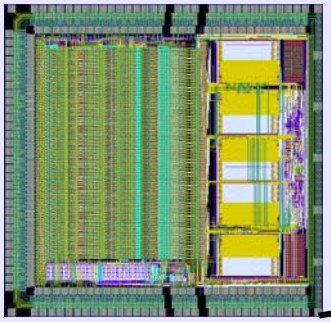
Preparing for the technical prototype within EUDET in 2009

2nd generation ASICs for Calo R/O (F. Sefkow)

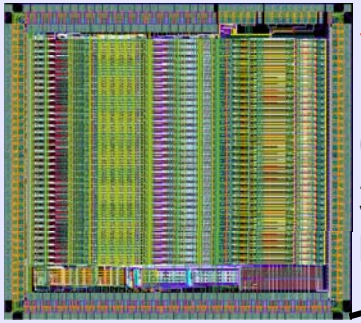


SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07

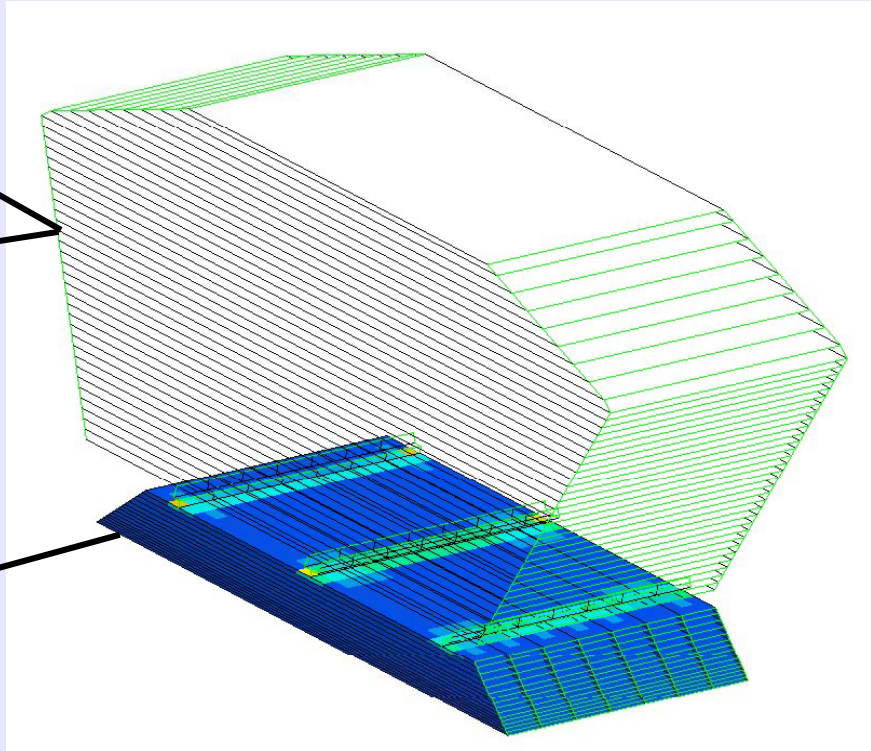
8-bit DAC (0-5V) for SiPM gain adjustment
2 gains / 12 bit ADC for energy measurements
Auto-trigger for zero suppression
12 bit TDC for time measurements (step ~100 ps)
Analog memory for time and charge (depth = 16)



HARDROC
Digital HCAL
(RPC, μmegas or GEMs)
64 ch. 16mm²
Sept 06



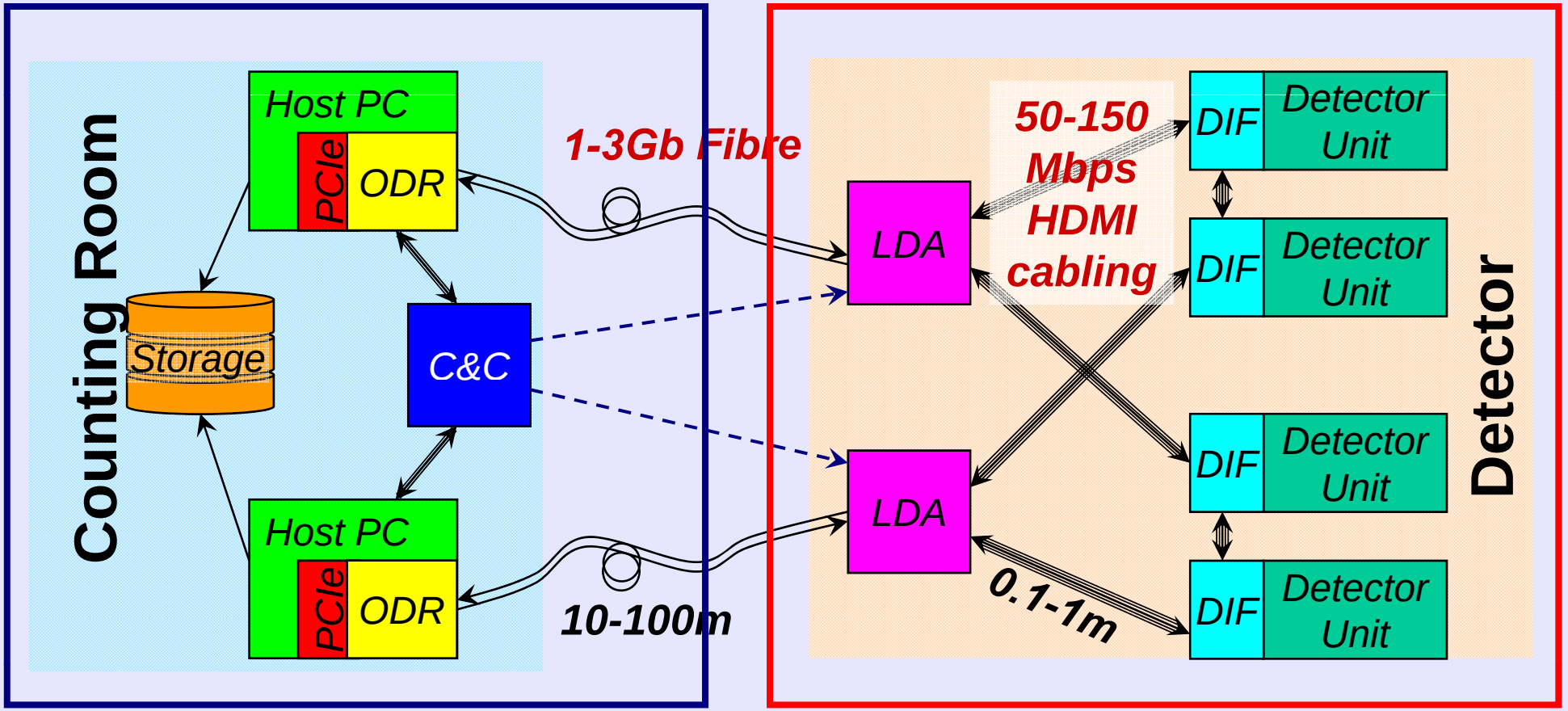
SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06



DAQ Architecture of CALICE

covered in Tao's talk

covered in Valeria's talk



EUDET DAQ will use DOOCS (Tao Wu)

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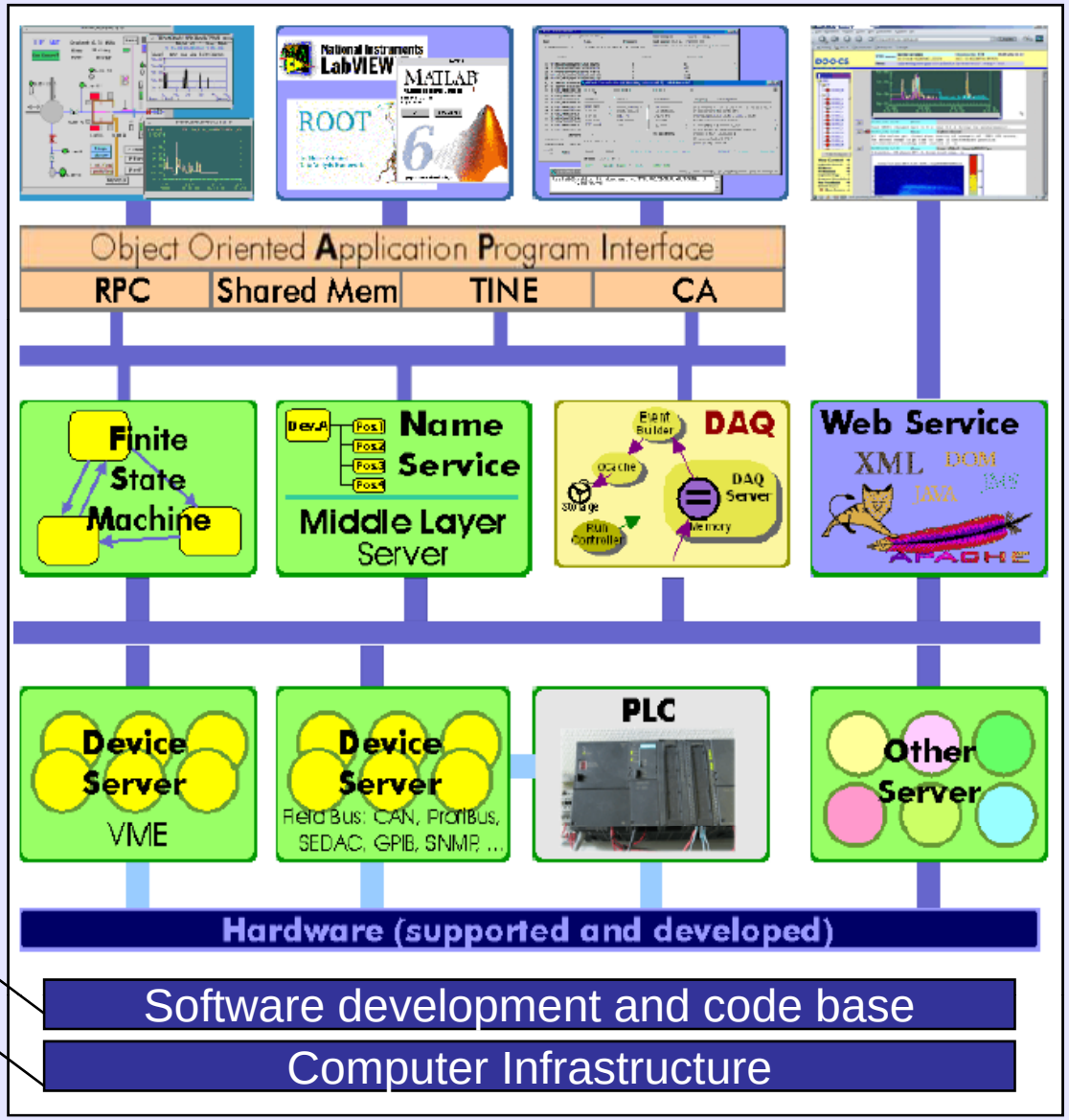


The Distributed Object Oriented Control System will also be used for XFEL Control and DAQ.

Off Detector DAQ & Software (Tao Wu)

Summary: Off-detector & Software development of DAQ System

- Off-detector Receiver has been built for receiving, event building & data storage; performance has been tested;
- Clock & Control instead of triggers, the board will be built soon;
- DOOCS framework is reusable & suitable for our DAQ system.
- How to apply DOOCS for the CALICE technical prototype is well understood
- The basic design for the CALICE application is ready
- Interface to the hardware is the starting point of the implementation of the CALICE project within DOOCS
- DAQ software is in designing phase…

Summary

- Newly developed readout systems get closer to reality

  ILC like architectures and real front end designs approaching

  encouraging to see R&D groups using common interfaces & standards

  good examples : EUDET (FP6), continue with DEVDET (FP7) ?

- Still to be done

  address further common issues (calibration, commissioning, detector ctrl)

  need to think about online data formats (offline software expects LCIO)

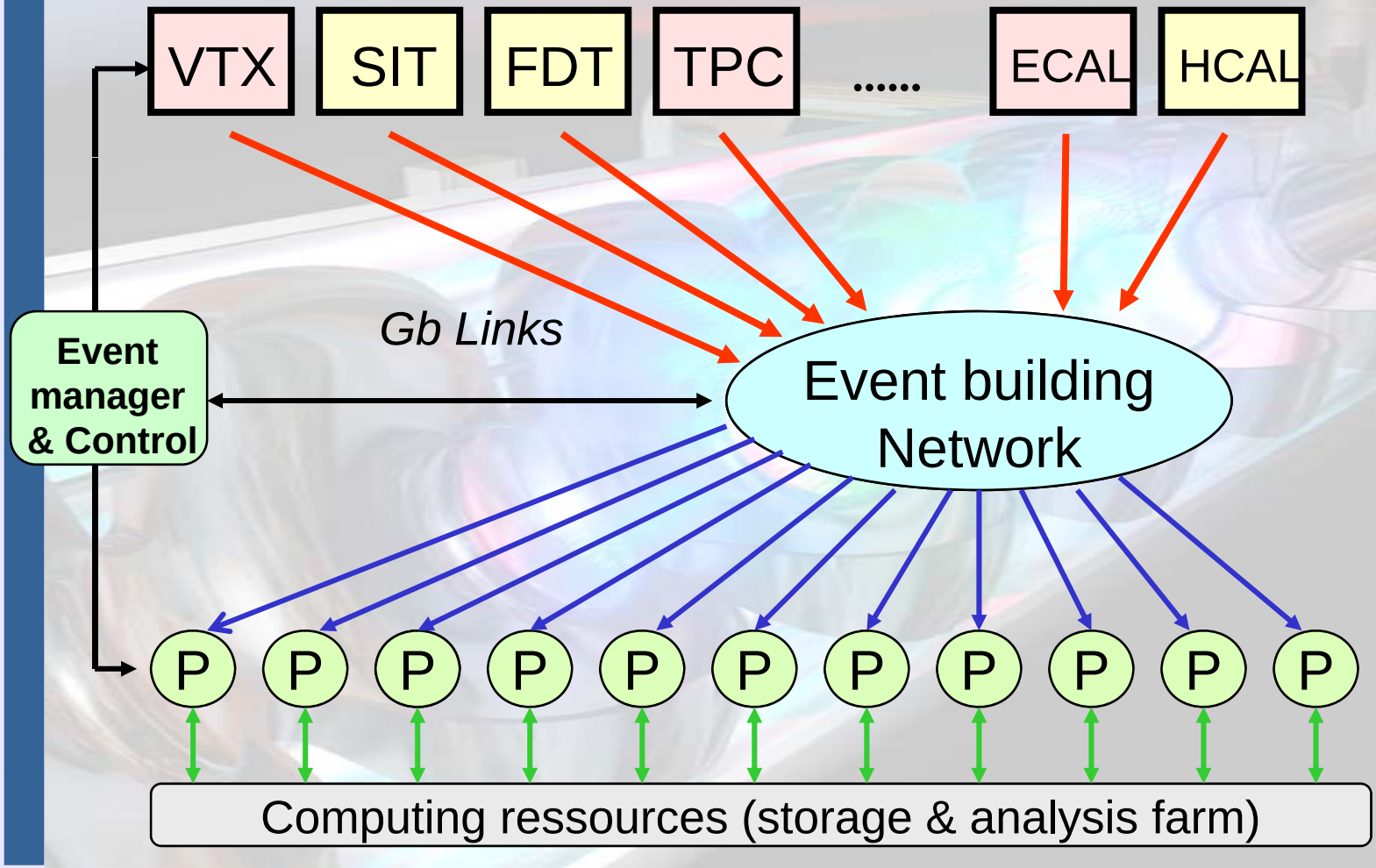
  need to learn how to profit best from new technologies (like ATCA/µTCA/AMC)

Thank you !

Backups

Keeping the concept DAQ Concept in mind

General concept unchanged since Tesla TDR



~ 10^9 channels
no hardware trigger
1 ms pipeline

readout between trains
~ 200 ms
commercial hardware

software event selection
- full train data to 1 node
- full detector information
- full train information

-> flexible & efficient

How to connect the Front End Readout

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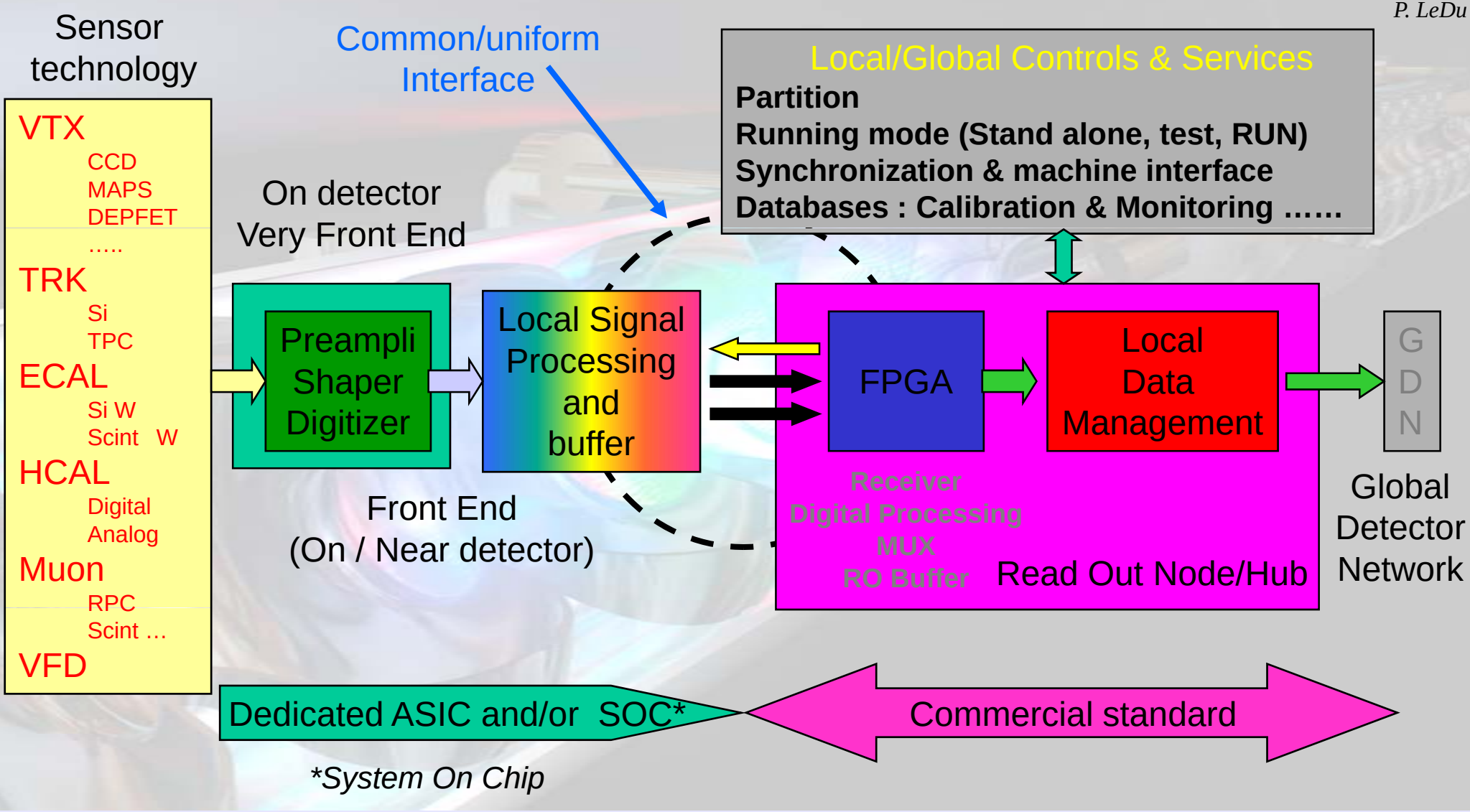
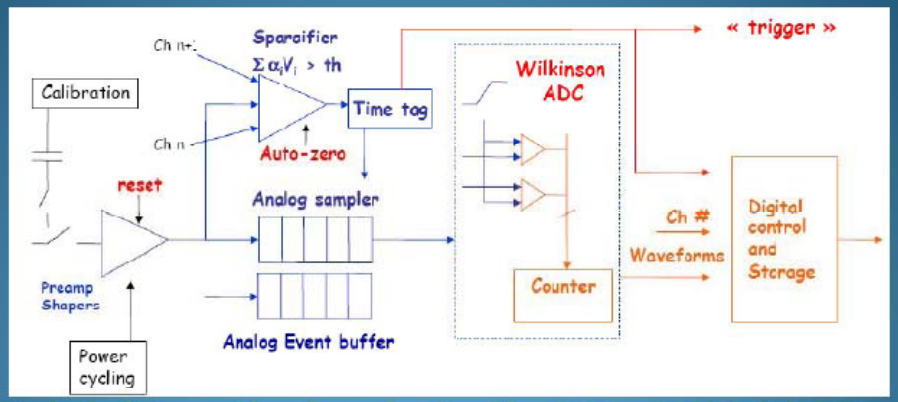
P. LeDu



Front End R&D for SiLC (A.Savoy-Navarro)

Floor 1: FE chip on elementary module



Full readout chain integration in a single chip, 512 or 1024 ch in 90nmCMOS

- Preamp-shaper
- Sparsification Trigger decision on analogue sums (3 or 5 adjacent channels)
- Sampling 8-deep sampling analogue pipe-line
- Analogue event buffering: Occupancy: 8-16 deep event buffer
- On-chip digitization 12-bit ADC (highly multpiplexed)
- Buffering and pre-processing: Centroids, χ2 fits, lossless compression & error codes
- Calibration and calibration management
- Power switching (ILC duty cycle)
- Digital control: operation fully programmable (all settings of chip operations), fault tolerance, robustness, reliability, flexibility.

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Front End R&D for SiLC (A.Savoy-Navarro)

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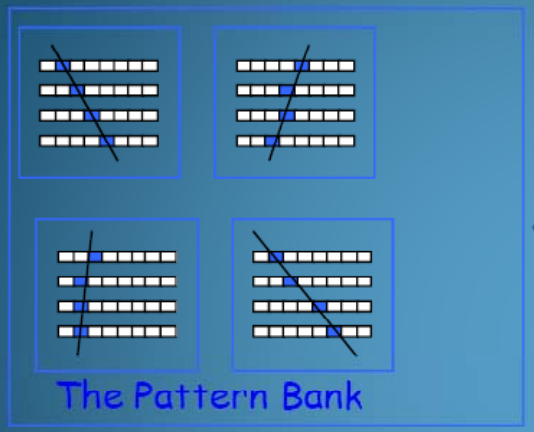
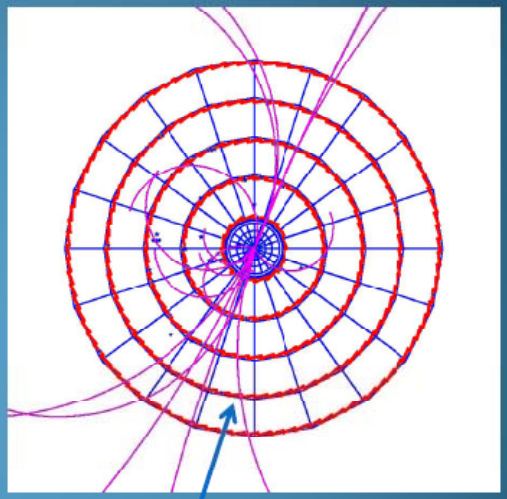
Floor 3: Si TRK DAQ in the C.R., integration phase





REAL TIME PROCESSING at floor3:
organize the processors for instance regrouping F2 elements belonging to a same azimuthal sector and perform tracking , a la CDF or FTK=FastTrack Finding (LHC).
SLOW CONTROL: synchronisation (Clock), power supplies, calibration signal, operation Parameters settings ....
COMBINE information from SiTracking wih other SUBDTECTORS

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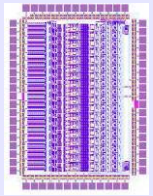
2nd generation ASICs for Calo R/O (F. Sefkow)

- Add auto-trigger, analog storage, digitization and token-ring readout !!!
- Include power pulsing : <1 % duty cycle
- Address integration issues asap
- Optimize commonalities within CALICE (readout, DAQ…)

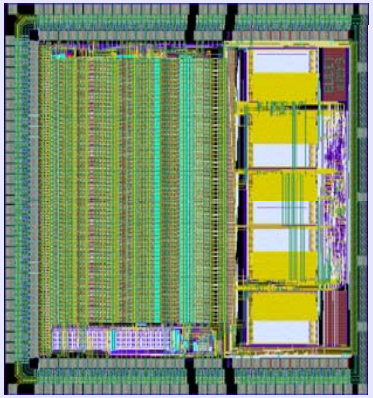
HCAL

FLC_PHY3 (2003)



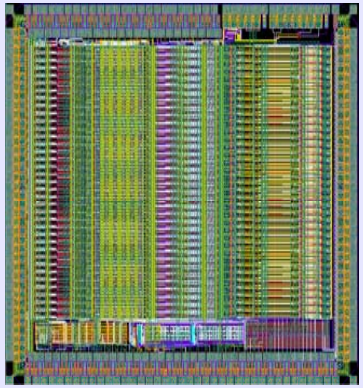
HCAL

HardROC (2006)



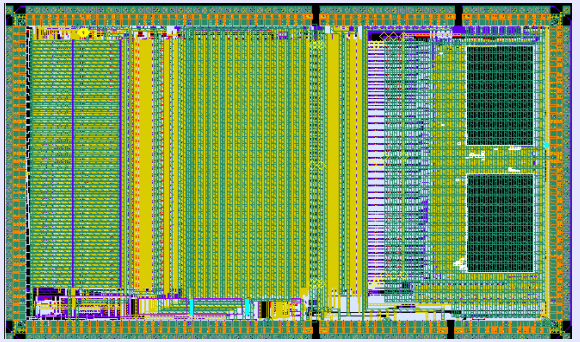
HCAL

SkiROC



HCAL

SPIROC



Front End R&D Examples

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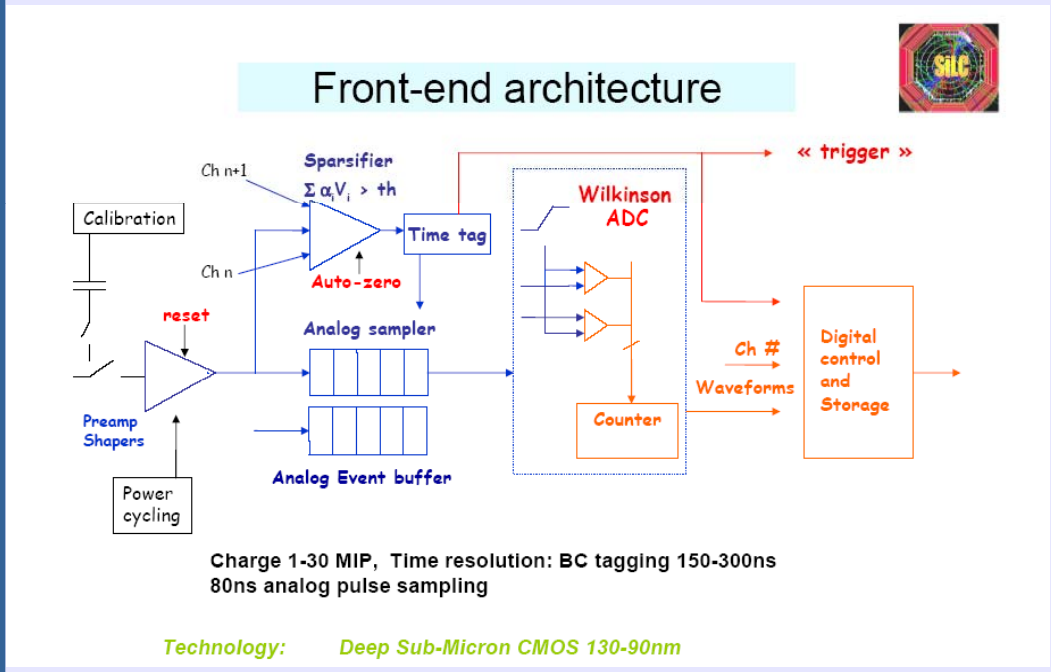
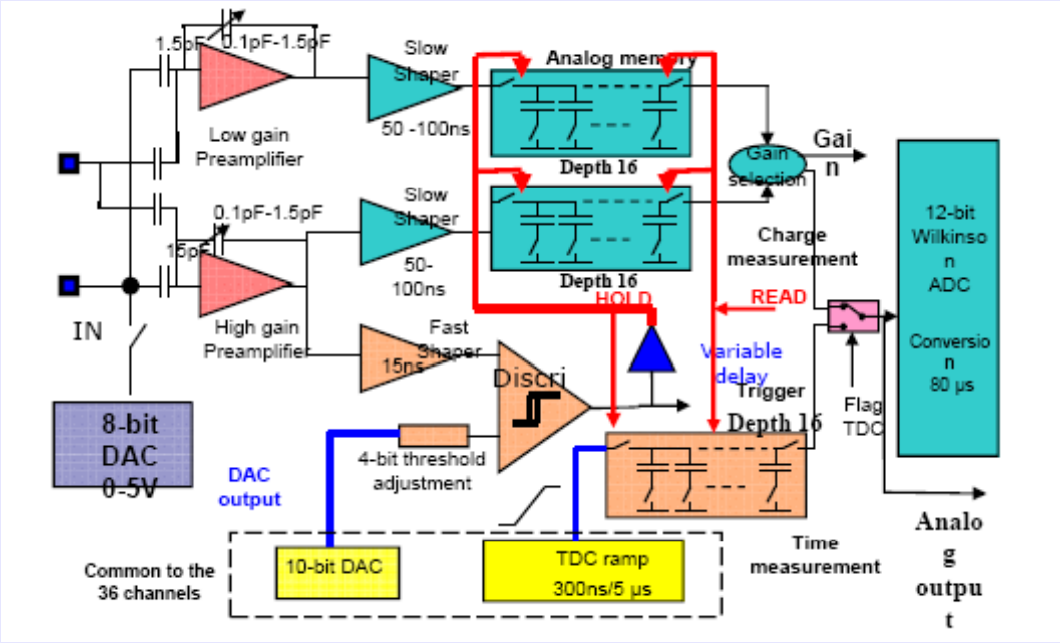
Architecture of CMOS readout chip of Silicon Strips (A. Savoy-Navarro for SiLC in the tracking session)

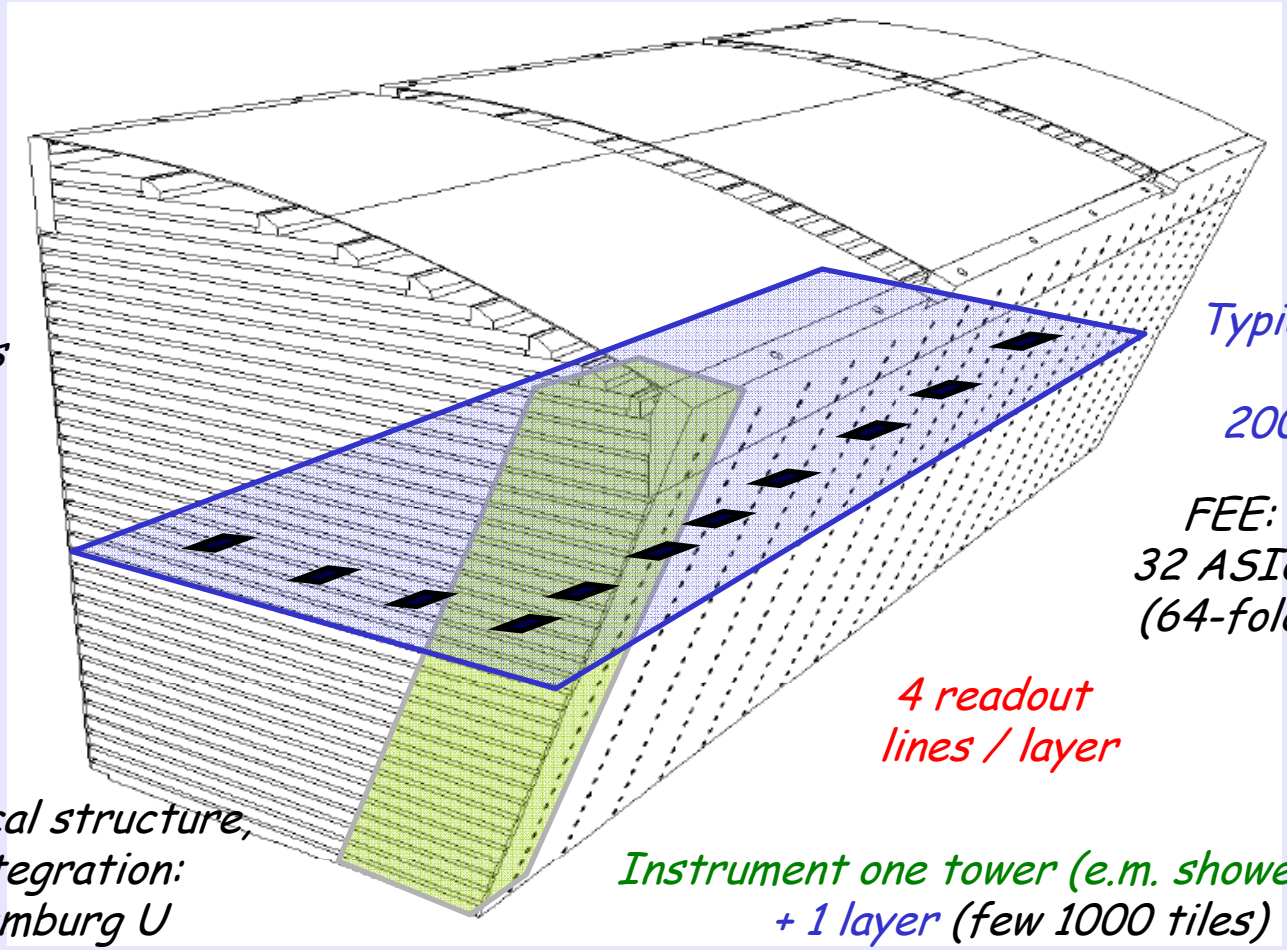


New ASIC readout chip for analog HCAL tests (F. Sefkow for CALICE in the Calorimeter session)



Many designs now fully integrate shaping, digitizing, hit detection, processing and digital buffering.
Getting closer to a real design for the ILC operation.
Output mostly digital via serial links (LVDS)

EUDET AHCAL Prototype (V. Bartsch)

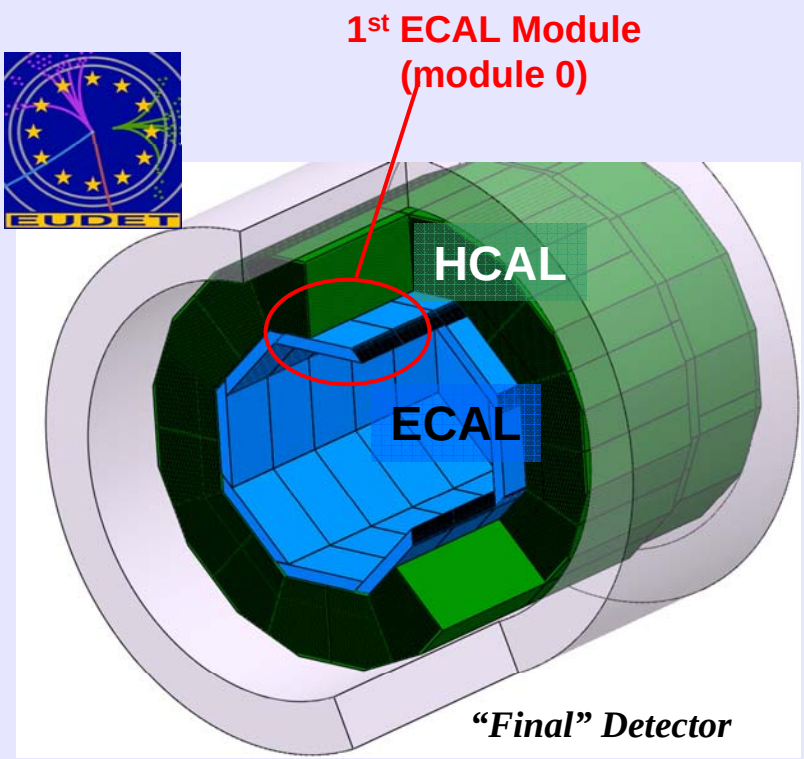


- 3 different detector types: ECAL, AHCAL, DHCAL
- study of full scale technological solutions

ILC Calorimeter DAQ (Valeria Barsch)

- ILC Calorimetry will use particle flow algorithms to improve energy resolution
  - => 1cmx1cm segmentation results in 100M channels with little room for electronics or cooling
- Bunch structure *interesting:*
  - ~200ms gaps between bunch-trains
  - Trains 1ms long, 300ns bunch spacing
- Triggerless

=> ~250 GB of raw data per bunch train need to be handled



M. Anduze