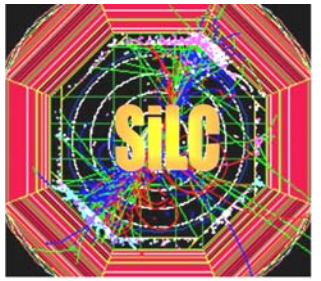
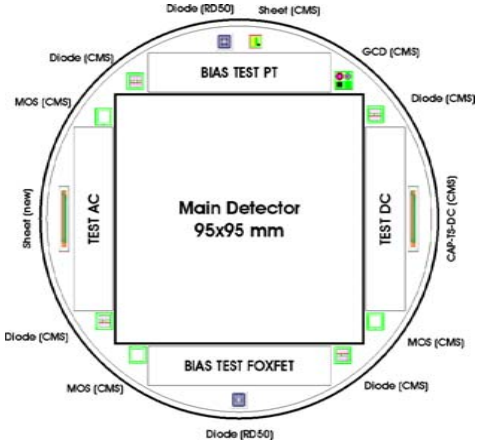
SiLC R&D Status Report

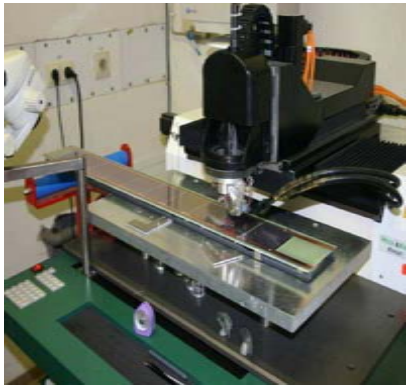
Valeri Saveliev (OSU)
on behalf SiLC Collaboration

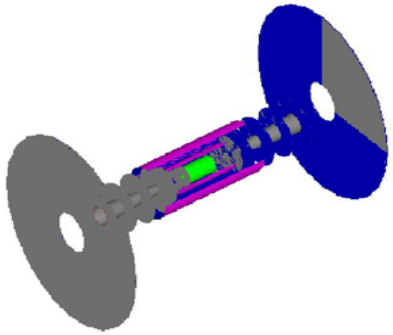


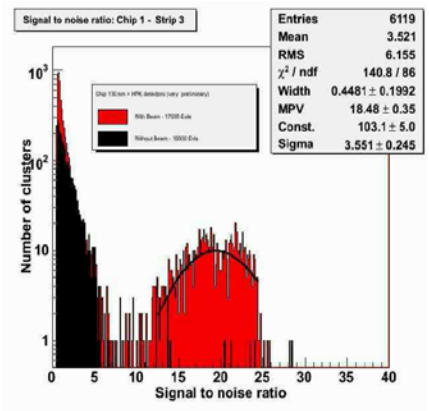
Main Topics

- ✓ R&D Sensors,
- ✓ R&D Electronics,
- ✓ Mechanics,
- ✓ Simulation,
- ✓ Test,
- ✓ Next









R&D on Sensors

- ✓ R&D on baseline micro-strip sensors, novel technologies,
- ✓ Quality Test Control (QTC),
- ✓ Development of collaboration with industry

BaselineTechnologies of Si Sensors

Future Linear Collider Experiment will have a large number of silicon sensors

- Order of 100-200 m2 (CMS has 200 m2)
- Tradeoff between large scale, precision, material budget and power consumption are main direction

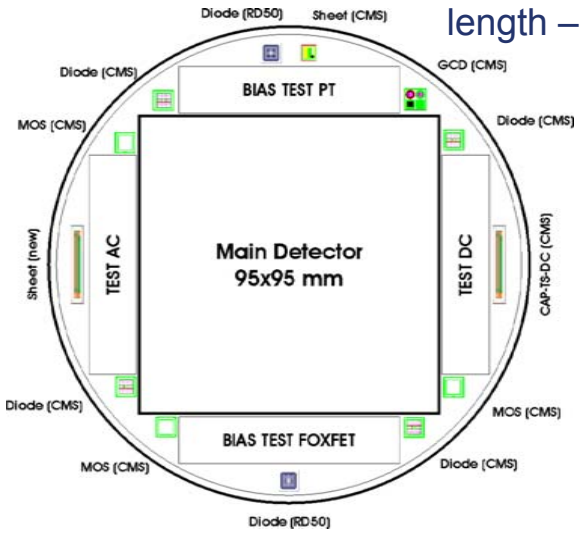
✓ SiLC baseline for outer layers
- ✓ 8”, high resistivity FZ sensors
- ✓ Thickness: 200 μm
- ✓ AC coupled strips
- ✓ 50μm pitch
- ✓ Strip length between 10 cm and very maximum 60 cm

✓ SiLC baseline for inner layers
- ✓ double sided 6” high resistivity FZ sensors
- ✓ AC coupled strips
- ✓ 25-50μm pitch

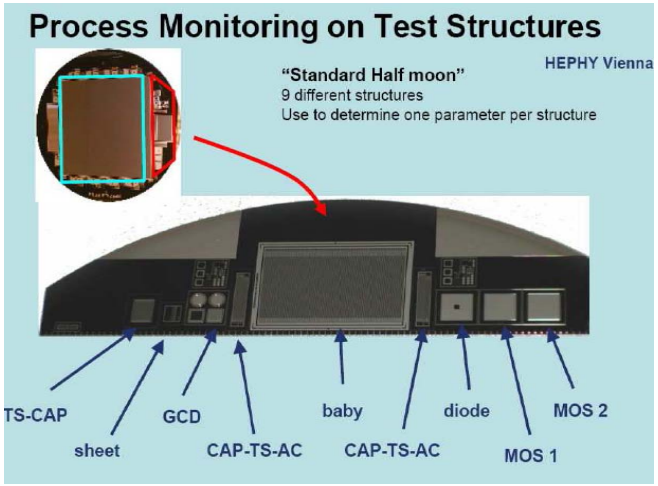
✓ SiLC baseline for inner forward layers:
- ✓ Pixels

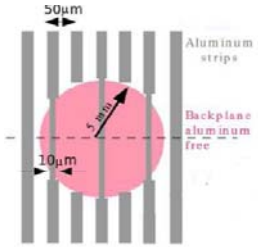
R&D on Sensors: μStrip Sensors

NEW 2007: HPK μstrips, 6'' wafer,
BUT: pitch – 50 μm,
thickness - 320 μm,
length – 9.15 cm



Test structures

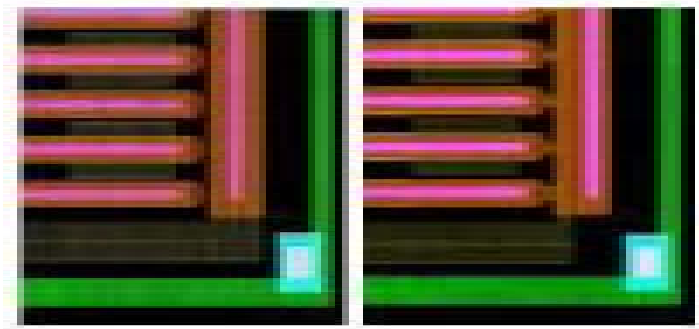


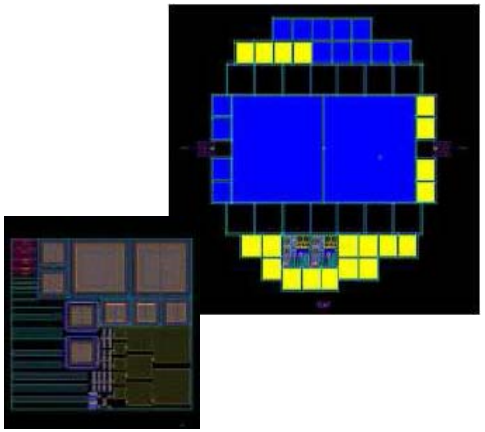


5 sensors specially treated for laser alignment

Sensors tested with detailed QA control (HEAPHY, IEKP)

NEW 2007: New technology approach: 3D planar (6") μstrip,
endless (hermetic),
low bias,
lower thickness,
faster,
rad. hard





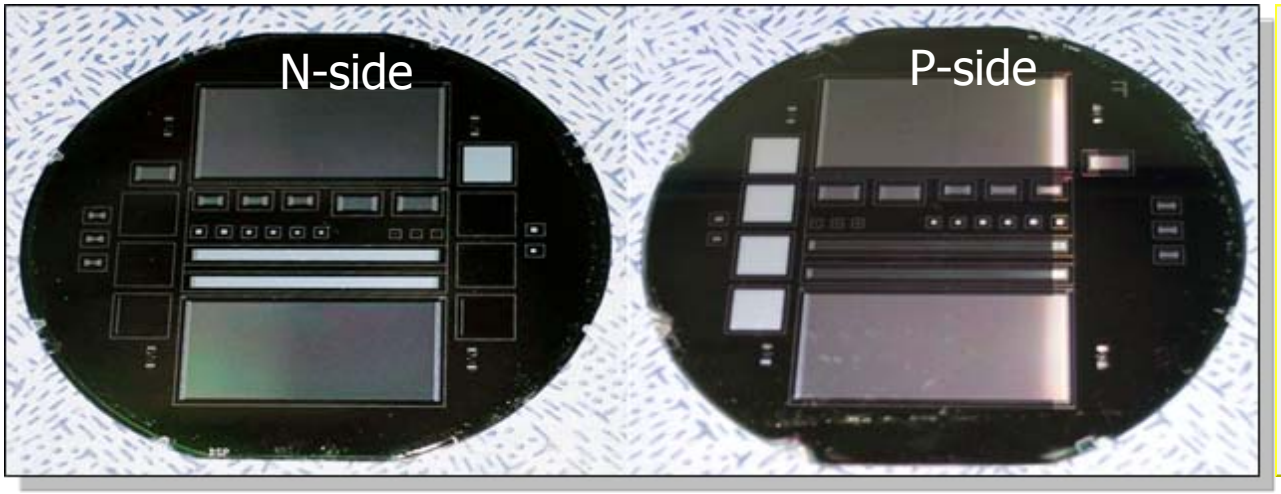
Test structures (not included this time)

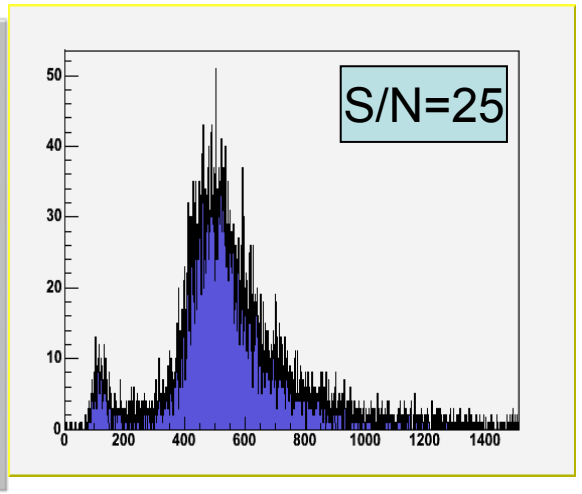
Si strip Sensors R&D at GLD (Korean team)

GLD Korean Team
Part of SiLC

DSSD Designed, Fabricated and Tested:
- IV/CV shows good quality sensor
- S/N shows that the sensors are in good shape
- more tests are in progress
- will fabricate AC-SSD on 6-inch(400 mm) and 8-inch(500 mm) wafers

Prototype





wafer	**TOPSIL (5inch, high resistivity, (100), FZ, DSP)**	**strip width**	**9μm**
		strip pitch	**50(100) μm**
thickness	**380 μm**	**readout pitch**	**50μm**
size	**51 x 26 mm²**	**readout channel**	**512(512)**

R&D on Sensors: Pixel Sensors

SiLC proposed since the beginning to use pixels in certain regions:

- ✓ Pixels for the very forward zone nearby the vertex detector
- ✓ Pixels in the overall internal region both central barrel and all very forward disks

  Not just an extension of the vertex region **but a new use of pixels (i.e. pixel sensors for large trackers (?))**

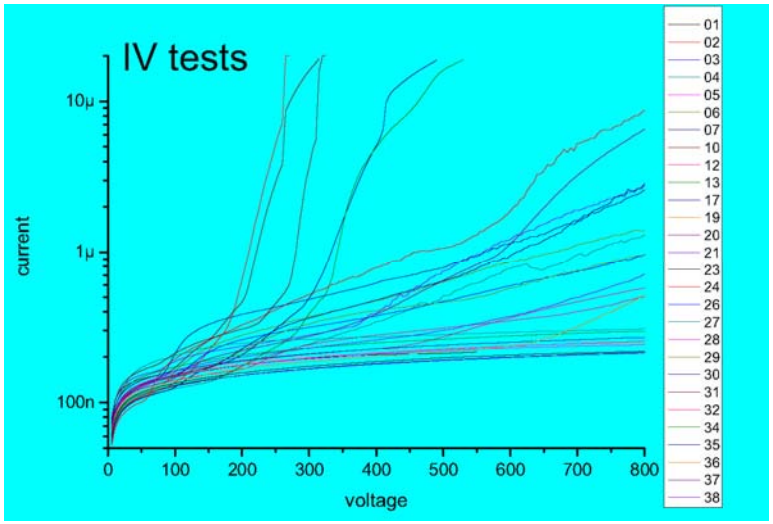
- ✓ Further on??? (i.e. an ‘’ all-pixel tracker’’)

The developments of pixel sensors are currently going within the microvertex R&D collaborations.

The main emphasis is on DEPFET,
SiLC collaborators also involve in this R&D activity - IFIC Valencia and CU Prague,
Growing interest on the 3D pixel technology, starting with expertise at CNM-IMB/CSIC and VTT; other teams are now joining.
The possible use of pixels is being taken into account as an important issue in optimization studies. This R&D aspect is expected to evolve in these next years.

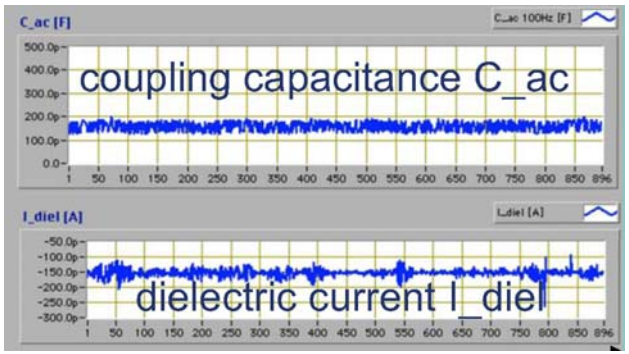
R&D on Sensors: Quality Control

Quality control of Sensors (IEKP and HEPHY, Mittarov talk)



Strip Scan Parameters

IV tested up to 800V ; Breakthroughs:
3 sensors below 450V, 1 below 300V
No pb. since operating voltage<100V



CV tests: requested a resistivity such that depletion voltage is between 50 and 100V;
All sensors fully deplete between 47-58V, average at 52.5V

R&D on Sensors: Connection to Industry

The Si Tracking activity implies developing close collaborative contacts with industrial facility, the collaboration between our 2 teams includes exchanging expertise and knowledge

✓ KEK side

Micron (DSSD strips)
Korean Si sensors
OKI (SOI)

✓ LPNHE side

HPK (new SSD & inline pitch adapter)
Korean Si sensors (new strips)
Canbera S.C(DSSD +novel Si tech)
Leti (?) (SOI)

Firms for new composite materials, cabling are also under investigation on both sides and expertise could be shared

R&D on Electronics

- ✓ DSM CMOS technology of FEE (going to 90 nm),
- ✓ Direct connection to the Silicon sensors (strip and pixel),
- ✓ Integration to the overal readout and DAQ

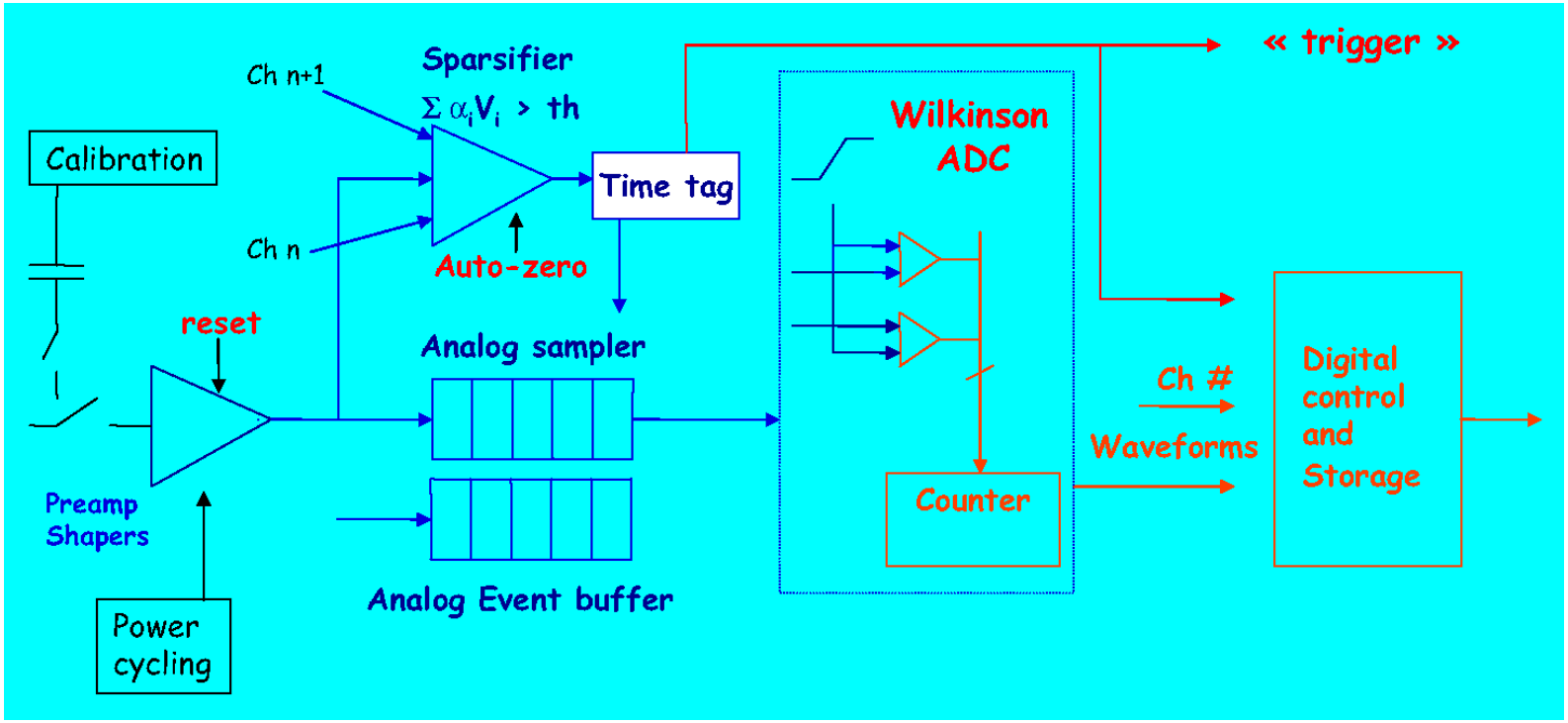
R&D on Electronics

Full readout chain integration in a single chip 512 or1024 on base 90 nm CMOS:

- ✓ Preamp-shaper - 30 mV/mip over 30 mip range,
- ✓ Shaper – two ranges: 500 ns – 1μs,
- ✓ Sparsification – threshold the on sum of 3-5 adjasted channels
- ✓ Sampling – 8samples at 80 ns sampling clock period, event buffer 8 deep,
- ✓ Noise baseline – measured with 180 nm CMOS: 375+10.5 e/pF @3 μs shaping, 210 μW power dissipation,
- ✓ On-chip digitalization – ADC10 bits,
- ✓ Buffering and digital preprocessing,
- ✓ Calibration and calibration management
- ✓ Power switching (ILC duty cycle) can save a factor up to 100

R&D on Electronics

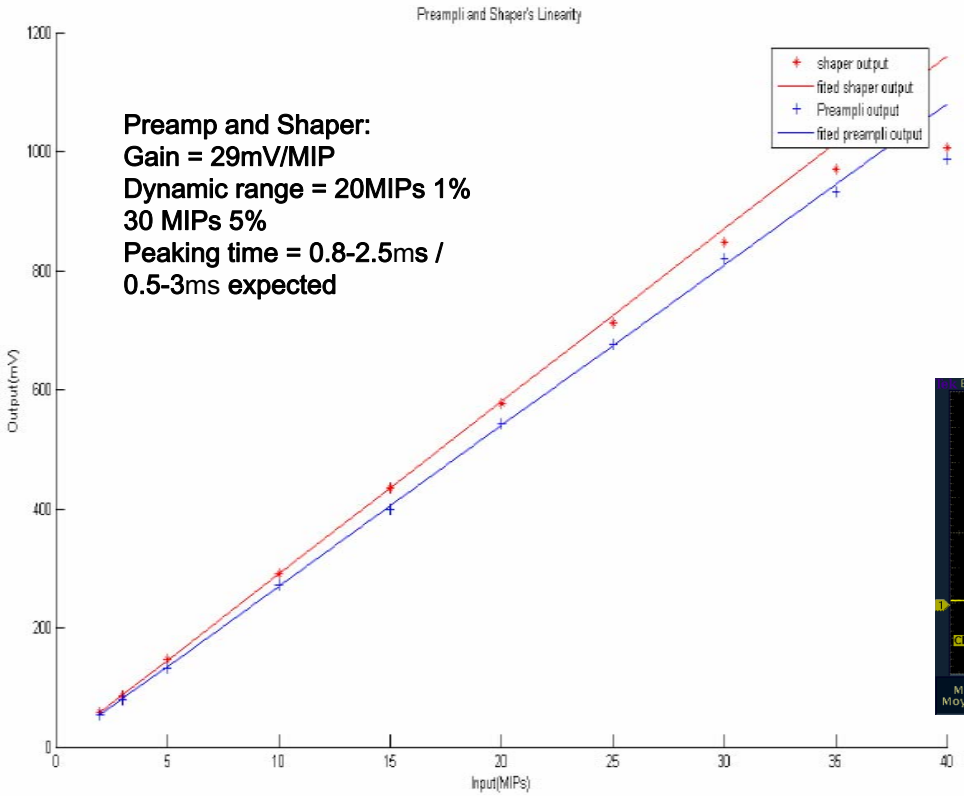
Front End Architecture



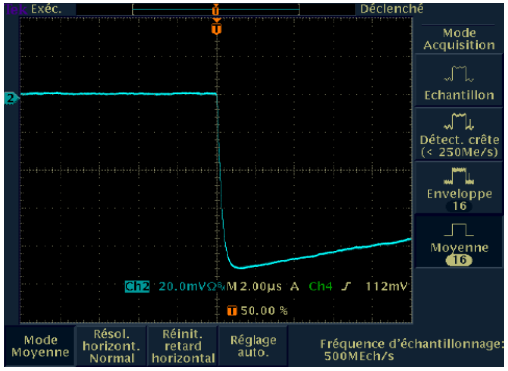
Full readout chain integration in a single chip 512 or1024 on base 90 nm CMOS

R&D on Electronics

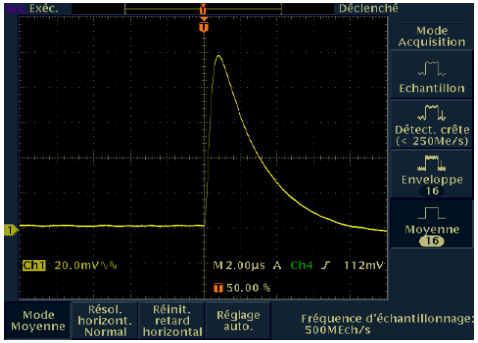
Preamplifier-Shaper Performance



Preamp and Shaper:
Gain = 29mV/MIP
Dynamic range = 20MIPs 1%
30 MIPs 5%
Peaking time = 0.8-2.5ms /
0.5-3ms expected



Preamp Output

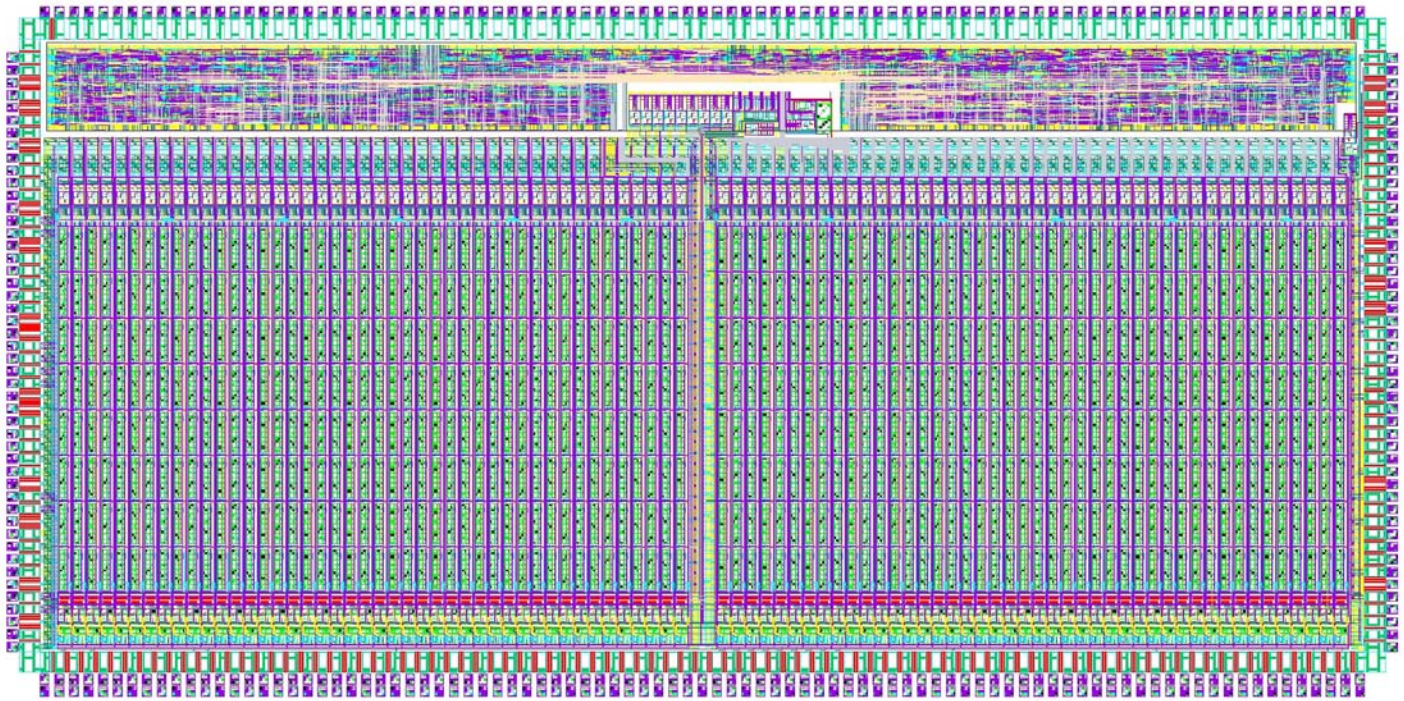


Shaper Output

SiTR_130-V1 successfully tested both at Lab test bench snd test beam (realistic conditions (see next)

R&D on Electronics

Just submitted (BU, LPNHE)



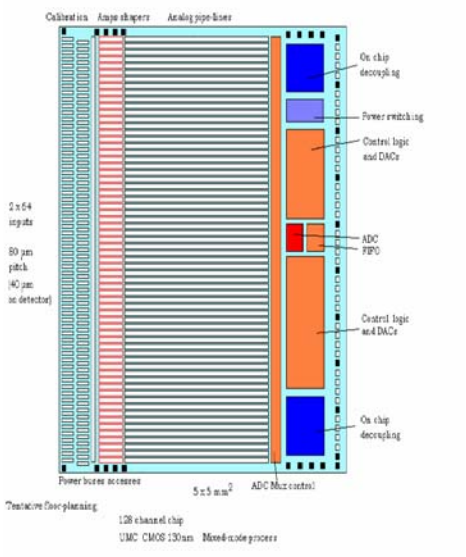
Sent to foundry, See DAQ session

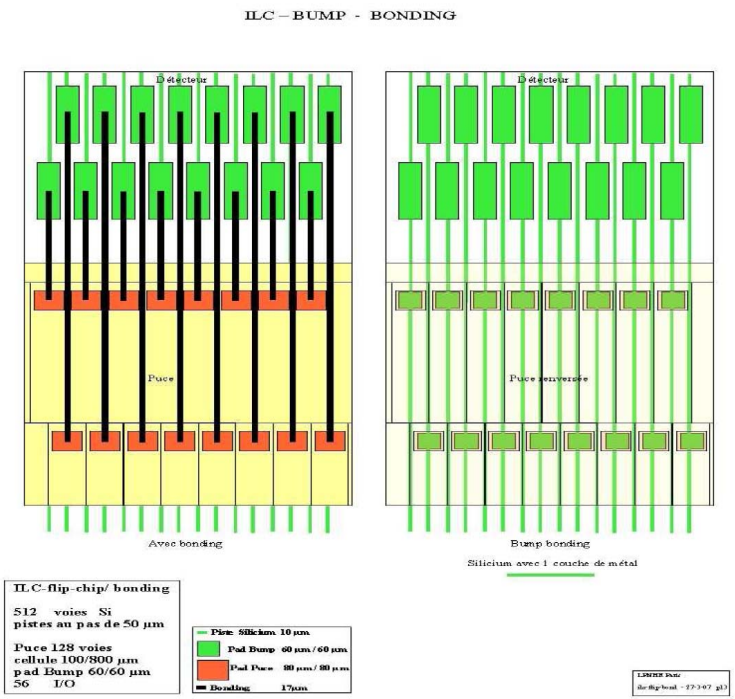
R&D on Electronics

Wiring FEE Chip onto μStrips –

goal: developing new routing and inline pitch technology for FE chip onto the strip.

First attempt: SiTR-130-96 chip on new HPK sensor





Decreasing %X0:

Chips directly routed onto μStrip by bomp bonding

Demonstration: 2008

Production: 2009

Simulation: Main Si Tracking components

✓ Inner components:

SIT/IT: link to VTX & TPC

improve the momentum resolution

FTD/FIT: extend/replace VTX & TPC at low angles (FWD)

✓ Outer components:

SET: link TPC to EM Calorimeter and helps in PFA

ETD/ET: same in the Endcap region

Moreover these 4 components provide an almost full angular coverage (also standalone tracking => redundancy)

Lot of work and studies devoted to emphasize these roles.

Simulation: Tools

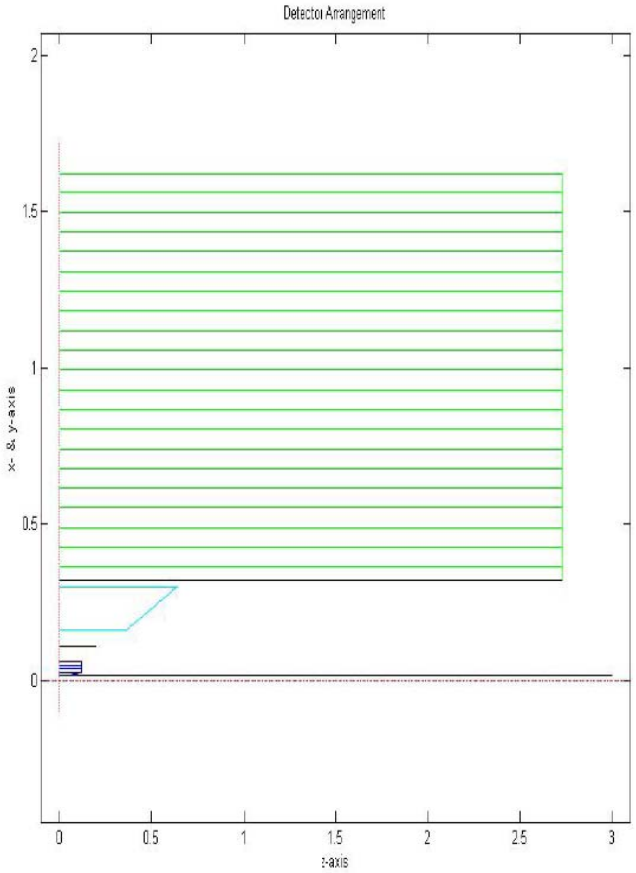
- ✓ Fast Simulations: LiC Toy, SGV
- ✓ Full simulations: GEANT4 based: MOKKA + Marlin Reco
  ILCROOT (for comparison)
- ✓ Test beams: Simulation and experimental prove of models

Main goals:

- ✓ Optimization of each component design in collaboration with each concerned subdetector(s)
- ✓ Study of the large angle and FWD region (connection with MDI and VFWD)
- ✓ Comparison with an all-Si-tracking design

Optimization Tools: Ex1 = LiC Toy

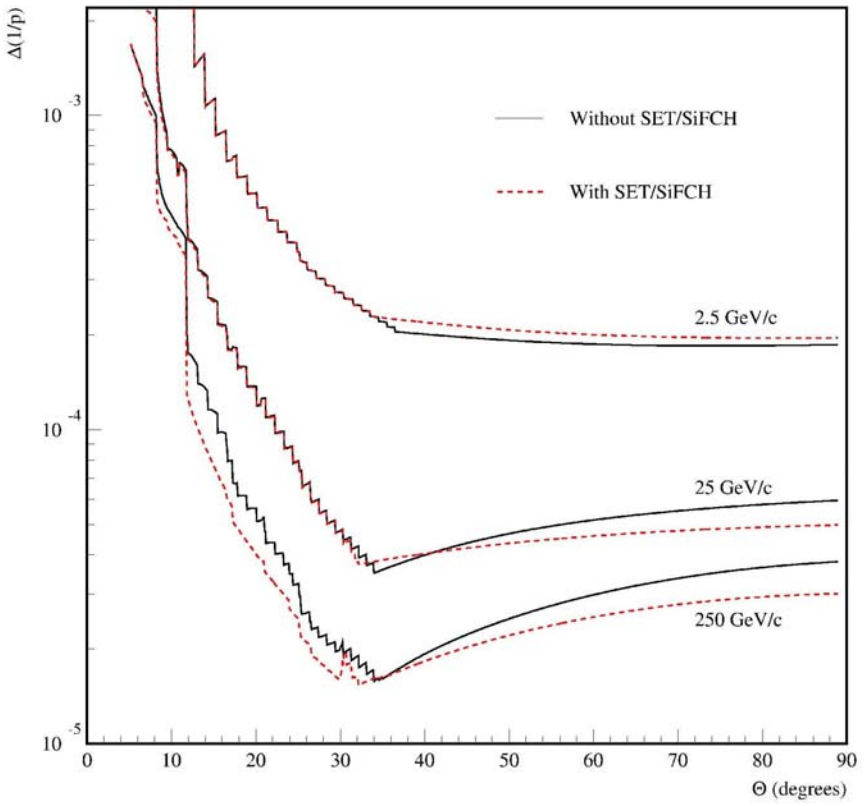
LiC Detector Toy, M. Regler, M. Valentan, R. Frühwirth, Vienna University: A mini simulation and track fit program, written in MATLAB, for fast and flexible detector optimization study.



RMS		$0 \le \lambda \le \pi/12$	$\pi/12 \le \lambda \le \pi/6$	$\pi/6 \le \lambda \le \pi/4$
$R\Phi$	without IT	$3.95\ 10^{-6}$	$3.99\ 10^{-6}$	$3.98\ 10^{-6}$
	with IT	$3.90\ 10^{-6}$	$3.98\ 10^{-6}$	$4.33\ 10^{-6}$
	modified IT	$3.81\ 10^{-6}$	$3.87\ 10^{-6}$	$4.26\ 10^{-6}$
z	without IT	$4.35\ 10^{-6}$	$4.65\ 10^{-6}$	$4.88\ 10^{-6}$
	with IT	$4.32\ 10^{-6}$	$4.02\ 10^{-6}$	$4.26\ 10^{-6}$
	modified IT	$4.27\ 10^{-6}$	$3.97\ 10^{-6}$	$4.12\ 10^{-6}$
ϑ	without IT	$1.50\ 10^{-4}$	$1.46\ 10^{-4}$	$1.17\ 10^{-4}$
	with IT	$1.19\ 10^{-4}$	$1.17\ 10^{-4}$	$1.00\ 10^{-4}$
	modified IT	$1.14\ 10^{-4}$	$1.15\ 10^{-4}$	$0.967\ 10^{-4}$
ϕ	without IT	$1.14\ 10^{-4}$	$1.19\ 10^{-4}$	$1.27\ 10^{-4}$
	with IT	$1.16\ 10^{-4}$	$1.21\ 10^{-4}$	$1.27\ 10^{-4}$
	modified IT	$1.10\ 10^{-4}$	$1.16\ 10^{-4}$	$1.22\ 10^{-4}$
$\Delta p_t/p_t$	without IT	$1.06\ 10^{-3}$	$1.08\ 10^{-3}$	$1.16\ 10^{-3}$
	with IT	$1.05\ 10^{-3}$	$1.02\ 10^{-3}$	$1.05\ 10^{-3}$
	modified IT	$1.05\ 10^{-3}$	$1.03\ 10^{-3}$	$1.05\ 10^{-3}$
$\Delta p_t/p_t^2$	without IT	$1.02\ 10^{-4}$	$1.01\ 10^{-4}$	$1.14\ 10^{-4}$
	with IT	$0.927\ 10^{-4}$	$0.921\ 10^{-4}$	$0.977\ 10^{-4}$
	modified IT	$0.942\ 10^{-4}$	$0.931\ 10^{-4}$	$0.998\ 10^{-4}$

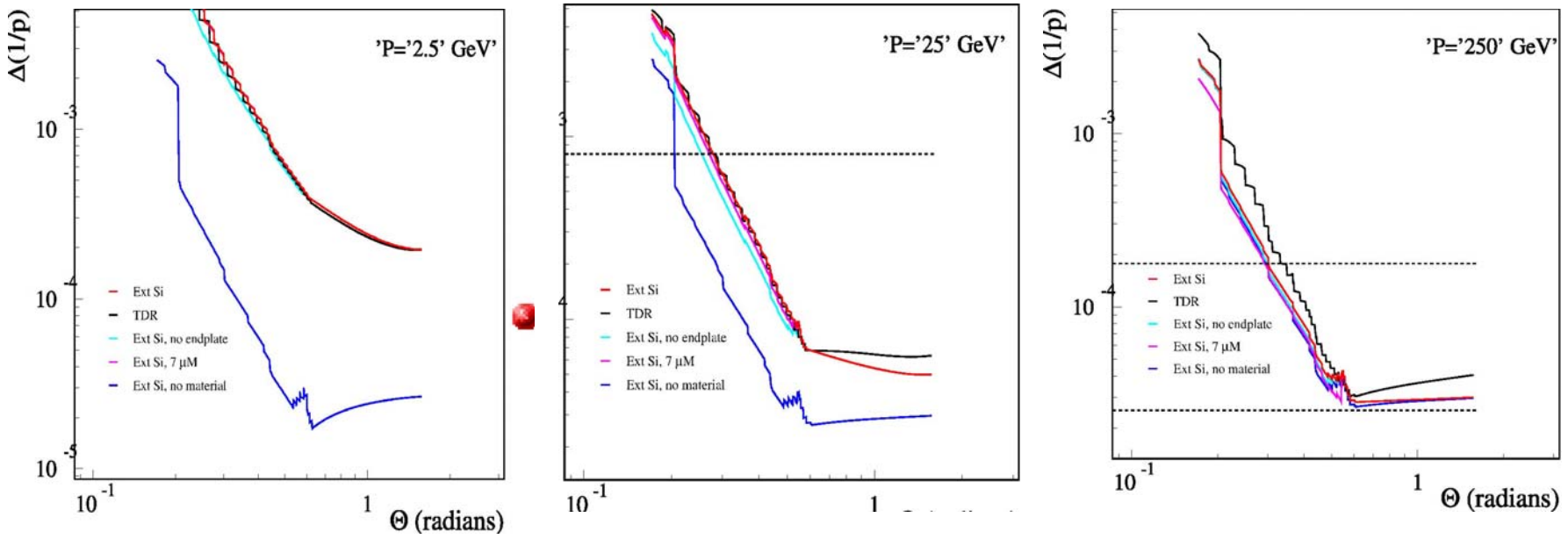
Optimization (SGV) M. Berggren

SGV studies have helped to define the optimal geometry of SET, and to show how the Silicon Envelope can ameliorate the momentum resolution for the LDC detector:

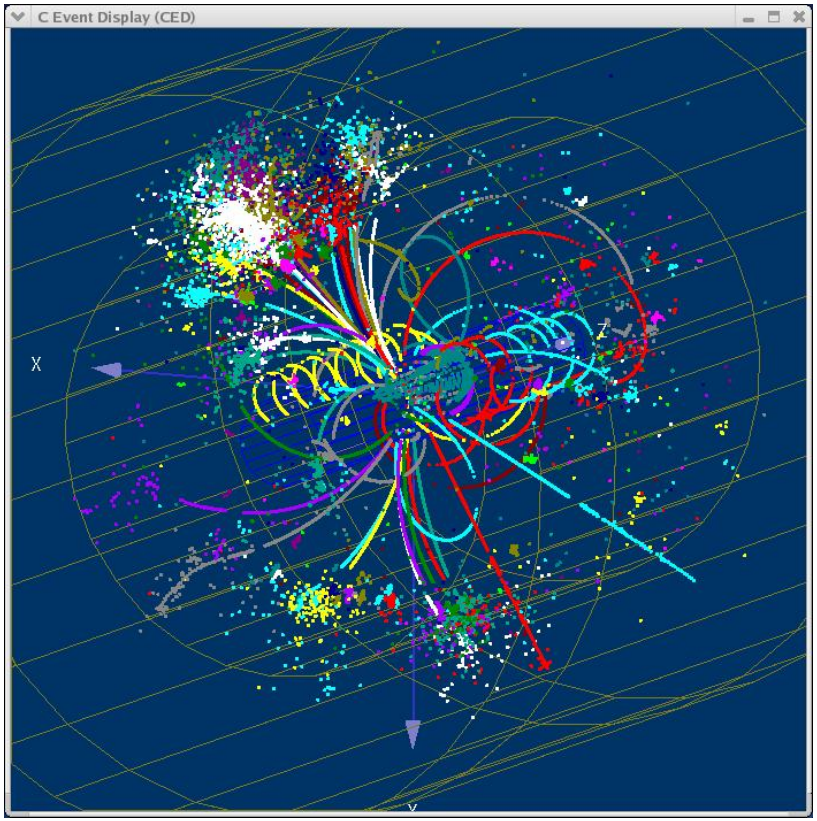


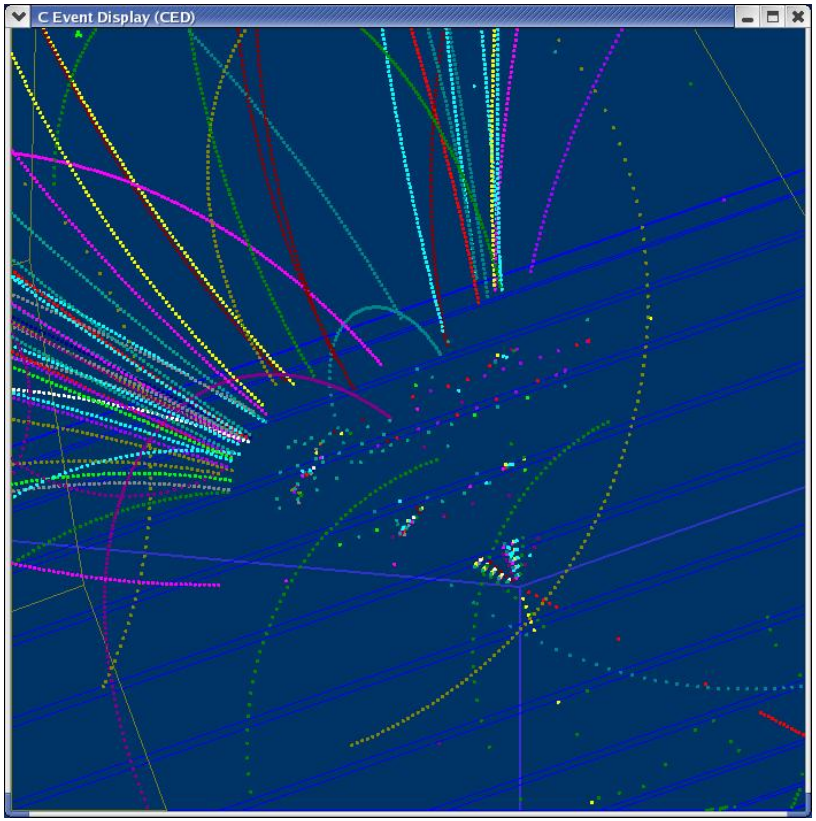
Optimization (SGV)

Given the effect performance curves wrt. Angle and Momentum, it is interesting to try to see what the ultimate performance for a given geometry would be.
With SGV, it is easy to change the material, and even to completely remove it (but keeping the measurement...)



Full Simulation: Example of importance





Importance of the SIT component

Optimization: SiLC Tracking Components

Common Effort:

Start the mass production of the Monte Carlo data for the Detector optimization and Physics Analysis,

Status:

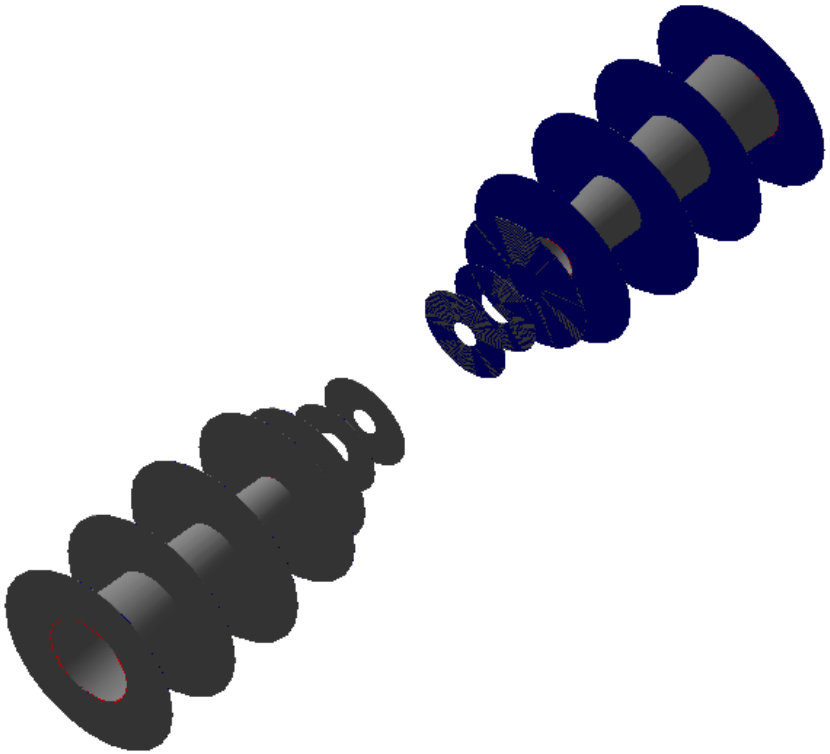
Provided all components of the SiLC Silicon Tracking Systems to Mokka Simulation Framework

Optimization: FTD Geometry

FTD: 7 Disks

First 3 pixel technology Si thickness 50 microns + Carbon Fiber support thickness 1 mm ,

Last 4 are general Si thickness 275 microns + Carbon Fiber Support 1 mm



Database ftd04 - table disk

Showing records 0 - 7 (7 total)

Show : 30 rows starting from 0 Full Texts

disk_number	z_position	inner_radious	outer_radious
1	220	29	140
2	350	32	140
3	500	35	210
4	850	51	270
5	1200	72	290
6	1550	93	290
7	1900	113	290

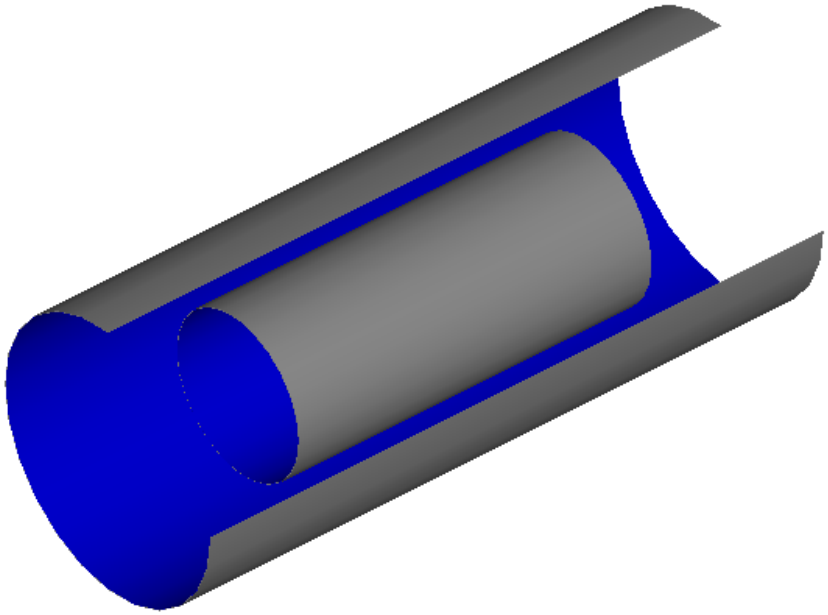
Show : 30 rows starting from 0 Full Texts

Insert new row

id	Si_thickness	Si_thickness_2	inner_support_thickness	inner_support_length	outer_support_thickness	outer_support_length	outer_cylinder_total_thichness	cables_thichness
0	0.05	0.275	1	4	2	4	1	0.08

Optimization: SIT Geometry

SIT: 2 barrel detectors Si thickness 275 mk + Carbon Fiber Support - thickness 1mm



Database sit02 - table sit

Showing records 0 - 2 (2 total)

Show : 30 rows starting from 0 Full Texts

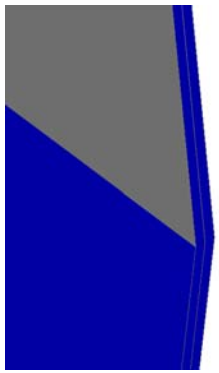
layer_id	inner_radious	half_z	sensitive_thickness	support_thickness
1	160	380	0.275	1
2	270	660	0.275	1

Show : 30 rows starting from 0 Full Texts

Insert new row

Optimization: ETD Geometry

ETD: 3 disks, XUV plane, Si thickness 275 microns + Carbon Fibers Support 1 mm,



Database etd01 - table ETD

Showing records 0 - 3 (3 total)

Show : 30 rows starting from 0 Full Texts

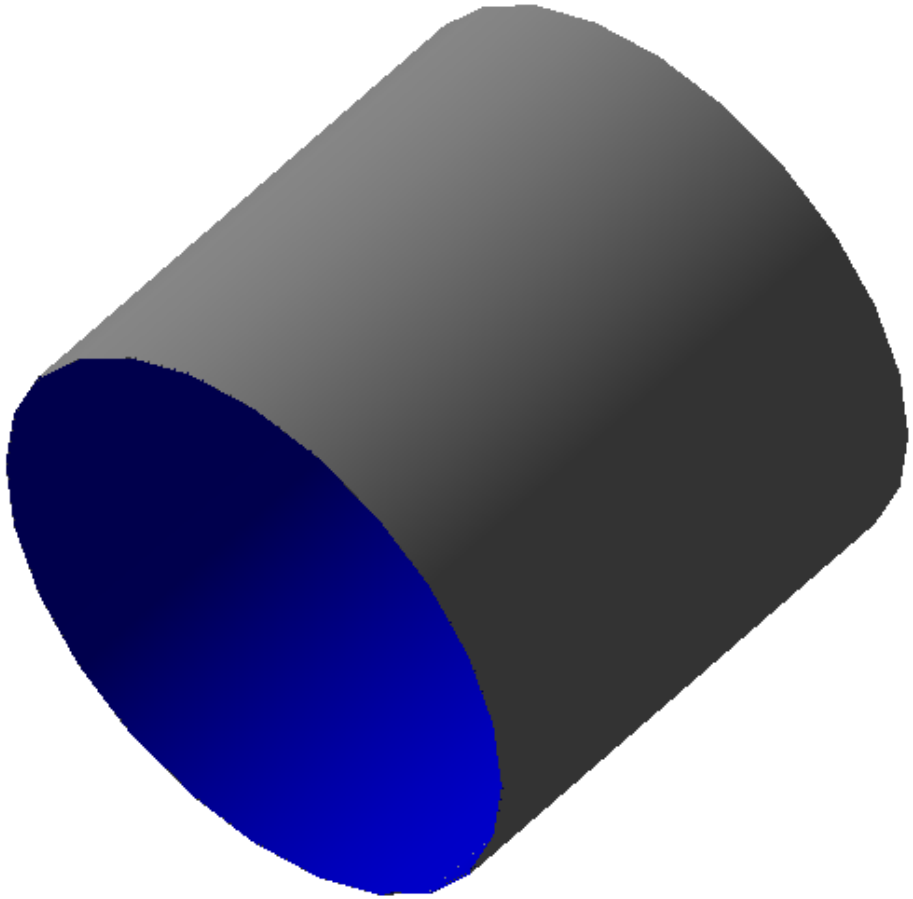
layer_id	inner_radious	half_z	sensitive_thickness	support_thickness
1	305	2368	0.275	1
2	305	2368	0.275	1
3	305	2368	0.275	1

Show : 30 rows starting from 0 Full Texts

Insert new row

Optimization: SET Geometry

SET: 2 barrel detectors Si thickness 275 microns + Carbon Fiber Support 1 mm



Database SET01 - table EST

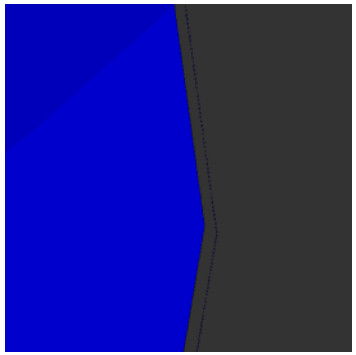
Showing records 0 - 2 (2 total)

Show : 30 rows starting from 0 Full Texts

layer_id	inner_radious	half_z	sensitive_thickness	support_thickness
1	1592.5	1500	0.275	1
2	1587.5	1500	0.275	1

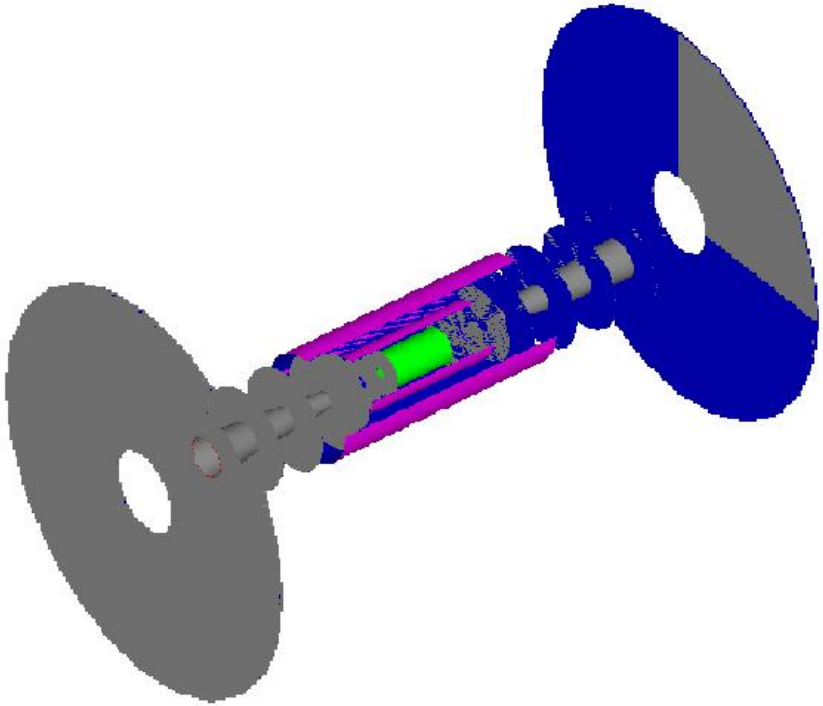
Show : 30 rows starting from 0 Full Texts

Insert new row



Optimization: Geometry

Assembled VXD, SIT, FTD, ETD:



Next step is implementation more realistic geomertry to get the connection to realistic digitalization

Simulation: Test Beam

Simulation of the Test Beam Setup is prepared for Mokka Framework with full Digitalization (Z.Drazal)

Optimization Tools: Track Fitting

Track Fitting (Marcel Vos) : CMS Kalman filter tool-kit .

The result of years of work by a lot of people. Validated in large-scale MC productions.

Extracted all relevant code in a series of libraries with limited external dependencies (CLHEP, ROOT).

Interfaced to toy geometries in standalone programme. Tested results for internal consistency and against existing fast-simulation packages.

Interfaced to MarlinReco (GEAR geometry, LCIO hits)

Optimization: Momentum resolution

$\Delta(1/p_T)$ @ 10 degrees :

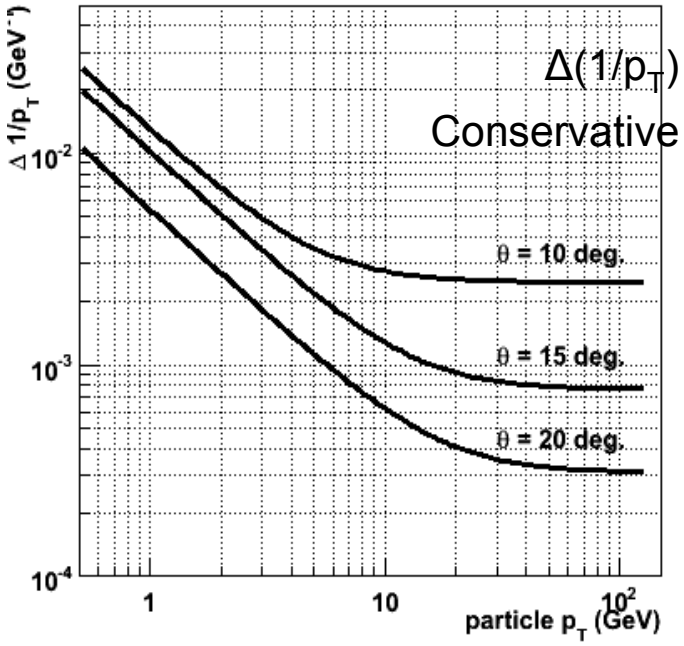
Reference (TESLA) set-up

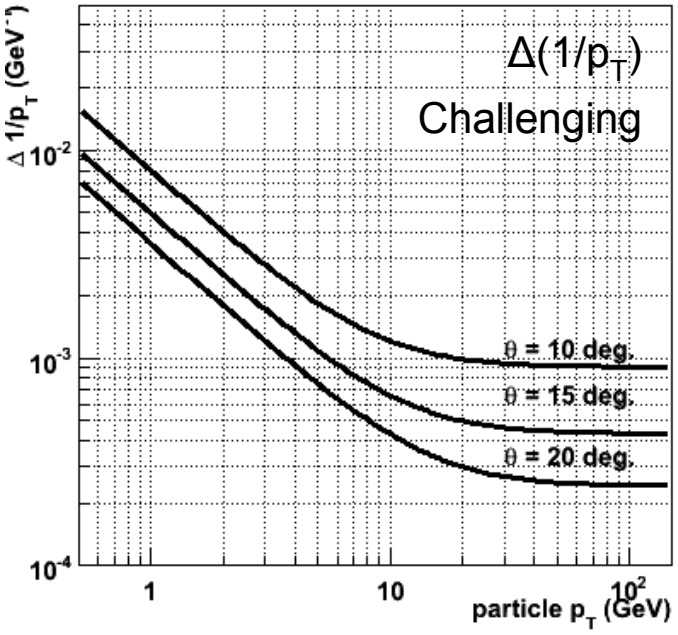
$1.8\times10^{-3}\oplus1.3\times10^{-2}/\ p_T$

Challenging setup

(5 μ m Rφ resolution, 1.2 ‰ X0/disk for FTD1-3, 4 ‰ X0/disk for FTD4-7)

$\Delta(1/p_T)=0.9\times10^{-3}\oplus0.8\times10^{-2}/\ p_T$





Optimization Tools: Pattern Recognition

Combinatorial algorithm based on KF kit

The baseline algorithm of the ATLAS (arXiv:0707:3071) and CMS (NIM A 559 143) experiments

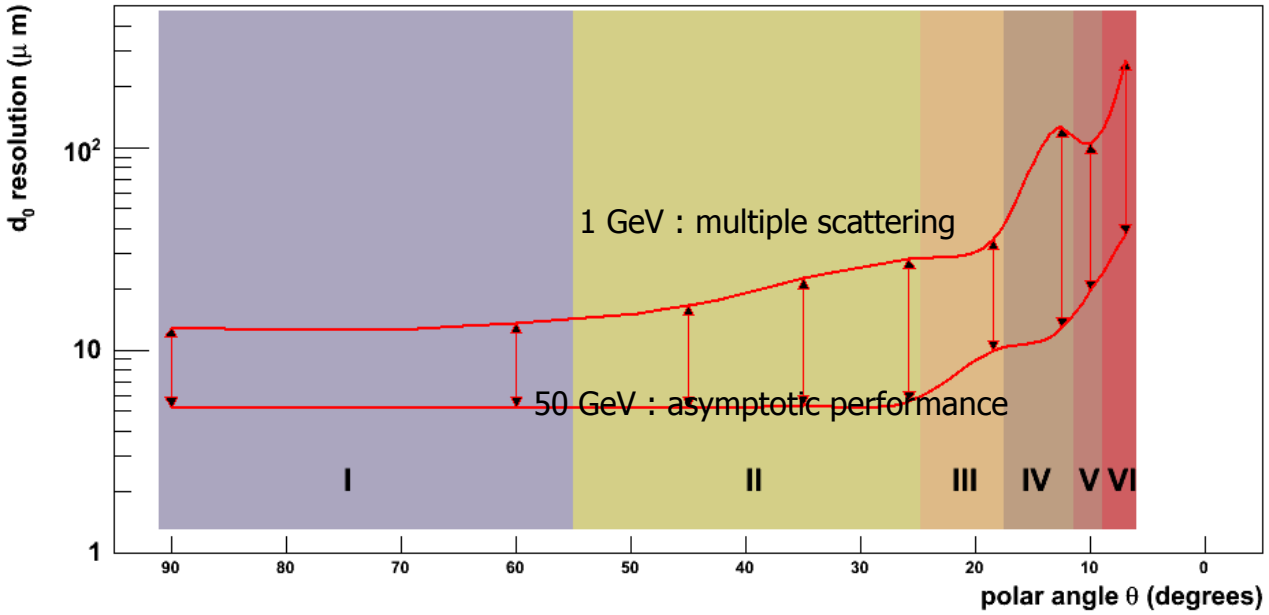
Standalone FTD reconstruction implemented in MarlinReco processor

Run on tt events with superposed pair background.

- Reference FTD (TESLA layout)
- 10 mm R-f resolution
- 1.2 % X_0/disk (1-3) and 0.8 % X_0/disk (4-7).
- Several scenarios for R-resolution, from pixel to single-sided strip.

Optimization: Vertexing with Forward Tracking

* I	35	< θ <	90	5 VXD + SIT
* II	25.8	< θ <	35	5 VXD + FTD1
* III	18.5	< θ <	25.8	3 VXD + FTD1+2
* IV	12.5	< θ <	18.5	VXD2 + FTD
* V	10	< θ <	12.5	FTD1,...
* VI	6.5	< θ <	10.0	FTD2,...



Mechanics related issues

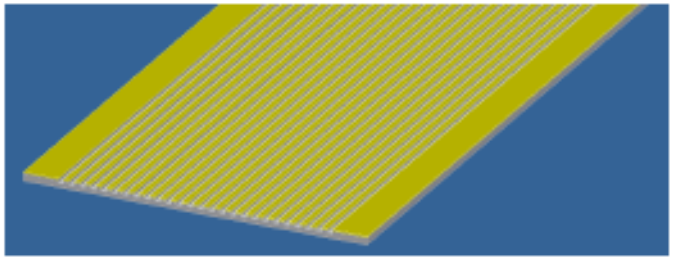
Mechanics play a central role also in lowering the material budget.
Among the main topics of common interest:

- ✓ New composite materials to build the mechanical structures
- ✓ Alignment
- ✓ Cooling

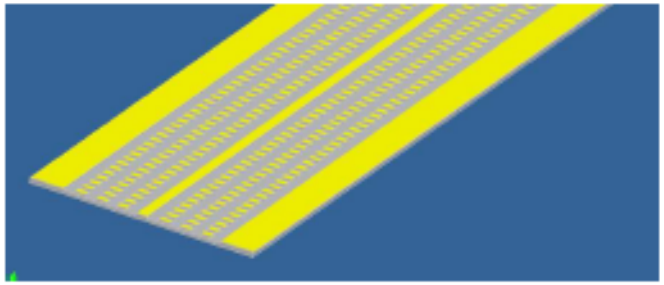
Mechanics: COOLING

- Single thin channel
- Double thin channel/reticule fin
- Multiple minichannel

Parallel minichannel

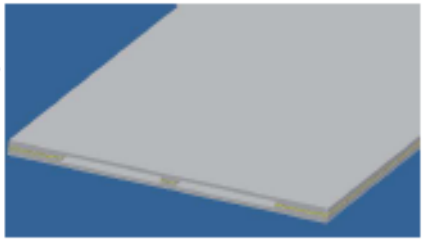


Double thin minichannel with reticule

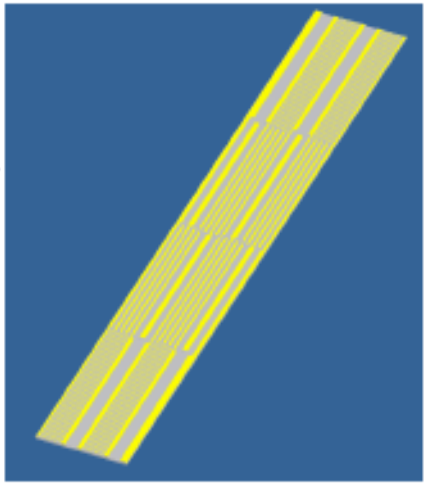


Single thin minichannel

Double thin minichannel

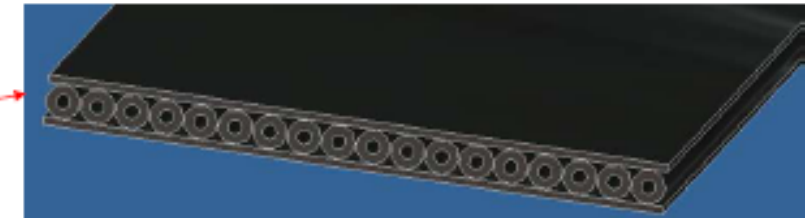


Trees thin minichannel



F.Bosi , M.Massa, SiLC Workshop, Torino, December 17th 2007

General scheme of the additive technique support .



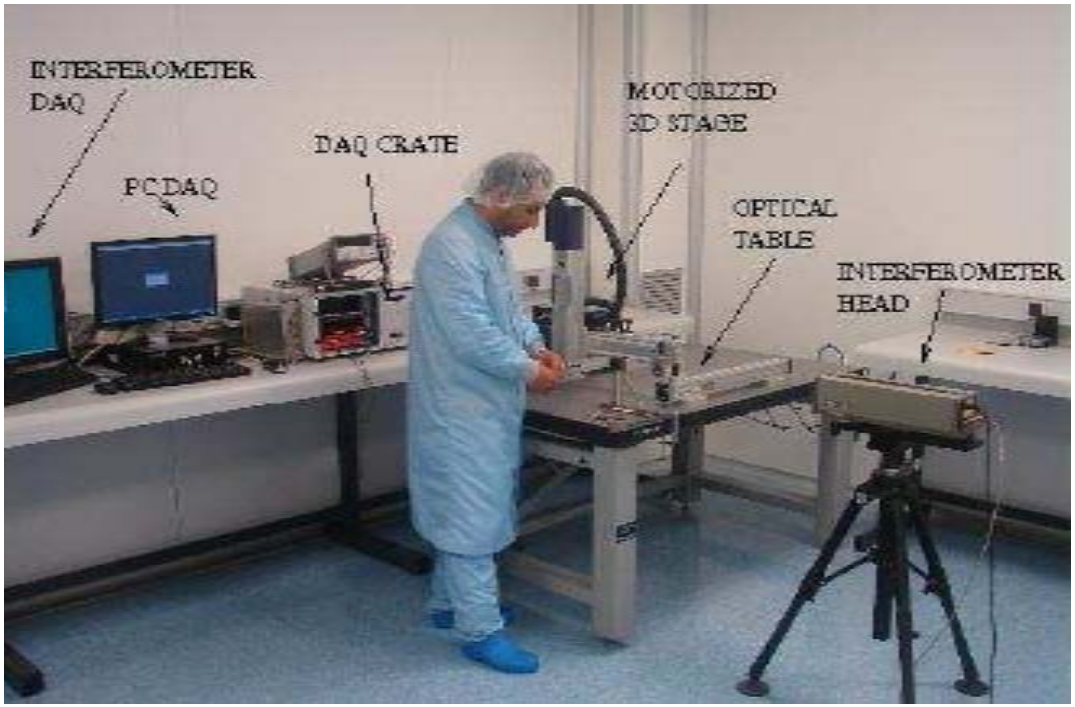
By courtesy of F. Bosi

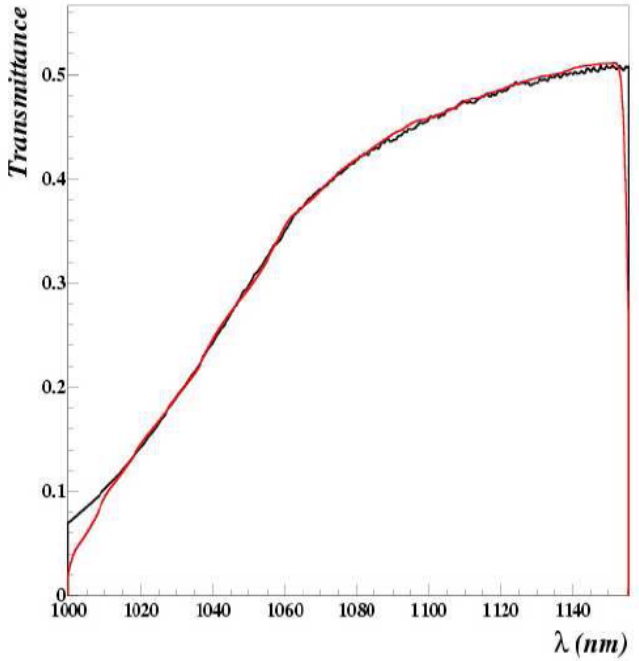
Test Facilities

- ✓ Test Benches:QT sensors, multiporpose, alignment
- ✓ Beam Test

Test Facilities: Alignment

Alignment Test Bench (see M.Fernandez talk)

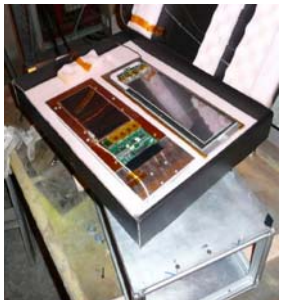




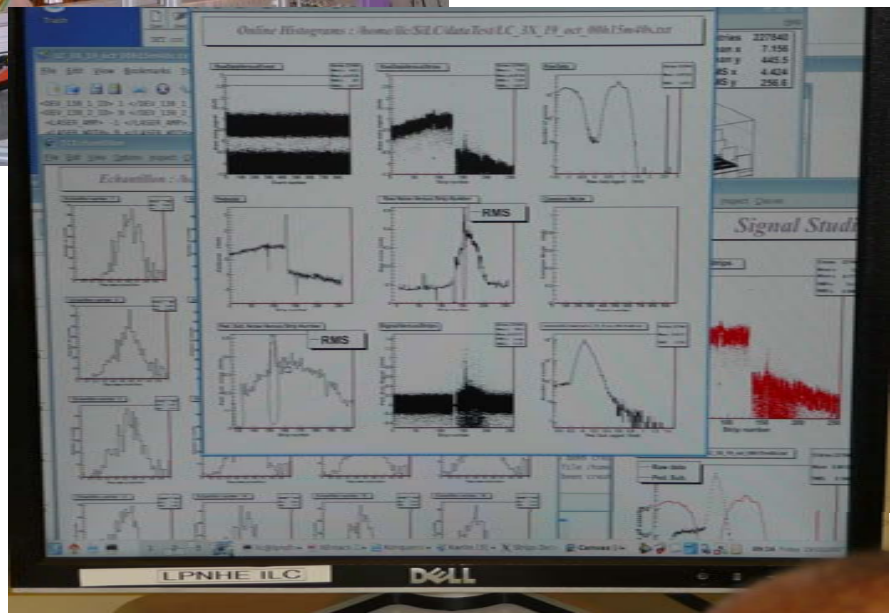
Precise test setup and good agreement with Optic simulations

Test Facilities: DESY Test Beam

Beam test preparation

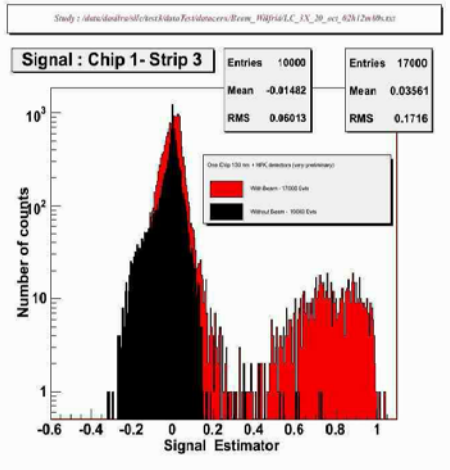


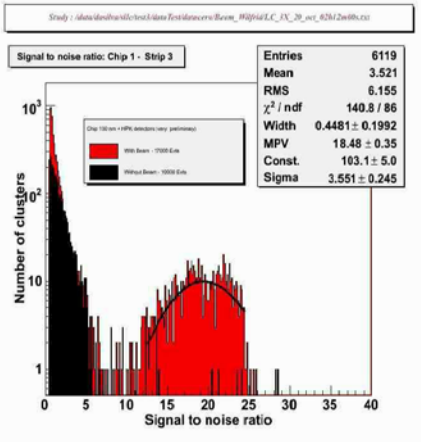
Test Facilities: DESY Test Beam

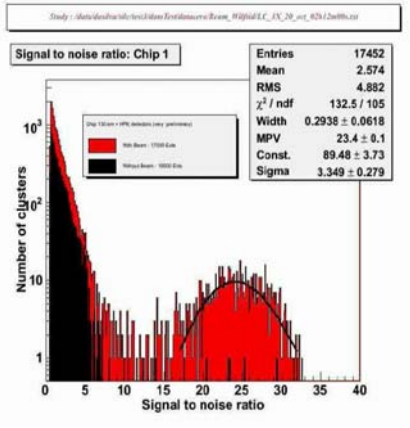


Test: Results

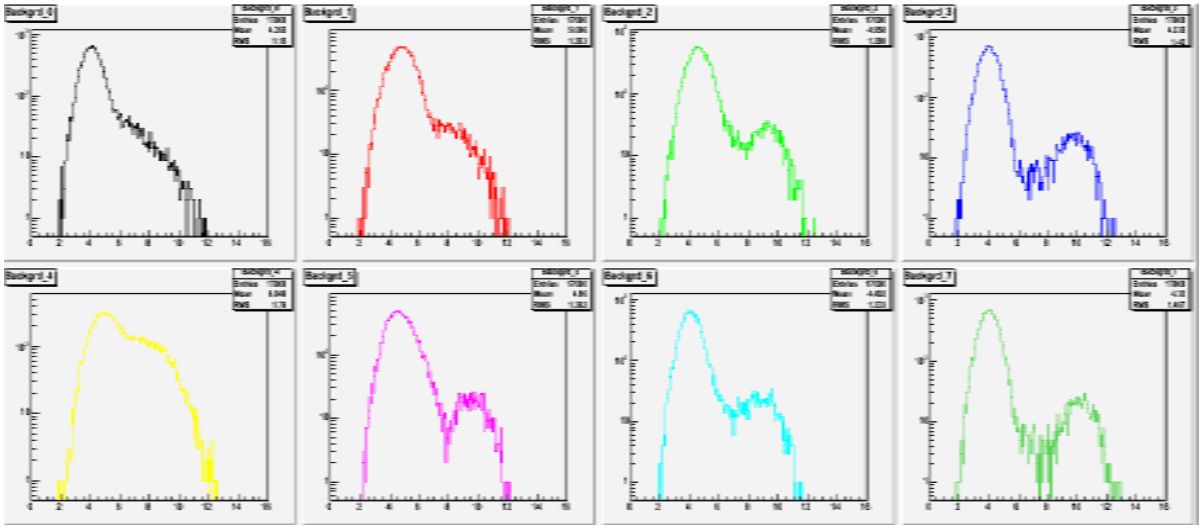
Black – No beam, red beam on, S/N ratio 18-24





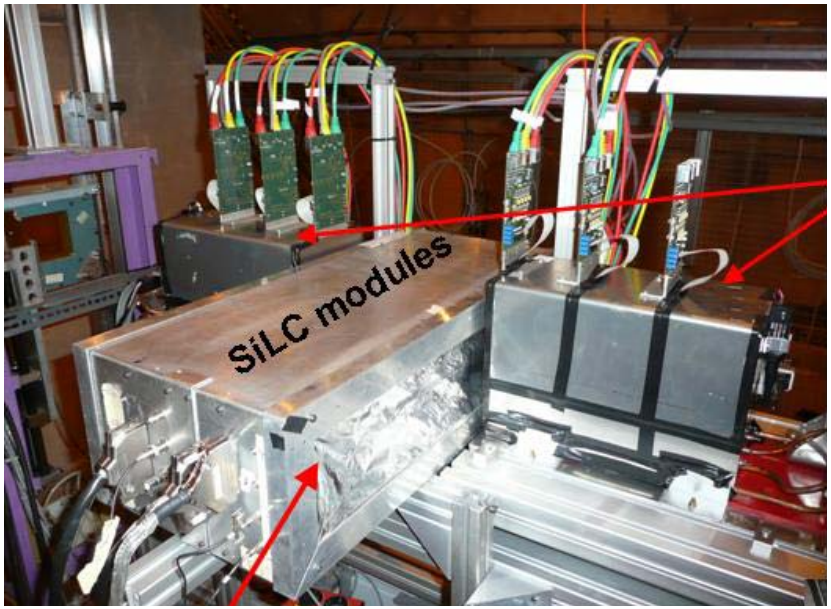


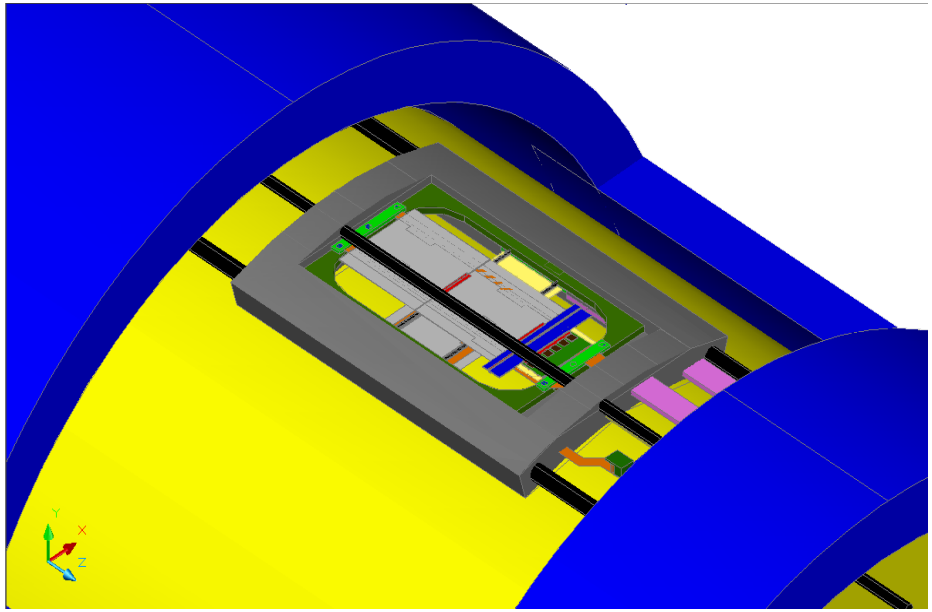
Strip length 18.5 cm



Optimization Tools: Beam Test

- ✓Test beam at CERN Oct 2008:
- ✓Combined Si strips with EUDET Telescope.





LCTPC in 2008:
test SIT/SET system
around the TPC

What's next …

SiLC is a transversal R&D activity:

- ✓ It intend play a major role, not only on development of novel technologies needed to overcome the challenges ahead of us for constructing large area tracking systems,
- ✓ Also study and compare the tracking alternatives proosed for the ILC with a joint optimizatiom task forse,
- ✓ At SiLC08, representatives from 3 proposed ILC concepts decided to collaborate with a joint simulation and optimization study, sharing tools and expertize,
- ✓ Same for combined beam test, especially at FNAL 2009.
- ✓ SiLC intends also further exploit synergy/collaboration with other machines and HEP domains, especially LHC and its upgrades.
- ✓ SiLC is following workplan and millestones as anticipated even on more challenging topics.

SiLC R&D Collaboration

U.S.A

Michigan U.
SCIPP-UCSC

Close connections:

- FNAL (DOE prop 05 funded)UCSC, FNAL, LPNHE
- SLAC (DOE prop 03: funded): UCSC, SLAC Michigan U, LPNHE and meetings SiD
- CERN (developed interest)

Europe

IMB-CNM/CSIC, Barcelona (SP) *(eudet ass.)*
Uni of Barcelona (SP)
Helsinki U. and VTT (Fi) *(eudet)*
IEKP, Karlsruhe U. (D)
Uni of Liverpool, (UK)
Moscow St. U. , Moscou(Ru) *(eudet ass.)*
Obninsk St. U., Obninsk (Ru) *(eudet ass.)*
LPNHE, Paris (Fr) *(eudet)*
Charles U. , Prague (CZ) *(eudet)*
IFCA, Santander(Sp) *(eudet)*
Torino U., Torino -INFN(IT)
IFIC-CSIC Valencia (Sp) *(eudet ass.)*
HEPHY, Academy Sci., Vienna (Au)

Asia

Kyungpook U. Taegu, Ko
Yonsei U., Seoul, Ko
Korea U. Seoul, Ko
Seoul Nat. U., Seoul, Ko
SungKyunKwan U. Seoul
Tokyo U. (Japan)
HAMAMATSU (Japan)

SITRA= sub sample of SiLC but many SiLC partners Are joining tests beam and related isues (EUDET}

Launched January 2002, Proposal to the PRC May 2003, Report Status May 2005, ILC tracking R&D Panel at BILCW07 February 2007, next PRC Status report April 08

The optimization of the Silicon tracking for ILD will be pursued within our ongoing Collaboration with Silicon tracking team als part of SiLC