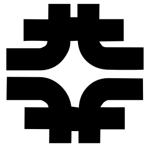
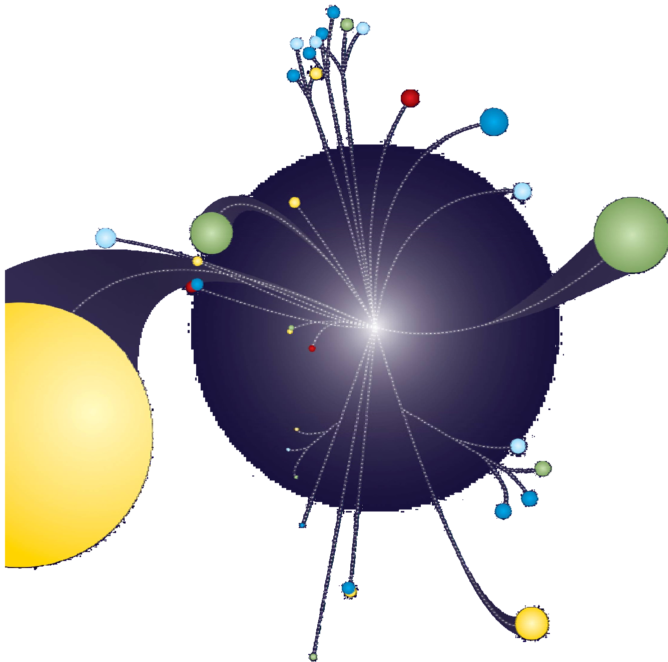


R&D on Pixel Detectors at Fermilab

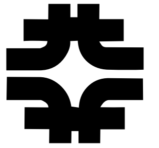


Marcel Demarteau

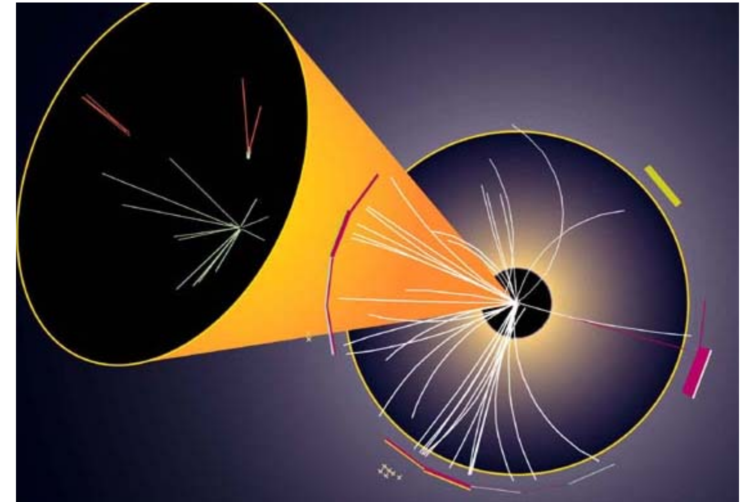
For the Fermilab Detector & Physics R&D Group

ECFA Workshop
June 9-12, 2008 – Warsaw

The Next Generation Detectors

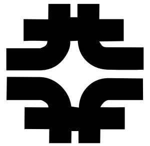


- The next generation detectors will emphasize precision
  - Collider experiments:
    results from the LHC will be the guide
  - Fixed target experiments:
    deep probes of (possible deviations of) the Standard Model
- Precision detectors fully reconstruct the final state over the full angular region
- Their performance is required to go about one order of magnitude beyond what has been achieved to date



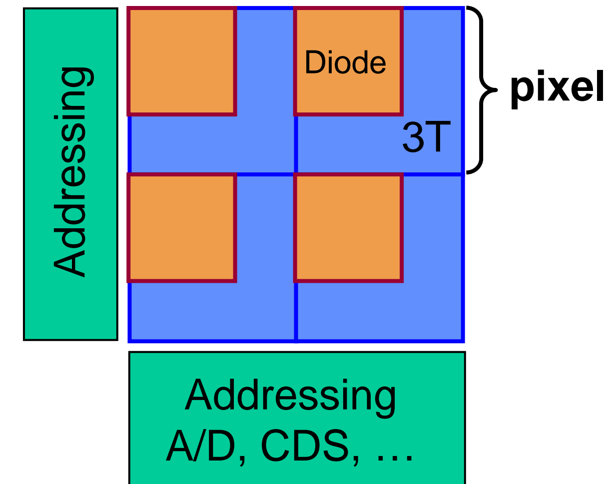
- Strategy:
  - Maximize integration of functionality
    - Maximize front-end processing power with minimal power requirements
    - Integration of particle detector with front-end readout
    - Maximize performance and minimize mass
  - We pursue those technologies that we believe are the most promising, despite (or because of) the fact that some seem very challenging
    - 3D vertical integration
    - Silicon on Insulator

Vertical Integrated Circuits – 3D

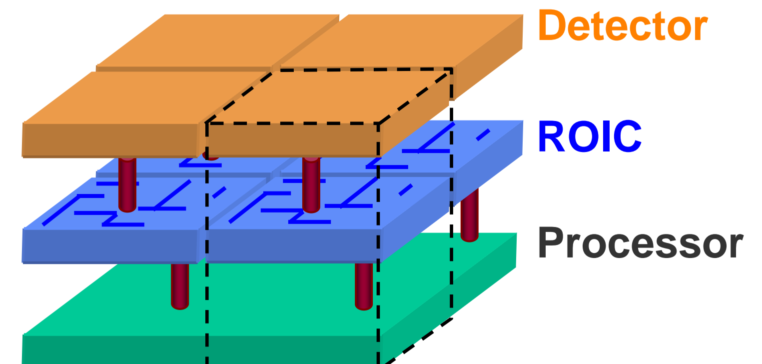


- "Conventional MAPS"
  - Pixel electronics and detectors share area
  - Fill factor loss
  - Co-optimized fabrication
  - Control and support electronics placed outside of imaging area
- 3D Vertical Integrated System
  - Fully active sensor area
  - Independent control of substrate materials for each of the tiers
  - Fabrication optimized by layer function
  - Local data processing
  - Increased circuit density due to multiple tiers of electronics
  - 4-side abuttable
- Technology driven by industry
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power, crosstalk

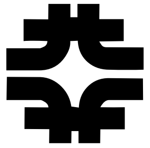
Conventional MAPS



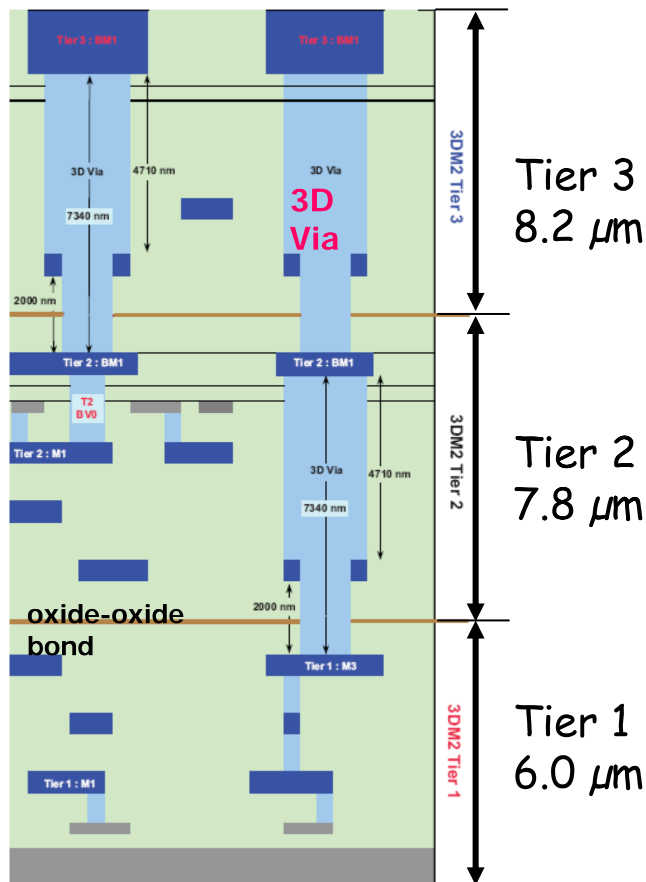
3-D Pixel

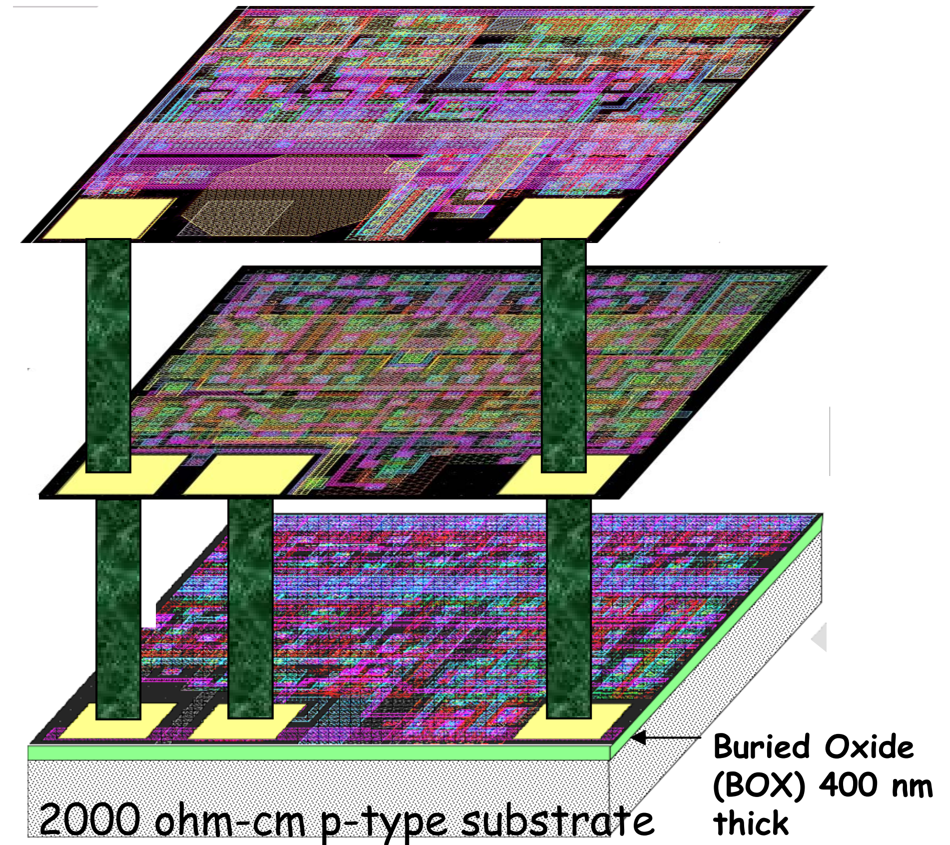


VIP Chip

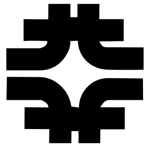


- **3D chip Vertical Integrated Pixel (VIP) chip submitted by Fermilab to DARPA funded MIT-LL 0.15 μm 3D SOI process on Oct. 15, 2006**
  - **Chips received back early 2008; key features:**
    - Analog pulse height, sparse readout, high resolution time stamp, front-end power ~ 1875 μW/mm^2 (before cycling), 175 transistors in 20x20 μm^2 pixel



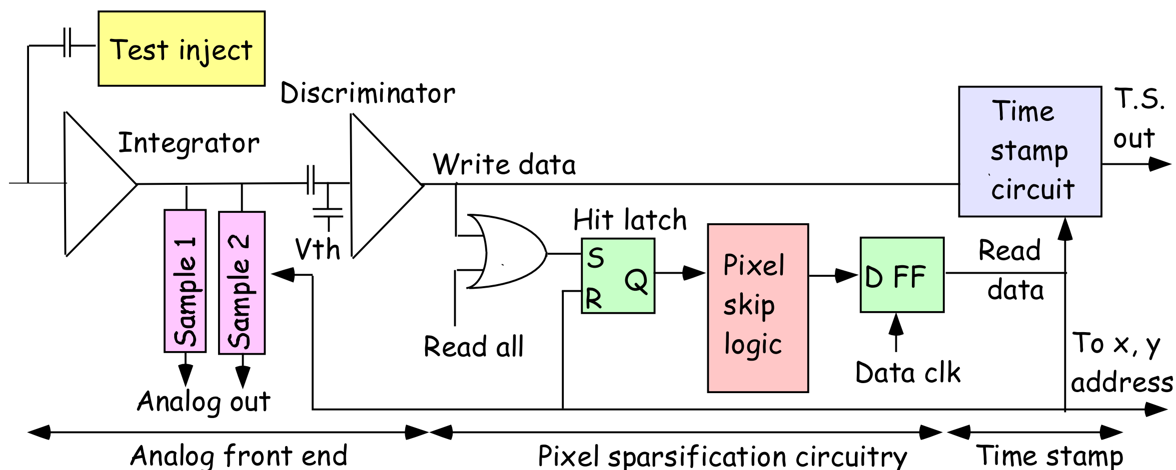


Architecture of Demonstrator Chip



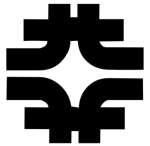
- Design:
  - Analog and binary readout information
  - Time stamping of pixel hit for ILC environment
    - Divide bunch train into 32 (5 bit) time slices
  - Sparsification to reduce data rate
    - Use token passing scheme with look-ahead to reduce data output
      - During acquisition, a hit sets a latch
      - Sparse readout performed row by row with x- and y-address stored at end of row and column
  - Chip divided into 3 tiers
    - Design for 1000 x 1000 array but layout only for 64 x 64 array.
  - Chip received Nov. 20, 2007

- First design which, on paper, meets 'all' of the ILC requirements for thickness, resolution, power dissipation, time stamping
  - Power is 0.75 microwatt/pixel ~ 18.75 microwatts/mm² (after pulsing)
  - Noise is ~30-40 e⁻
  - S/N = 100-200:1

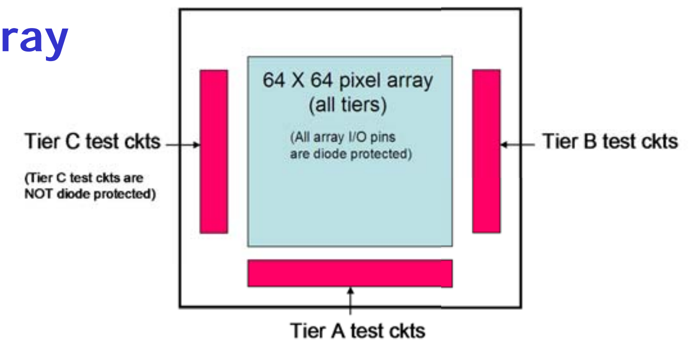


Schematic pixel cell block diagram

VIP Test Results



- Received ~6 functioning chips
- Chip is divided into test structures and 64 x 64 array

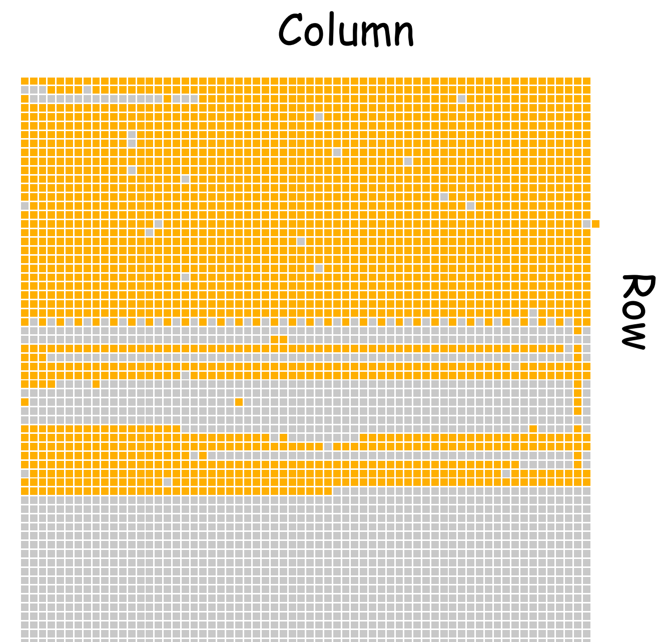


- Test structure results for individual tiers
  - Chip does not operate at nominal voltages
  - Ramp circuit jitter from chip to chip
  - Some parts work on some chips
  - Noise causes jitter in ramp timing
  - Performance is a little faster than simulations on some tiers

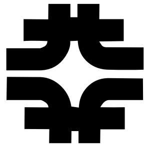
- Full array tests
  - Digital test results
    - Serial readout for address partially working on some
  - Analog test results
    - Analog pedestals measured for full array

Read_all_cells, all 4096 pixels addresses should be generated and read out …

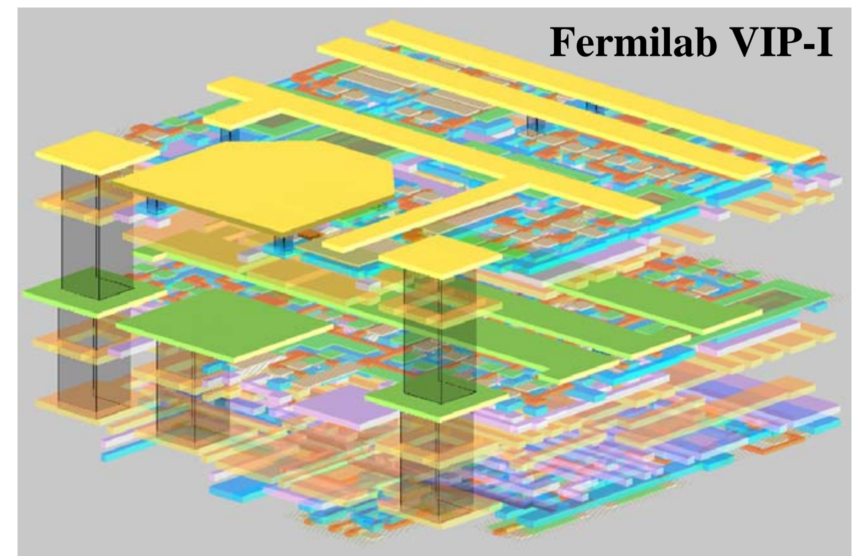
Last week able to readout all cells!



Next Steps with MIT-LL

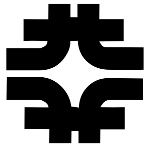


- MIT-LL VIP process has some shortcomings
  - Processing problems
    - Trapped charge between tiers 2 and 3 during fabrication
  - Other design problems
    - ESD protection diodes are very leaky; serious problems for circuits with analog inputs
    - Current mirrors not working properly
  - Significant chip-to-chip variations
  - Yield is poor, reasons not understood
  - Measurements disagree with simulations
  - Long turn-around time
  - Not a commercial process
  - Discussions are ongoing with other users



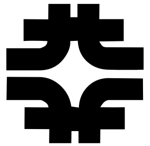
- MIT-LL has new DARPA sponsored 3D run in September '08 – feature size 150nm, SOI, 3 tiers
  - Fermilab will submit version 2 of the VIP chip addressing all known shortcomings

3D Initiative with Commercial Vendor



- Fermilab started an initiative with a local vendor who is one of the leaders in 3D: Tezzaron, based in Naperville (and Singapore) **http://www.tezzaron.com/**
- Tezzaron has fabricated a number of 3D chips for commercial customers
  - Memory devices and CMOS sensors
- Process Characteristics/Flow
  - Wafers with "Via First" process are made at a commercial foundry: Chartered Semiconductor in Singapore
  - Wafers bonded in Singapore by Tezzaron
    - Facility can handle up to 1000 wafers/month
  - Bonded wafers are finished by Tezzaron
    - (Bump) Bond pads
- Potential Advantages
  - Lower cost and faster turn around
  - One stop shopping
  - Process is available to customers from all countries

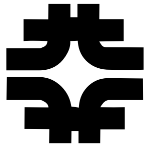
Chartered Semiconductor Manufacturing



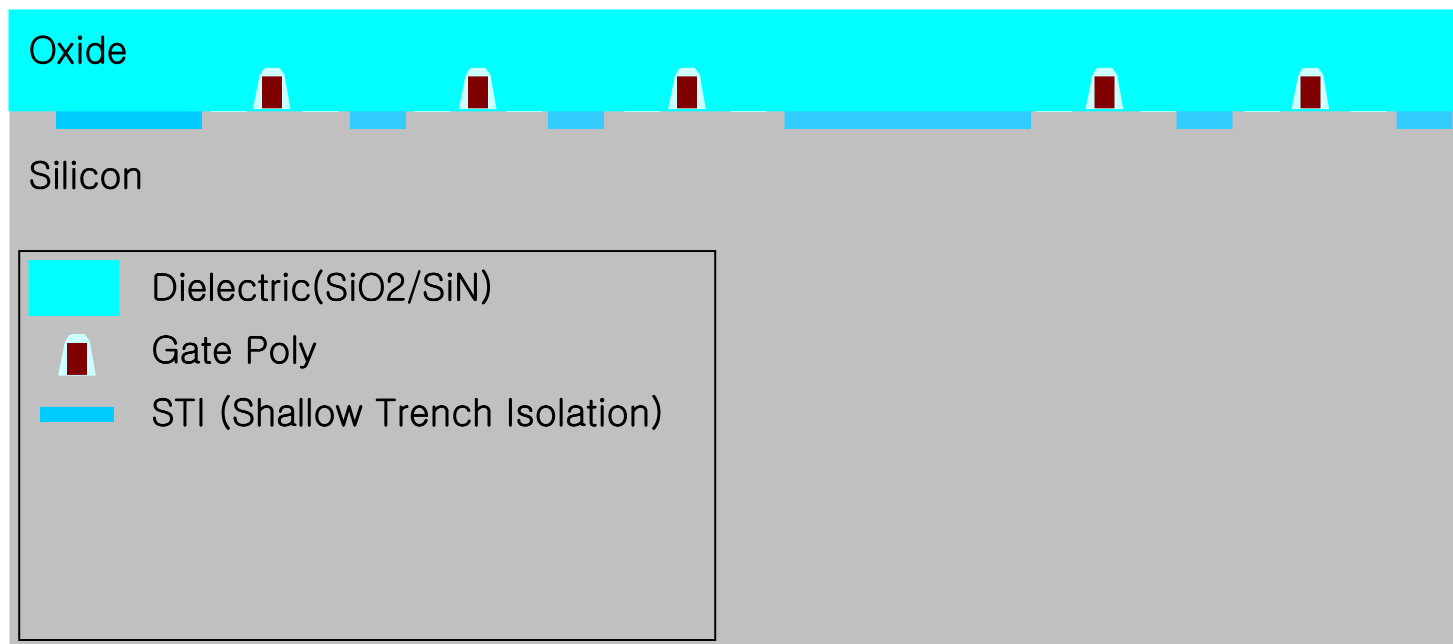
- Chartered Semiconductor Manufacturing fourth largest dedicated independent commercial semiconductor foundry, located in Singapore
  - Extensive line of CMOS and SOI processes from 500 nm down to 45 nm
  - Common Chartered-IBM platform for processes at 90 nm and below
  - Chartered 130 nm process is similar to the IBM 130 nm process but has different layer arrangement and transistor thresholds
  - Commercial tool support for Chartered Semiconductor
  - Chartered produced nearly 1,000,000 eight inch wafers in the 130 nm process

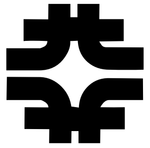
- Chartered 130 nm mixed signal CMOS process for 3D integration
  - 8 inch wafers
  - Reticle size 24 x 32 mm
  - Features:
    - Deep N-well
    - MiM capacitors – 1 fF/um2
    - Single poly
    - 8 levels of metal

Tezzaron Process



- Tezzaron employs “Via First – After FEOL” approach
  - Complete transistor fabrication on all wafers to be stacked
  - Etch super via on all wafers to be stacked
  - Fill super via at same time connections are made to transistors
  - Complete BEOL processing (metal layers)





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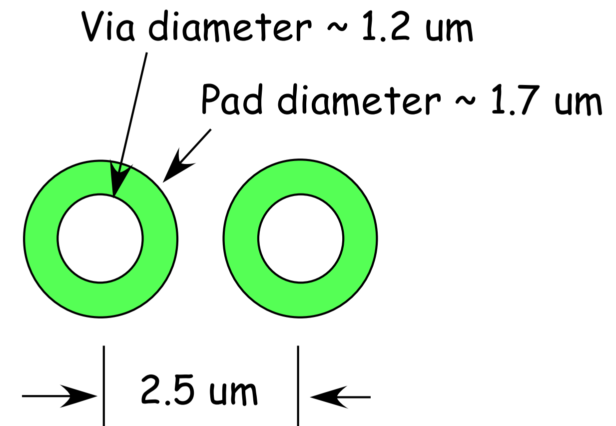

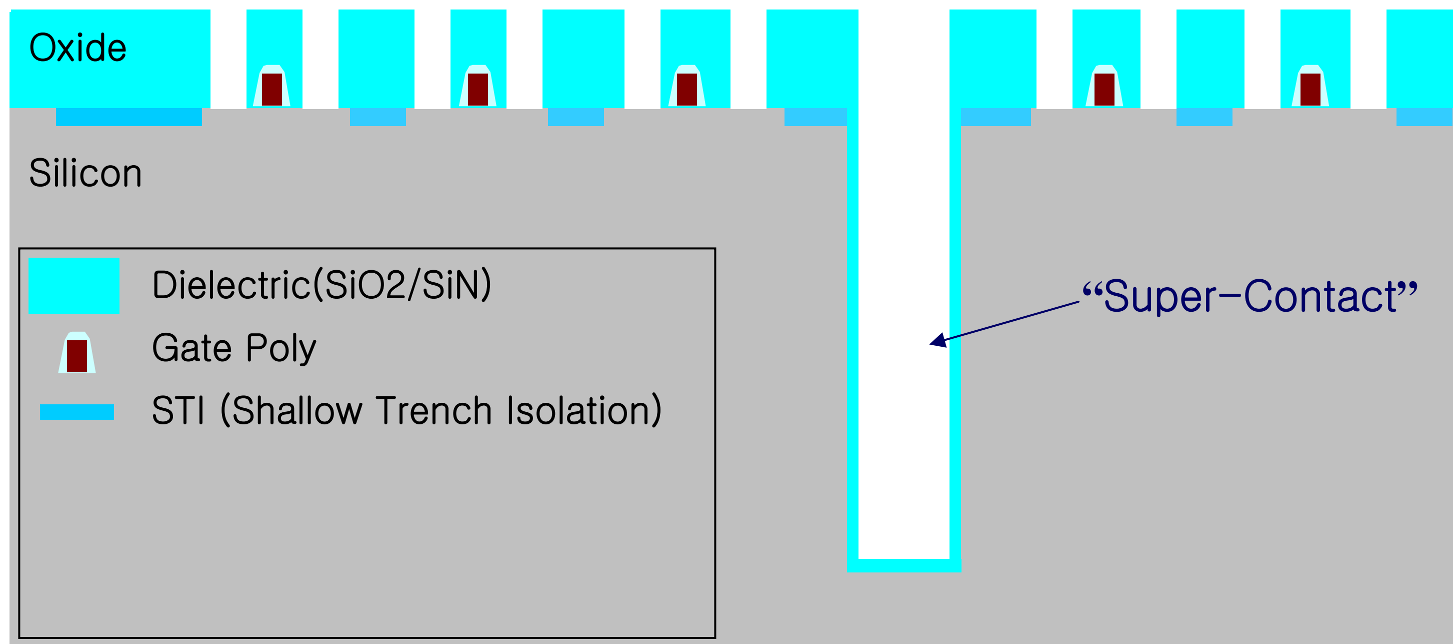

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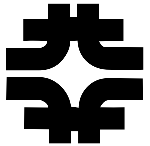

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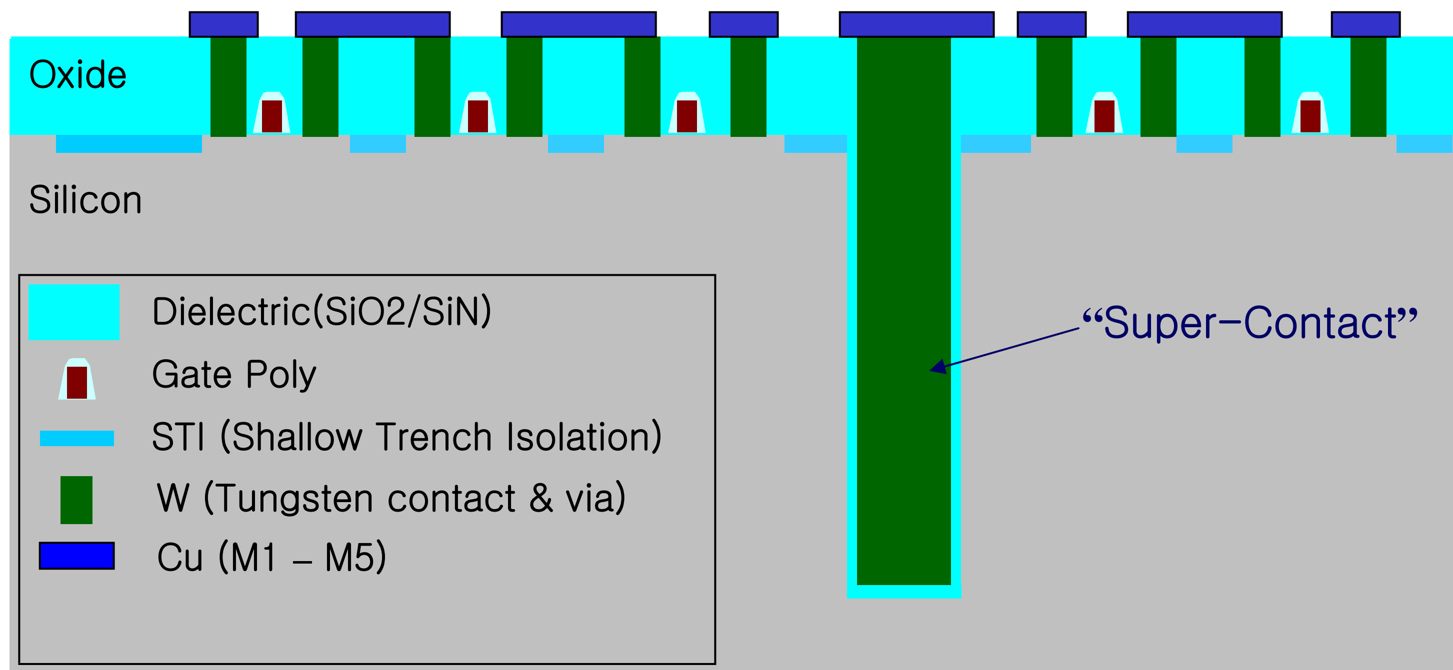
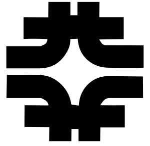


Tezzaron Process



- Tezzaron employs "Via First – After FEOL" approach
  - Complete BEOL processing: metal layers (8) and top Cu metal (0.8 μm)

Oxide

Silicon

"Super–Contact"

Dielectric(SiO2/SiN)

Gate Poly

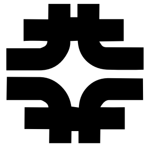
STI (Shallow Trench Isolation)

W (Tungsten contact & via)

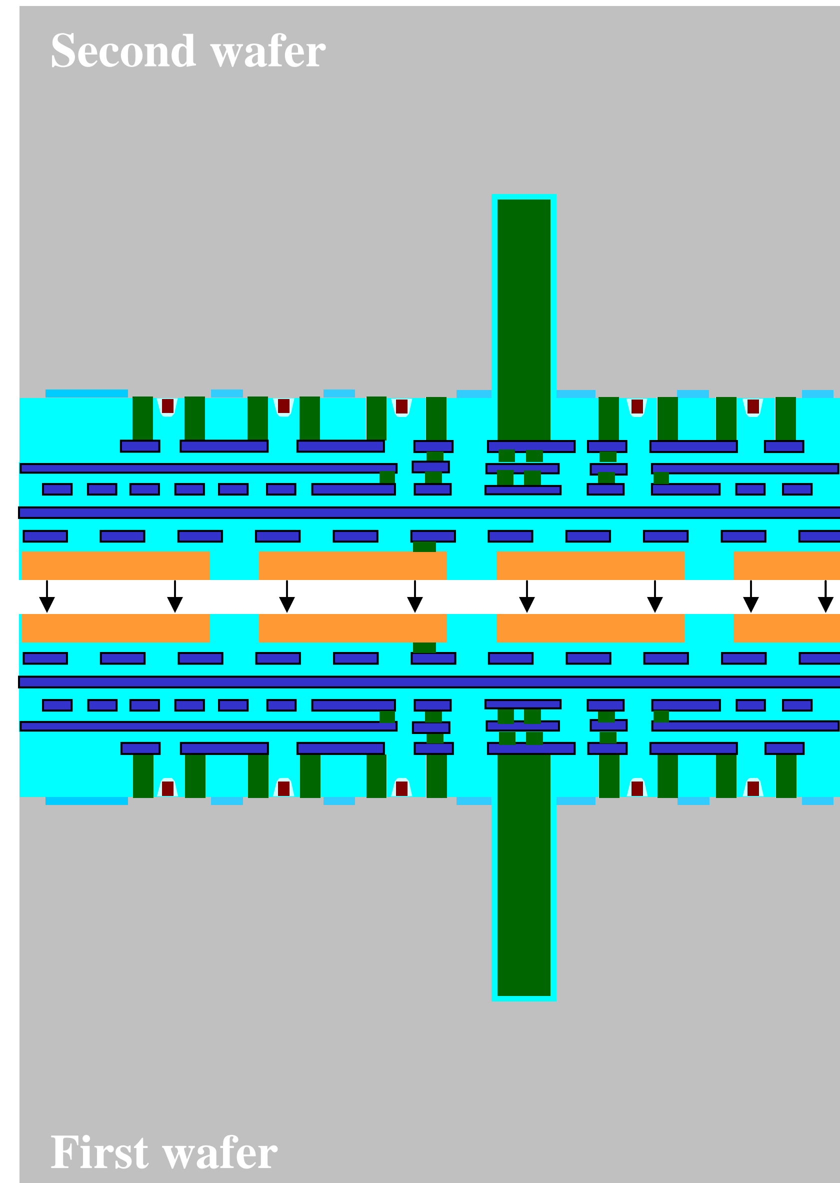
Cu (M1 – M5)

Cu (M6, Top Metal)

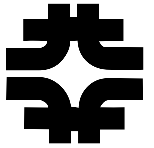
Tezzaron Stacking Process



- Stack second wafer
- Bond second wafer to first wafer using Cu-Cu thermo-compression bond
  - Bonding performed at 40 psi and 375 ^{o}C
  - Three sigma bonding alignment: 1 μm
  - Missing bond connections: 0.1 ppm
  - Temperature cycling of bonds from -65 to + 150 ^{o}C
    - 100 devices, 1500 cycles, 2 lots, no failures



Tezzaron Stacking Process



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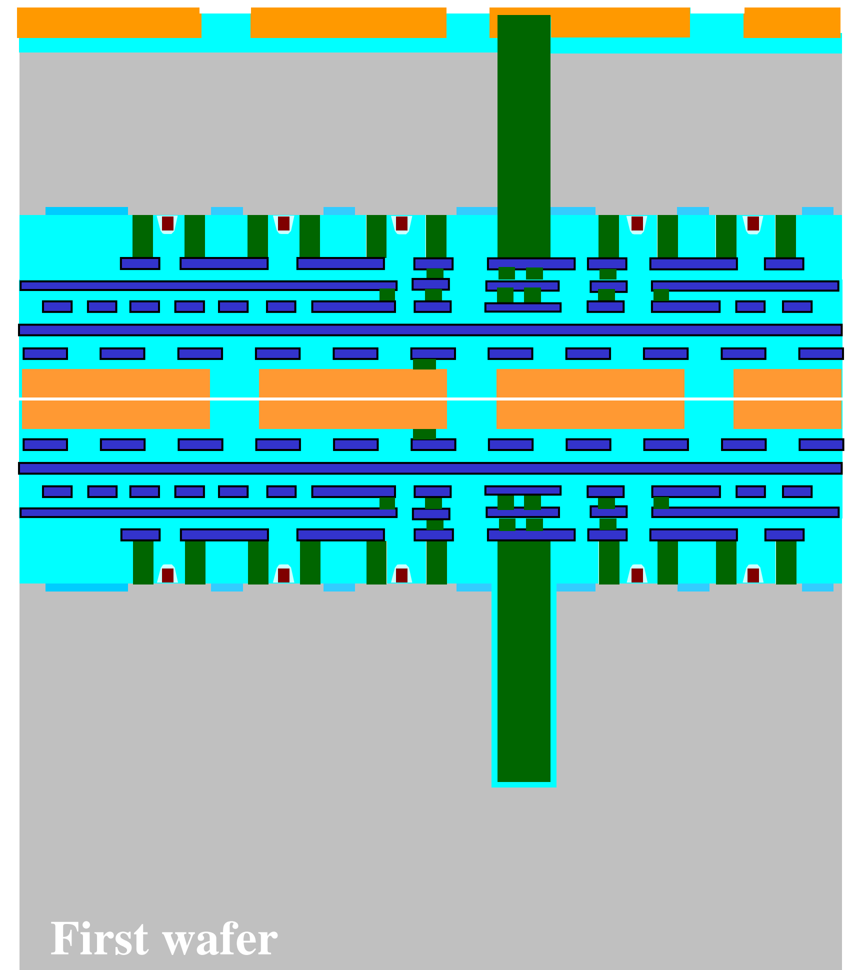
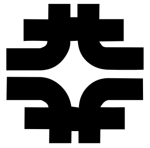
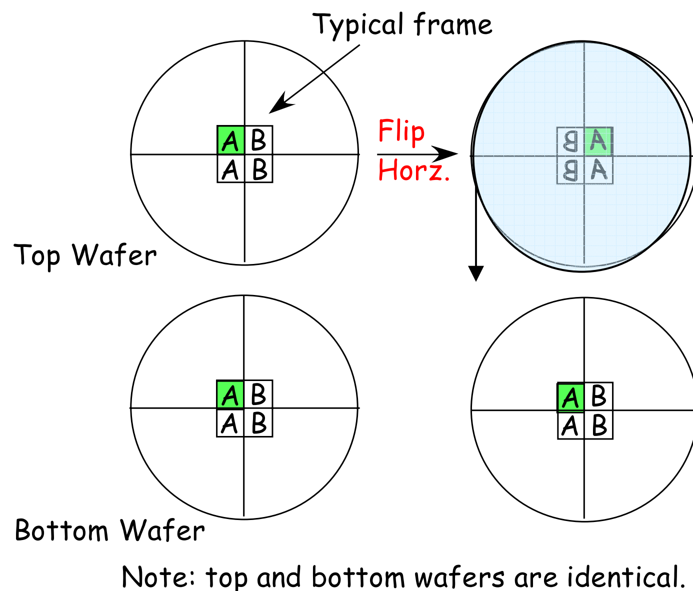
  - Three sigma bonding alignment: 1 μm
  - Missing bond connections: 0.1 ppm
  - Temperature cycling of bonds from -65 to + 150 ^{o}C
    - 100 devices, 1500 cycles, 2 lots, no failures
- Thin the second wafer to about 12 micron total thickness to expose super via.
- Add metallization to back of second wafer for bump- or wirebonding (or to bond second to third wafer)



Fermilab 3D Multi-Project Run



- Fermilab will be submitting a 3D multi project run to Tezzaron
- There will be only 2 layers of electronics fabricated in the Chartered 130 nm process, using only one set of masks. (Useful reticle size is 16 x 24 mm)
- The wafers will be bonded face to face
- Bond pads will be fabricated for bump bonding or DBI bonding at Ziptronix
- Offering open invitation to the community to participate



- Interested parties
  - Received LOI from CNRS/IN2P3
    - Strasbourg
    - Orsay – LAL
    - Paris 6/7 - LPNHE
    - Marseille – CPPM
  - Received LOI from INFN, Bergamo
  - Other groups have expressed interest

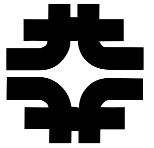
UNIVERSITÀ DEGLI STUDI DI BERGAMO
FACOLTÀ DI INGEGNERIA

Bergamo, April 18th, 2008

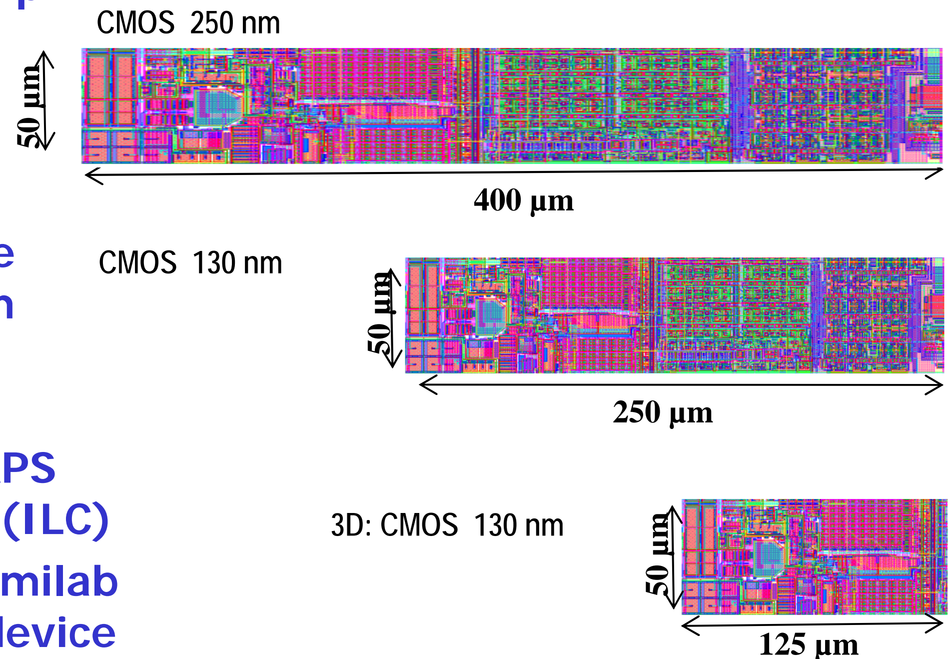
Ray Yarema
Head of the Electrical Engineering Department
Fermi National Accelerator Laboratory
Batavia, IL

Participation to Multiproject Engineering Run with Tezzaron

Candidate Projects for 3D MPW Run

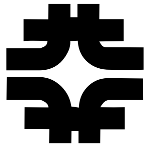


- Fermilab intents to submit a redesign of the VIP chip, adopted to 2 tiers
- Fermilab intends to develop a 3D chip to explore the advantages of 3D for the sCMS pixel detector (LHC)
- CPPM has expressed interest in converting the current 0.25 um ATLAS pixel design to a 3D structure with 2 tiers in the Chartered 130 nm process (LHC)
- Strasbourg proposes to work with Fermilab to develop a simple 3D MAPS device with 7 bits of time stamping (ILC)
- Bergamo proposes to work with Fermilab to develop a 3D version of a MAPS device using deep n-well with sparsification and time stamping (ILC/Super b-factory)



- Truly generic detector development with international base

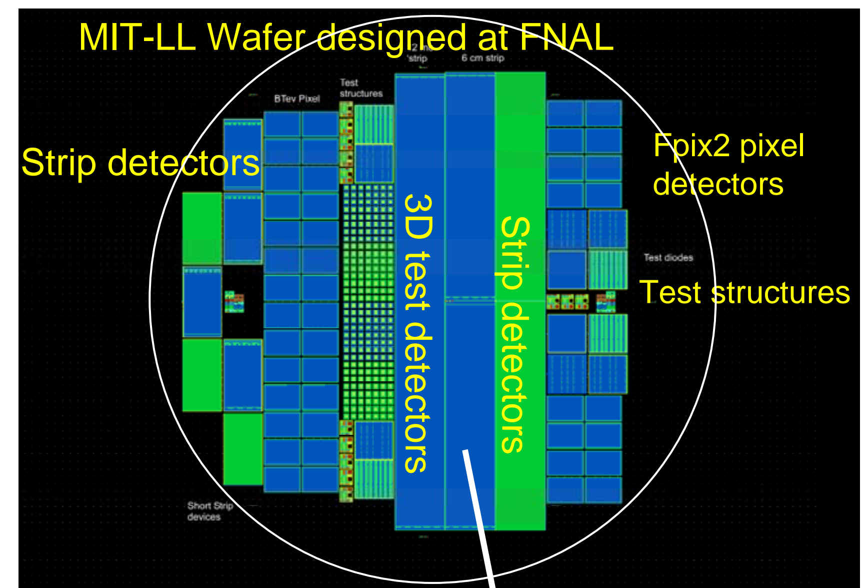
Towards Integrated Detectors

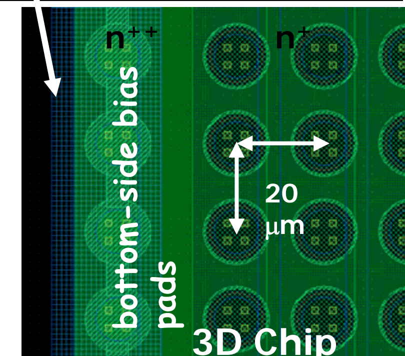


- Ultimate goal is to have integrated unit of front-end electronics and thin (~50μm thick) fully depleted detectors with very fine pitch
- Concurrent with 3D readout development, developing thin sensors with fine-pitch readout to be bonded to 3D readout devices

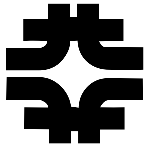
- Sensor Issues:
  - Device bonding
  - Sensor thinning and laser annealing
  - Development of edgeless sensors

- Thin edgeless sensors
  - Designed sensors on 6″ n-type wafers to be bonded to 3D chips
  - Sensors fabricated at MIT-LL
  - Thinned to 50 and 100 μm (depth of trenches), implanted and laser annealed
  - Deep trench etch, n doped poly-silicon fill provides edge doping
  - Sensors sensitive to the edge, 4-side abuttable, i.e. no dead space

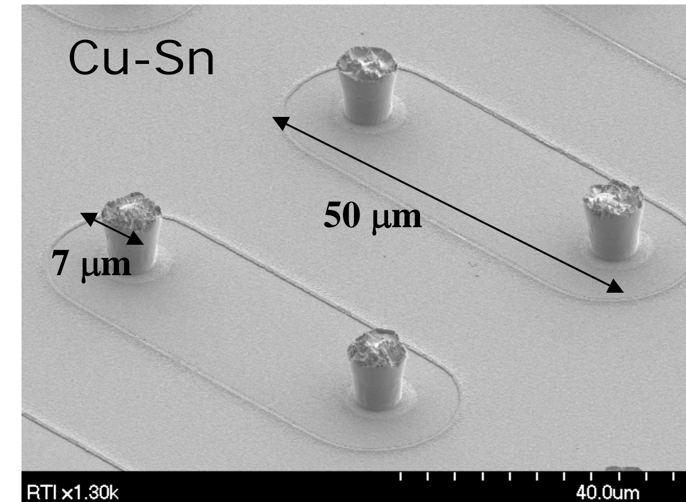


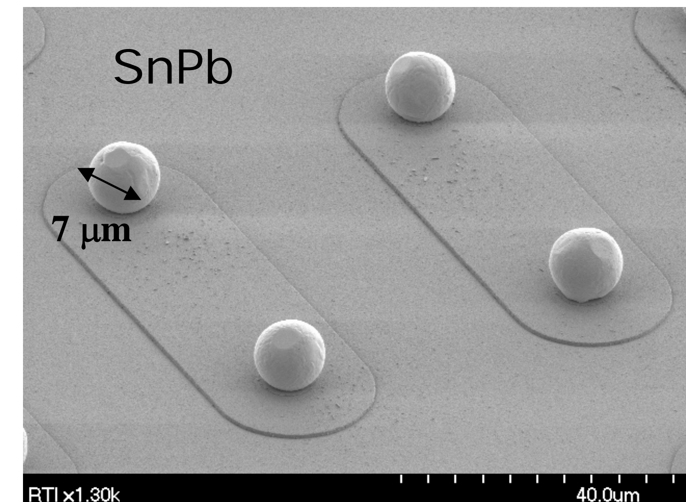


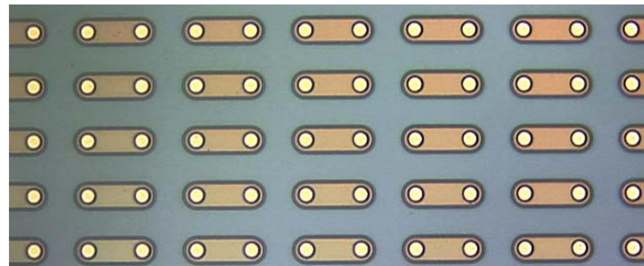
Device Bonding



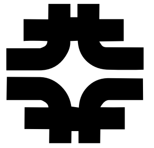
- Developed, in collaboration with RTI (NC), bump bonding process compatible with pixilated devices having a 20 μm pitch
- Completed design and fabrication of passive test structures based on 50 μm pitch, but using bumps compatible with 20 μm pitch
- Two test structures designed for testing
  - CuSn bonded to Cu
    - Cu-Sn: 7 μm diameter bump
    - Cu: 11 & 15 μm diameter bumps
    - 176 x 128 bump array (22528 bumps) 50 μm pitch in x and y
  - SnPb bonded to Ni/Au
    - SnPb: 7 μm diameter bump base
    - Ni/Au: 7 μm diameter bond pads
    - Daisy chains connecting 22 bumps



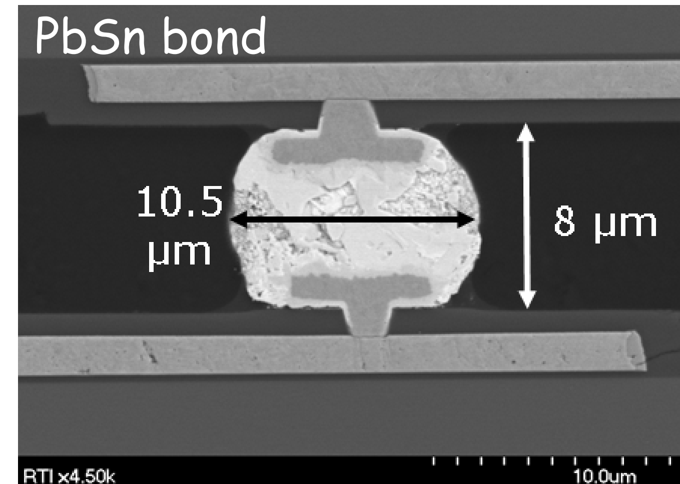




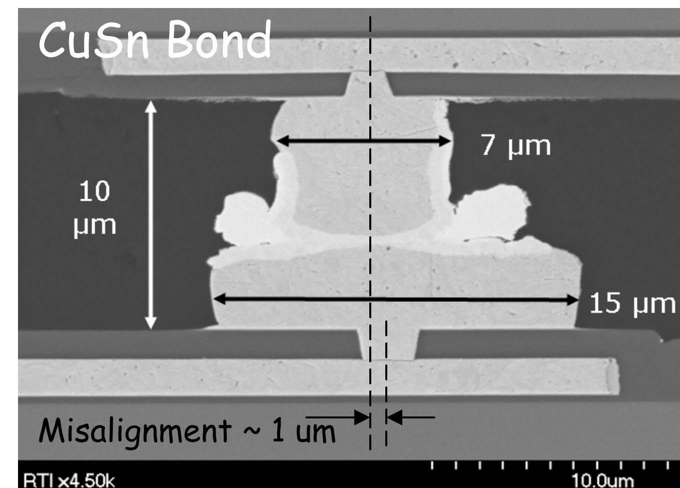
Fine Pitch Bump Bond Feasibility



- Results from tests
  - Bond yield of 10 μm PbSn balls poor
  - Bond yield of 7 μm CuSn on 11/15 mm Cu pad was 99.995%
  - All CuSn bonded chips had die shear strengths greater than the strongest PbSn bonded chip
  - Interconnect resistance 10~27 mΩ

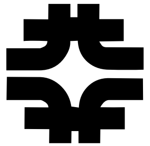


- Established feasibility of CuSn bonding for fine pitch (20 μm) assembly of 3D circuits and could apply these processes to functional 20 μm pitch devices that we have in hand
  - Both PbSn and CuSn bonds can represent a high X_o for fine pitch assemblies or high density interconnects

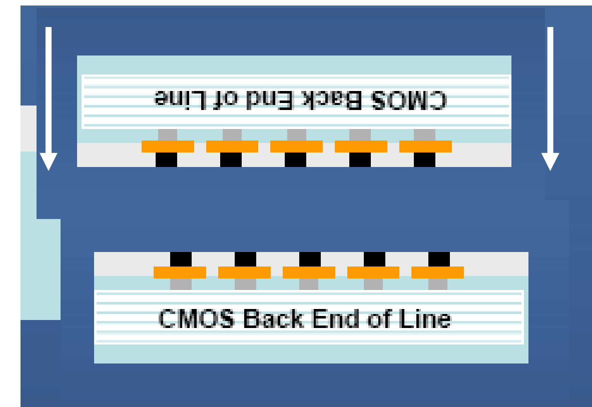


- As next step pursuing different technology that constitutes lower mass

Direct Bond Interconnect



- CuSn bump bonds pose a problem for low mass fine pitch assemblies
- Pursuing IC bonding to a detector with Ziptronix (NC) using the Direct Bond Interconnect (DBI) process
  - Significantly reduces material budget
  - Ziptronix DBI process allows aggressive post bond thinning due to the strength of the oxide bond
  - Tezzaron and Ziptronix are industrial partners
  - Understood bond yields for 10 μm pitch with 1Mbonds/cm^2

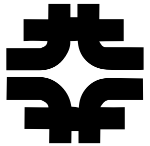


DBI:

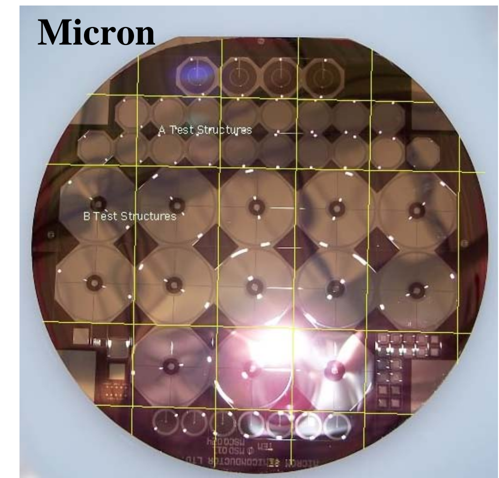
- **Plate DBI (magic) metal**
- **Deposit oxide, terminate surface with amine group**
- **Bring surfaces in contact**
  - $Si–NH_2 + Si–NH_2 \rightarrow Si\text{-}N\text{-}N\text{-}Si + 2H_2$
  - Bonding occurs at RT
  - Bond strength increase with t
- **After oxide bond is strong enough, wafers are heated to form thermo compression bond between Magic Metal implants.**

- Work plan with Ziptronix:
  - DBI process sensor and readout wafers
    - Including MIT-LL wafers and BTeV FPIX2.1 wafers
    - Thin the sensor chips to 75 microns (readout wafers not thinned for the time being)
    - Dice the bonded pairs
- Deliverable: >25 bonded pairs for further processing and testing

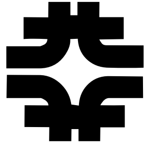
Sensor Thinning and Laser Annealing



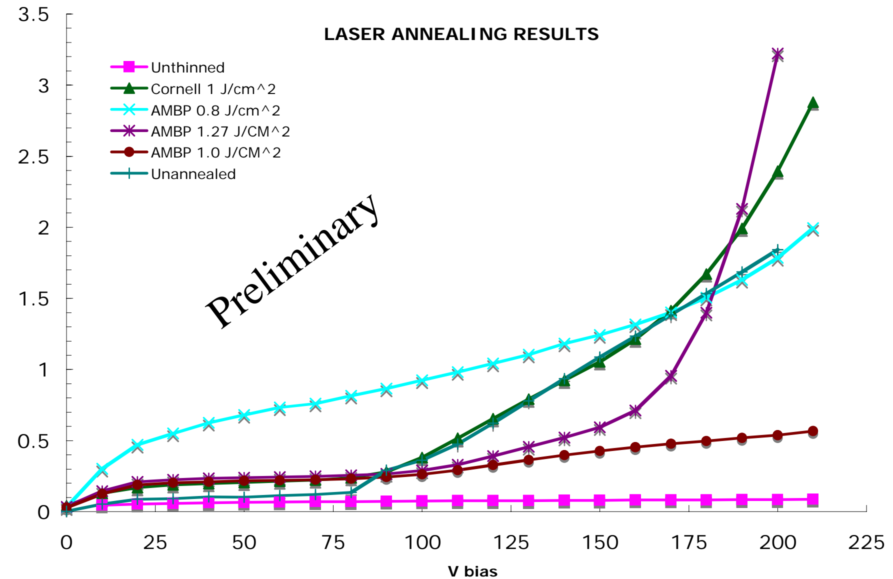
- Preferred detector thickness < 50μm
- Problem: After thinning provide a backside Ohmic contact while keeping the topside below ~500 ºC to protect topside CMOS circuitry
- Studies on two sets of sensors:
  - 300 μm thick silicon strip detectors (Hamamatsu), 4x10 cm^2 with low leakage current (Run IIb)
  - Si diodes from Micron Semiconductor (processed at MIT-LL; info proprietary)
- Processing steps:
  - Test wafers
  - Mount on pyrex handle, grind to 50 μm
    - remove back implant and aluminization
  - CMP (Chemical-mechanical planarization) to ~ 1 nm
  - Implantation to re-establish Ohmic contact
    - 10 KeV phosphorus at 0.5 and $1.0 \times 10^{15}/cm^3$ for HPK
  - Laser anneal
    - Use a raster scanned Excimer Laser to melt the silicon locally
    - This activates the Ohmic implant and repairs the implantation damage by re-crystallizing the silicon
      - AMBP - 0.8, 1.0, 1.2 J/cm^2, 248 nm laser
      - Cornell - 1.0 J/cm^2 305 nm laser

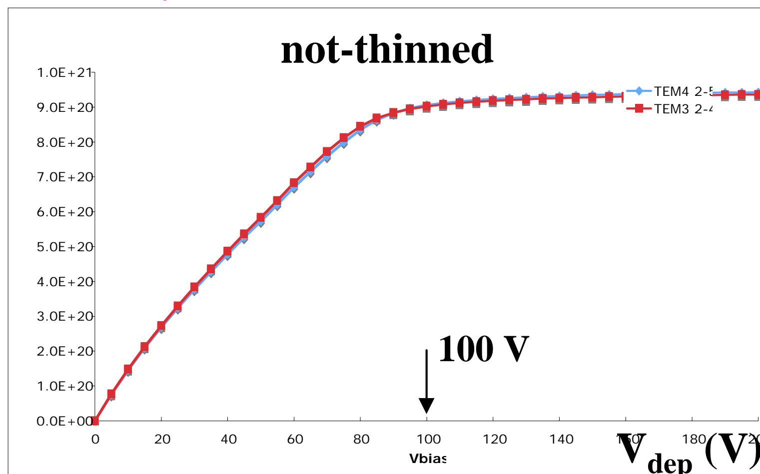


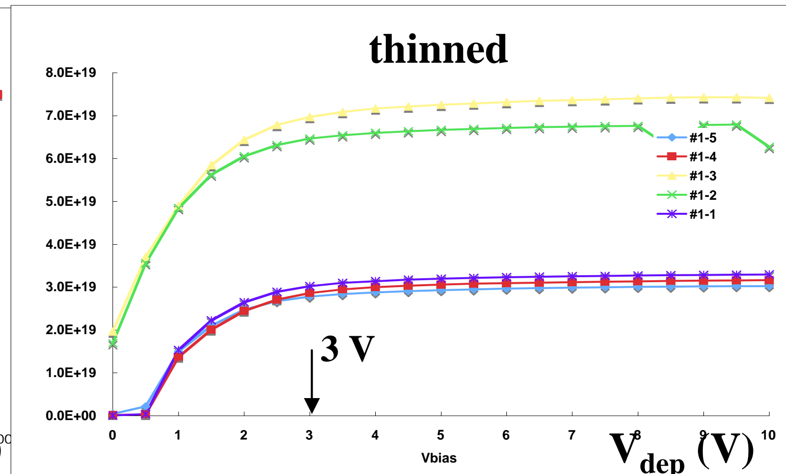
Sensor Thinning and Laser Annealing

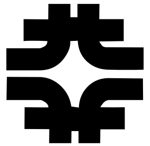


- Processing steps continued
  - Laser annealing IV result
  - Backside processing
    - Deposit Al layer on the back side to provide external connectivity
    - Mixed results so far on I_{leak}
  - Remove from handle, dice
  - Test of IV and CV
    - $V_{dep} \sim t^2$
    - $V_{dep} = \sim 90V$ (before)
    - $V_{dep} = \sim 3V$ (after)

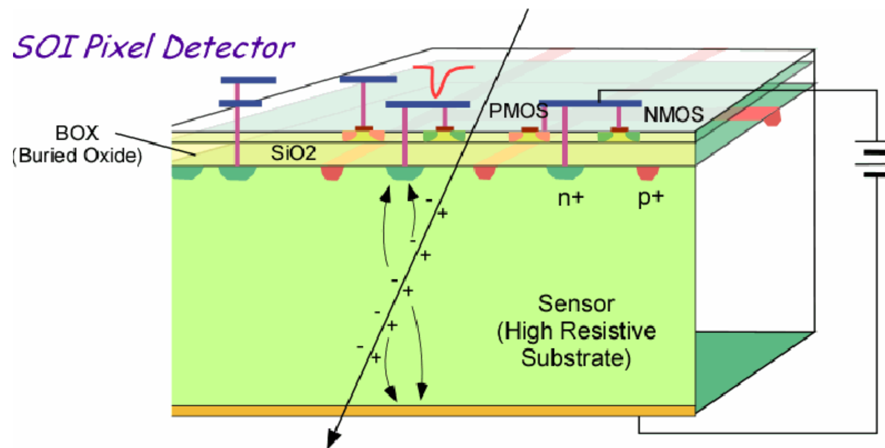






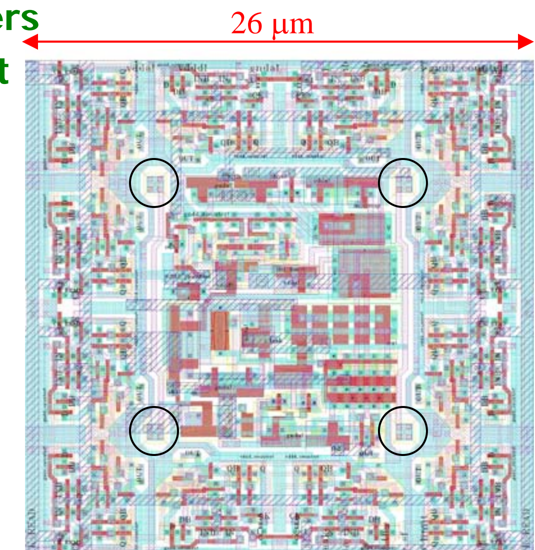


SOI Detectors

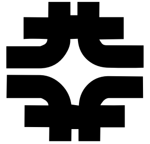


- **Bonded SOI Wafer**
  - low resistive top layer; standard CMOS Electronics (NMOS, PMOS)
  - separated through a Buried OXide (BOX) layer to
  - Bottom substrate layer which forms detector volume; diode implants are formed beneath the BOX and connected by vias

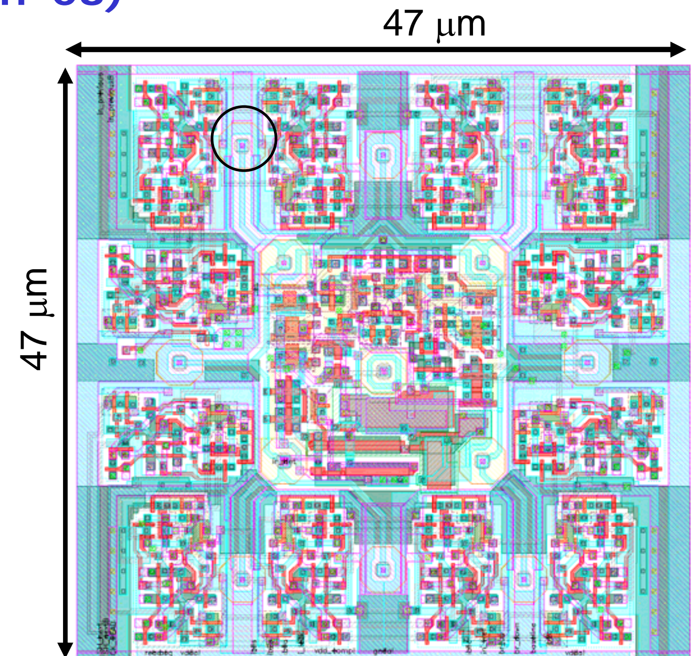
- Designed MAMBO Chip in the OKI (Japan/KEK) 150 nm process
  - MAMBO: Monolithic Active pixel Matrix with Binary cOunters
  - A wide dynamic range counting pixel detector plus readout circuitry, sensitive to 100-400 keV electrons, high energy X-rays, and mips
  - OKI process incorporates diode formation by implantation through the BOX
- Design submitted Dec. 15, ’06 received June ’07
- Chip characterized
  - Significant differences with simulation



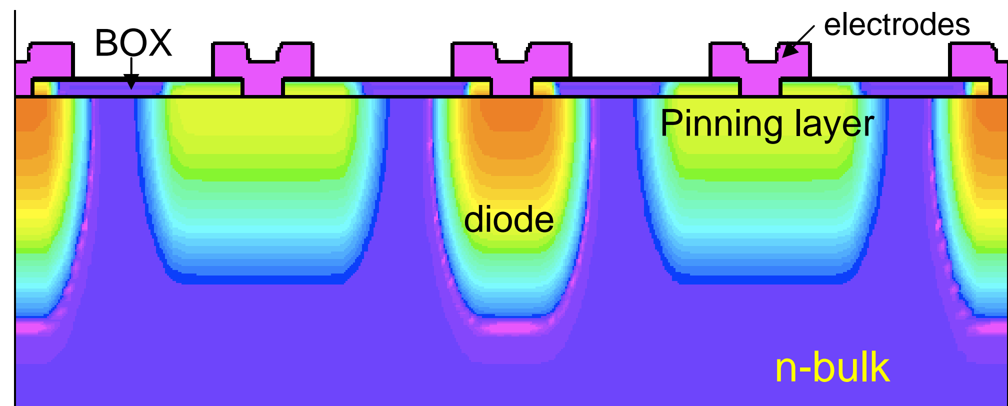
SOI Detectors



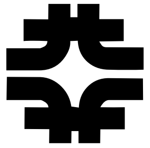
- Designed MAMBO II Chip in the OKI (Japan/KEK) 200 nm FD process, based on experience with MAMBO I (submitted March '08)
- Matrix of 94×94 pixels; 47 μm pitch
  - 13 charge collecting diodes
  - Integrated corrections of problems from MAMBO1



- Simulation of American Semiconductor, 180nm process, SOI diodes with dual gated transistor
  - Process parameter extraction for the diode fabrication
  - Full 3D device simulation of the diodes for the optimization of ASI based pixel detector
    - With pinning layer, charge collection gets worse (depletion thickness reduced)

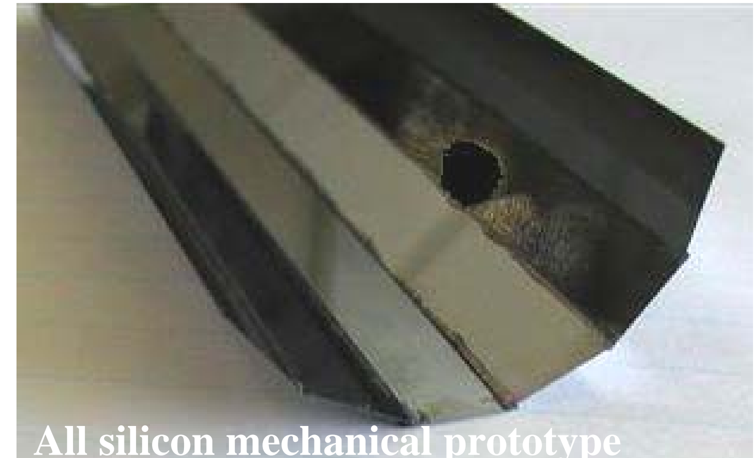


Pixel Detectors Mechanical Design



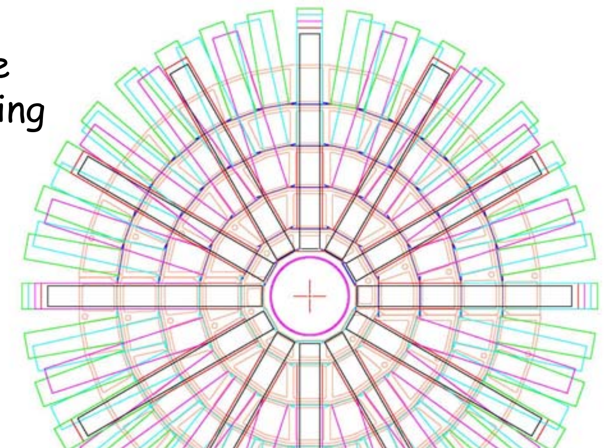
- For the SiD detector concept, proposed all silicon layout to mitigate CTE issues
  - Sensors glued to one another along edges by thin beads of epoxy and supported by thin, flat carbon fiber/epoxy end membranes
  - Table shows FEA study of gravitational sag and maximal displacements for a ΔT of 10 ^{0}C

Layer	Gravity (μm)	Δx (μm)	Δy (μm)	Δz (μm)
1	0.1	0.9	1.8	5.3
2	0.1	1.0	3.0	5.6
3	0.3	1.6	4.0	5.8
4	0.6	2.6	5.7	6.2
5	1.4	4.4	8.1	6.6



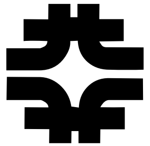
- Study of cables and material budget
  - Assumptions:
    - Four cables per "ladder" (two per end)
    - 0.070% X_0 per cable at normal incidence
    - 0.1% X_0 per "ladder" at normal incidence.
    - Cables run radially outward to the disk periphery
  - long barrel vs. barrel/disk design
    - 30°: 1.0% vs 1.35% X_0
    - 10°: 3.0% vs 1.8% X_0

Cable Routing



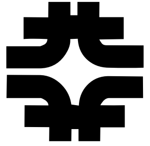
Note: cabling to bring signals of long ladders to ladder ends not included yet in the radiation length calculation.

Conclusion



- Fermilab's goal is an overall integrated pixel detector development program for future experiments
- Identified the 3D integrated technology as the most promising development, with work commencing in 2006
- Study of SOI technology for application of particle detectors
- Achievements to date:
  - 3-tier VIP chip in MIT-LL, 150nm, SOI process. Able to readout all channels!
  - Binary pixel counter, MAMBO, in OKI 150nm SOI process
  - Wafer thinning and laser annealing
  - Exploration of various bonding technologies for very fine pitch detectors
  - Ultra low-mass mechanical designs
- Plans:
  - 3-tier VIP-II chip to MIT-LL, 200nm, SOI process
  - Binary pixel counter, MAMBO-II, in OKI 200nm SOI process
  - Continue wafer thinning and laser annealing
  - Direct Bonding of 50mm readout and 100mm sensors with Ziptronix
  - Study of impact of cable routing
  - Submission of serial powering chip, SPI-chip
  - 3D MPW run with Tezzaron
- Plan to forge ahead in all areas
- Very hopeful that our new direction of exploring commercial vendor for 3D process will deliver successful devices on very short timescale
- Collaborators always welcome!

Invitation for Pixel08



- Pixel08 Workshop, to be held at Fermilab, September 23-26, 2008
  - http://conferences.fnal.gov/pixel2008/
  - Confirmed invited speakers:
    Maurice Garcia- Sciveres (LBL)
    Peter Siddons (BNL)
    Bob Patti (Tezzaron)
    Dr. Fukushima or
    Dr. Motoyoshi (Zycube/Tohuku)
    Jan Jakubek (Czech Tech. University)
    Klaus Gaertner (Weierstrass Institute)
    Tsuyoshi Nakaya (Kyoto)

Pixel08

International Workshop
on Semiconductor Pixel Detectors
for Particles & Imaging

Fermilab 23-26 September 2008

Key Topics
Pixels for HEP & Nuclear Physics, Current Experiments • Pixels for HEP & Nuclear Physics, Future Experiments
Pixels for Imaging in Medicine, Biology & Material Science • Pixels for Astronomy & Astroparticle Physics Experiments
Pixels for Light Sources • New Pixel Technologies • Pixels for Vision & Commercial Applications

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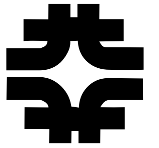
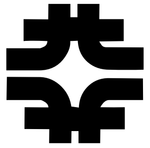
Backup Slides

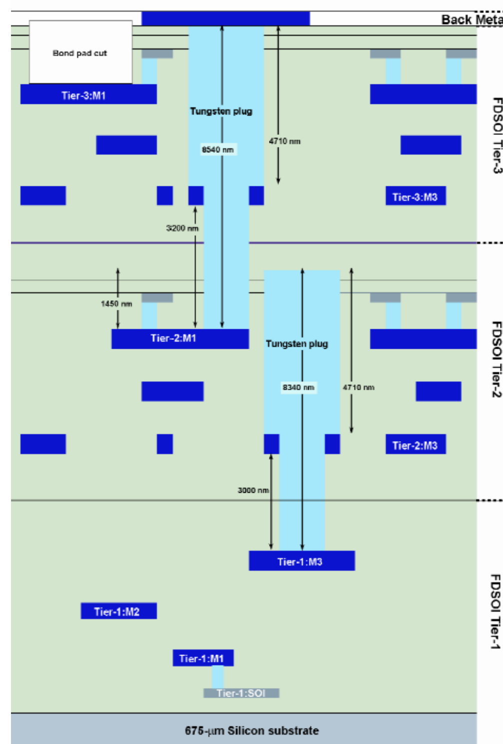


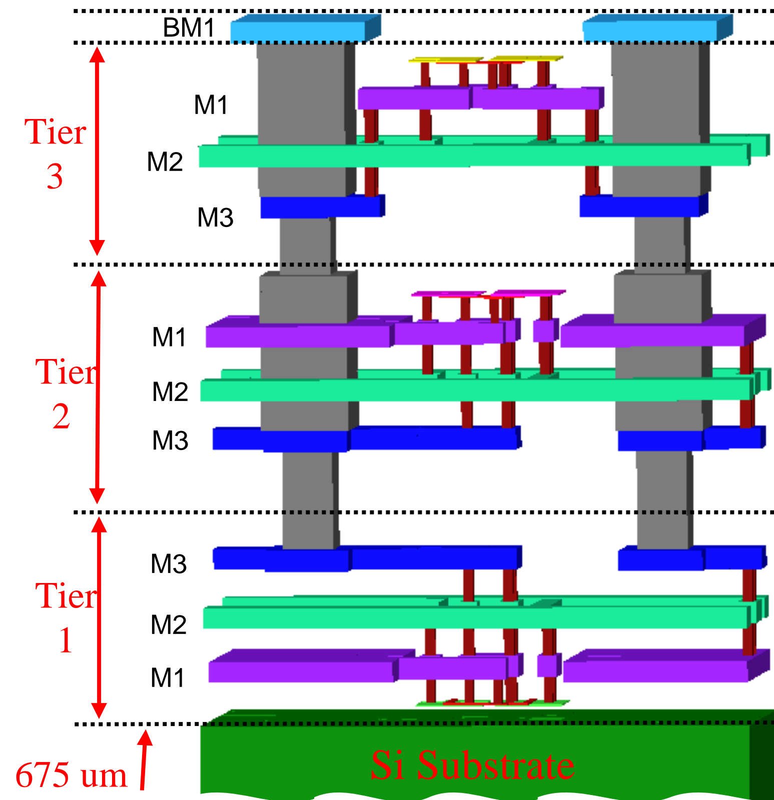
Modeling 3D Circuits



- Applied for an SBIR Phase I grant with CFD Research Corporation (www.cfdrc.com) to develop automated design tools for detector and electronics integration which will allow the extraction of physical parameters of these devices based on the integrated circuit layout
  - Modeling and analysis of radiation effects
  - Modeling of thermal and mechanical properties

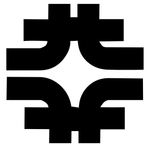
MIT-LL 3D Layer Description





CFDRC Full 3D Model

Pixel Readout Scheme



- Pixel being read points to the x address and y address stored on the perimeter.
- At same time, time stamp information and analog pulse height is read out
- During pixel readout, token scans ahead for the next hit pixel (200 ps/cell)

Assume 1000 x 1000 array
X and Y addresses are 10 bits each

X
Y
Time
Digital Data Mux X,Y,Time
Serial Data out (30 bits/hit)

Y address bus

Analog outputs
Start Readout Token

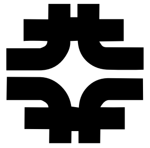
10
X=1
T1buf
10
X=2
T2buf
X=1000

1
5
T1
1
5
T2

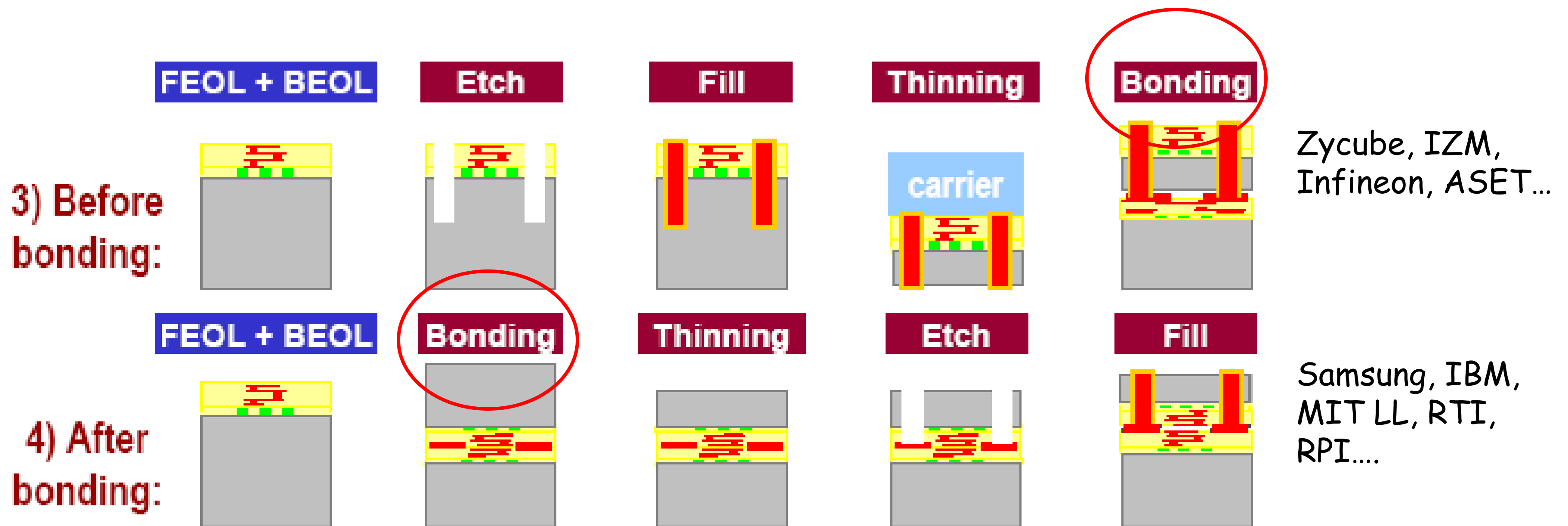
cell 1:1
cell 2:1
cell 1000:1
10
Y=1
1
Token to row Y=2
cell 1:2
cell 2:2
cell 1000:2
Y=2
Token to row Y=3
cell 1:3
cell 2:3
cell 1000:3
Y=3

Note: All the Y address registers can be replaced by one counter that is incremented by the last column token.

VIA Last Approach

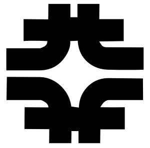


- Via last approach occurs after wafer fabrication and either before or after wafer bonding



Notes: Vias take space away from all metal layers. The assembly process is streamlined if you don't use a carrier wafer.

VIA First Approach



- Through silicon Via formation is done either before or after CMOS devices (Front End of Line) processing