EUDET HCAL Electronics Integration

Riccardo Fabbri

on behalf of the *CALICE* Collaboration

ECFA 2008 **Warsaw, 10 June 2008**

- **Physics Motivation and Design Constraints**
- **SPIROC Chip**
- **HCAL Base Units**
- **HCAL Endcap Board**
- **Time Schedule**
- **Conclusions and Outlook**

Physics Requirements and Design Constraint

- **Integration of Electronics into Analogue Hadronic Calorimeter (HCAL) for ILC**

- **Thousand of channels to be handled (high-granularity calorimeter)**

  $\Longrightarrow$ **physics motivation: particle data flow**

- **Non-invasive integration needed; as close as possible to active area in detector**

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  $\Longrightarrow$ physics motivation: particle data flow

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  $\Longrightarrow$ compact design with integrated sensors & electronics

  — minimum dead areas

  — minimum power consumption

  — maximum compactification

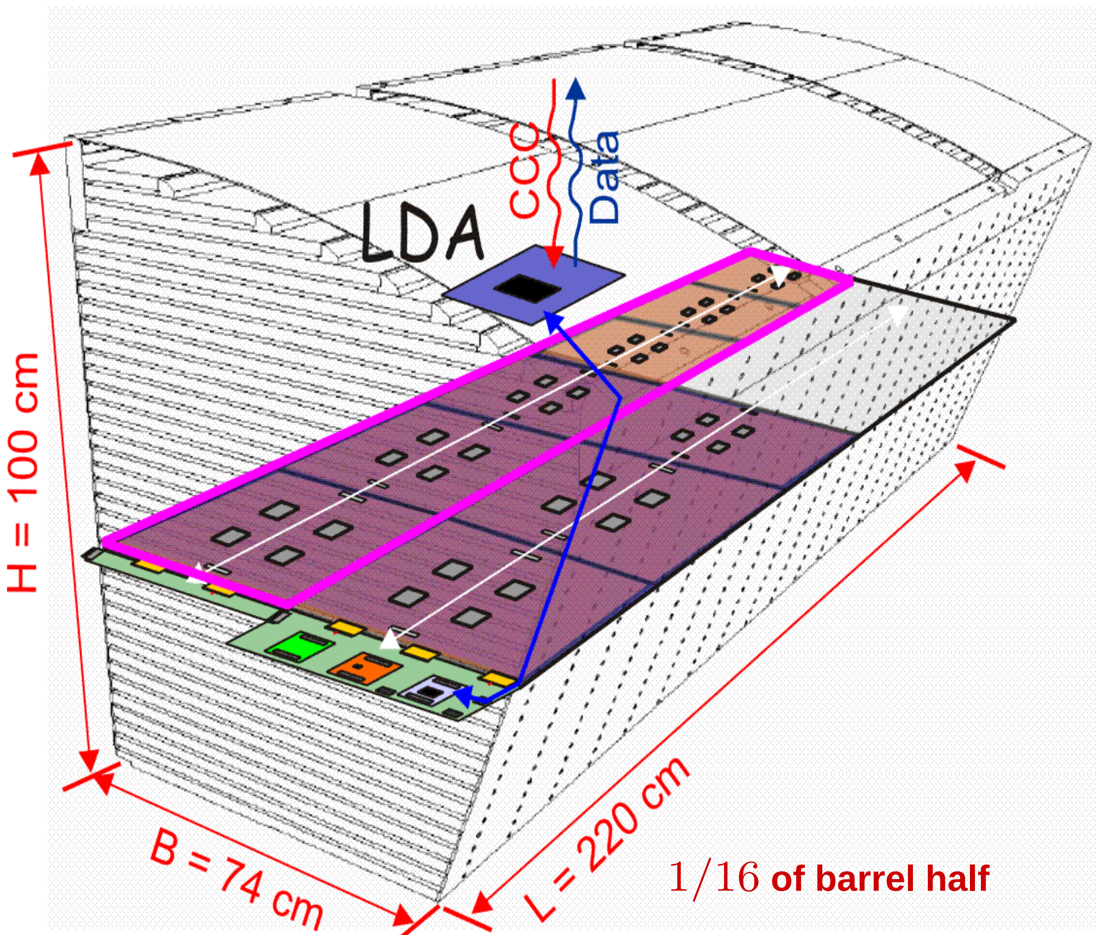
Design Proposal

Barrel of HCAL architecture:

— **scintillator-based calorimeter**

— **granularity: $3x3$ cm^2 tiles**

— **SiPM readout (one per tile)**



$1/16$ **of barrel half**

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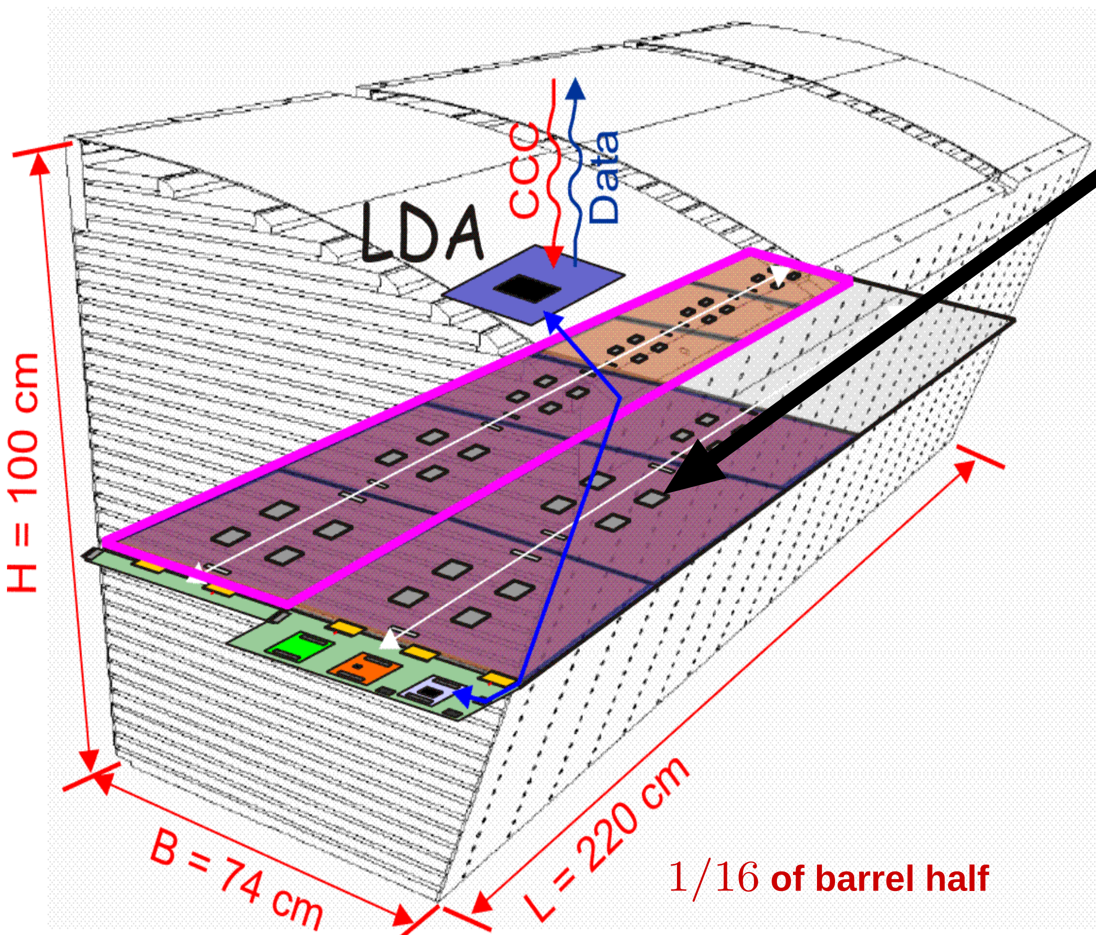

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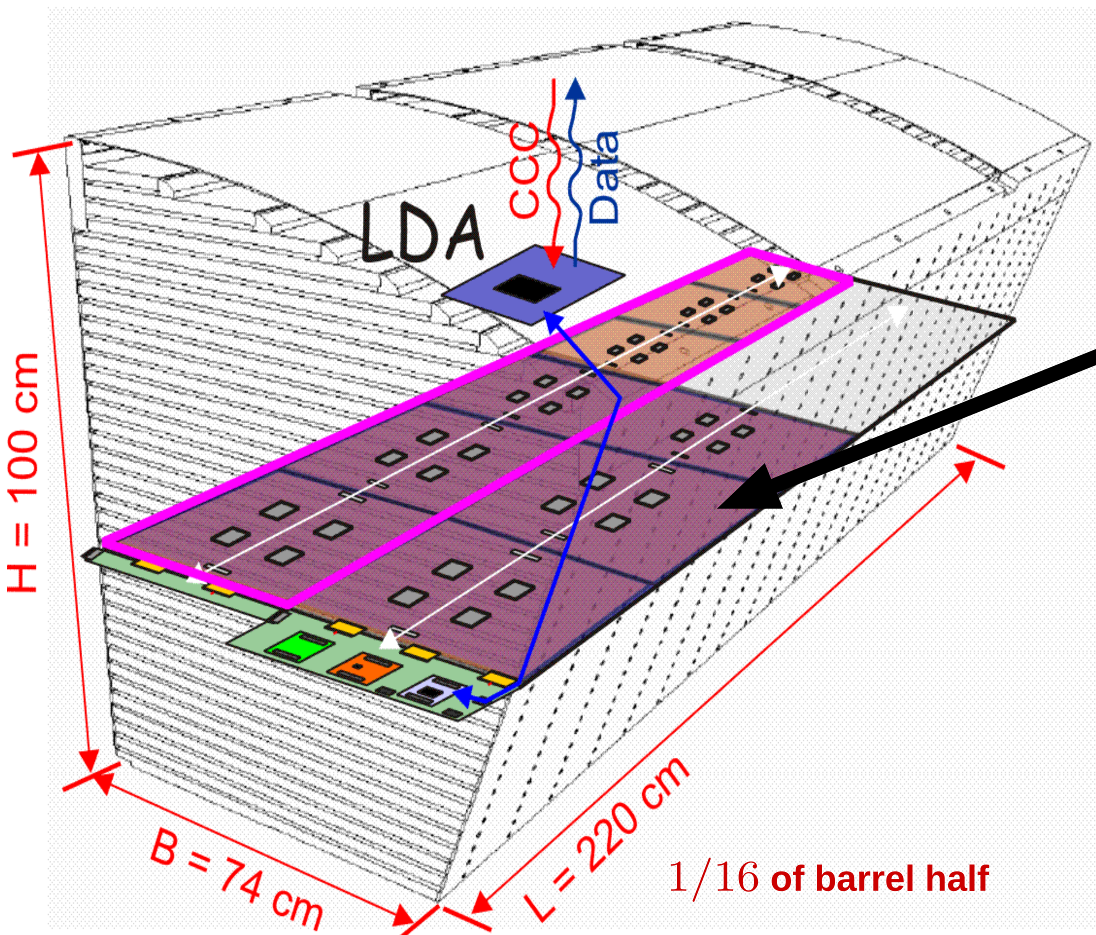

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  hosts up to $12x12$ tiles/4SPIROCs

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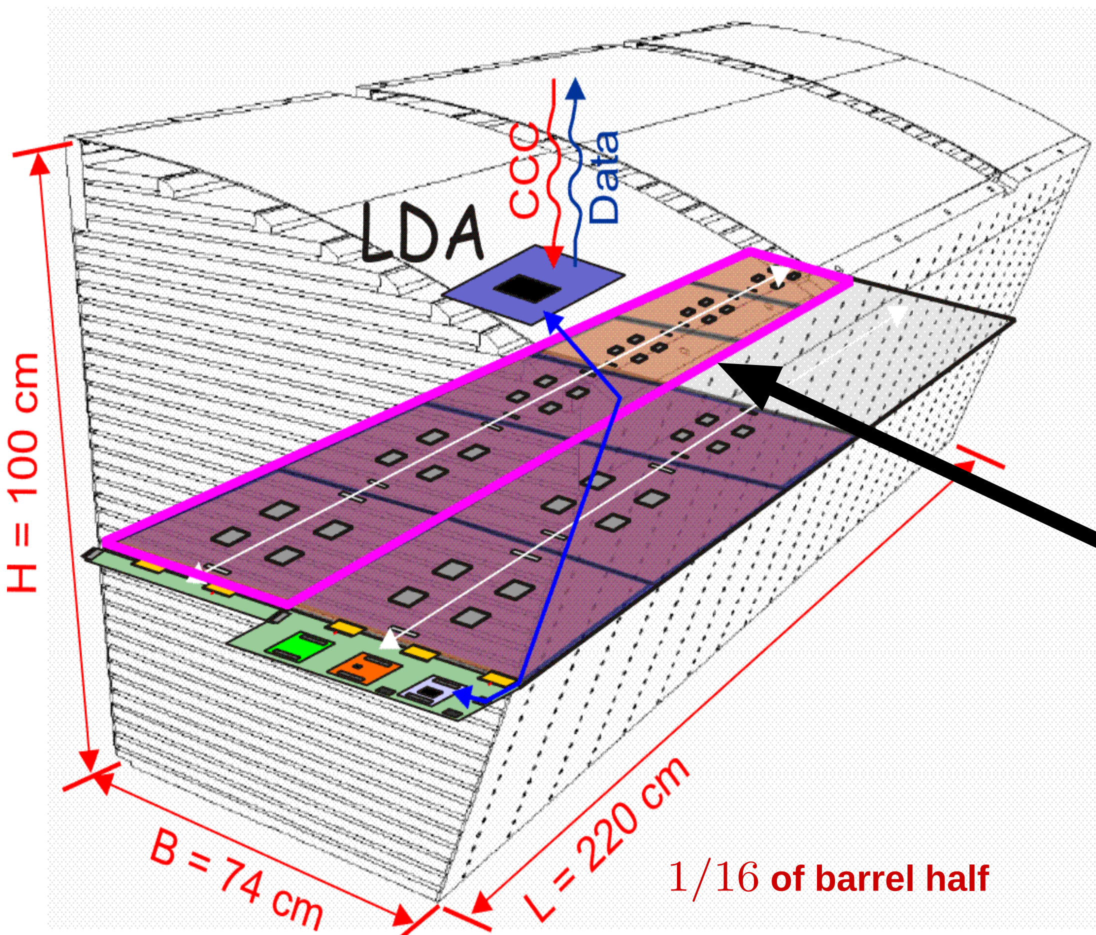

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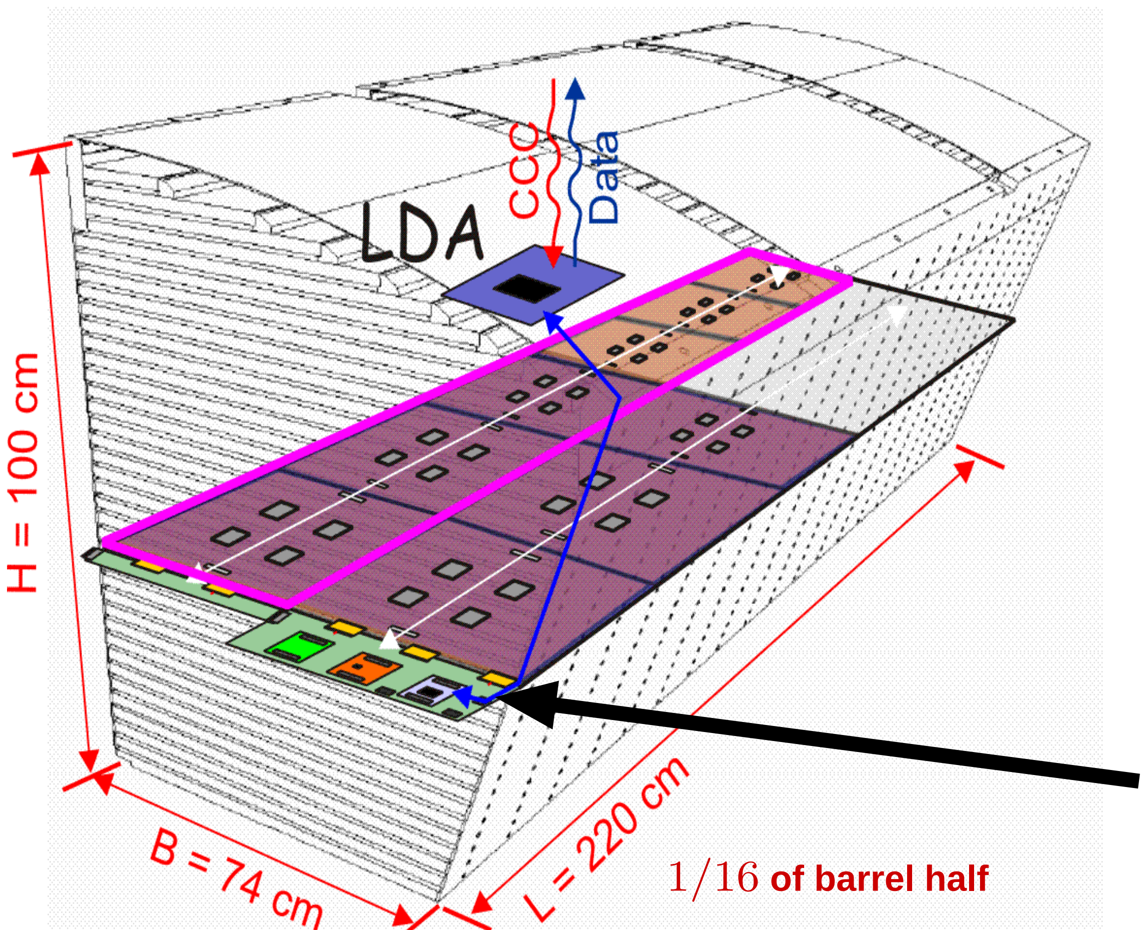

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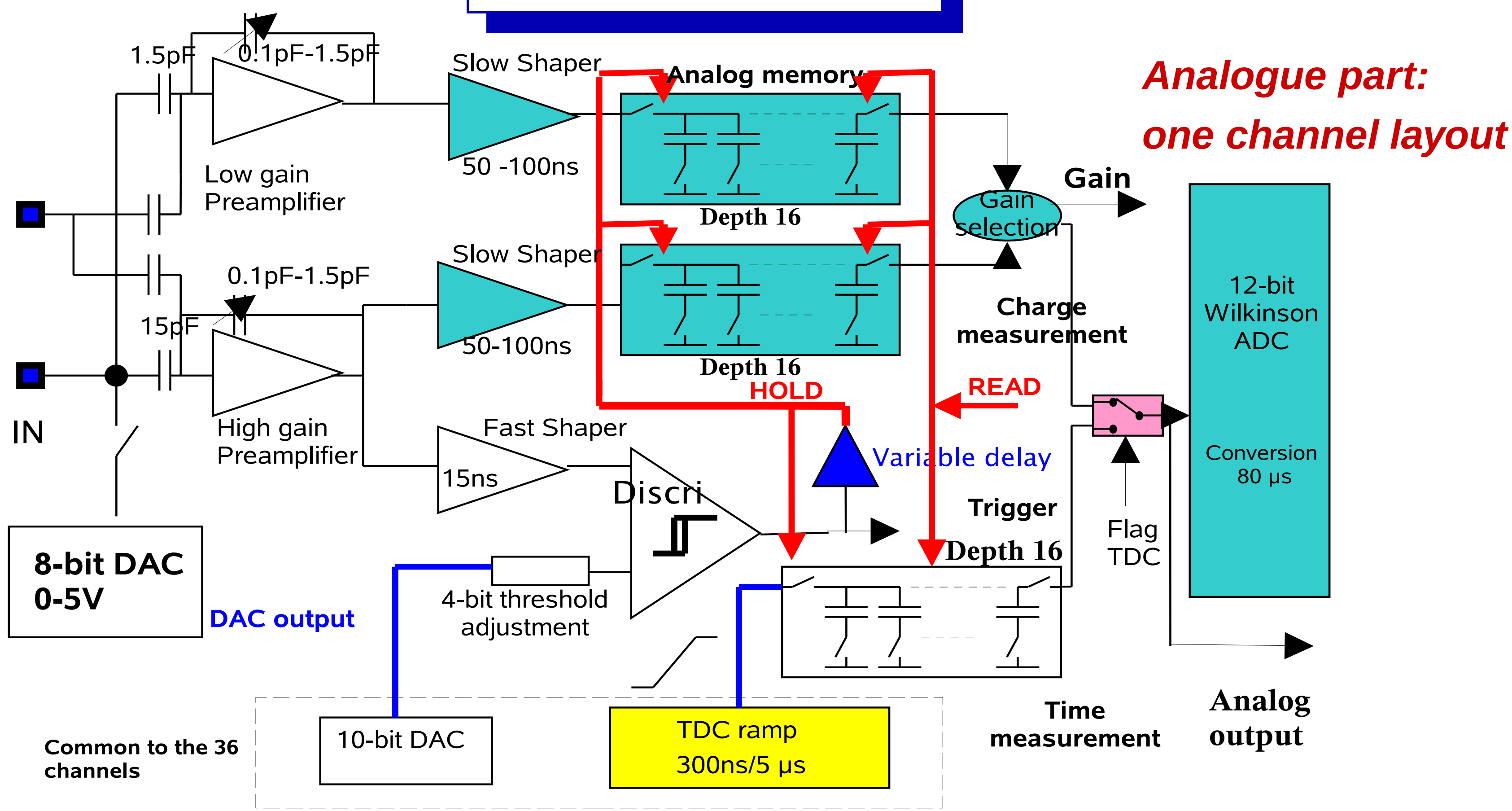
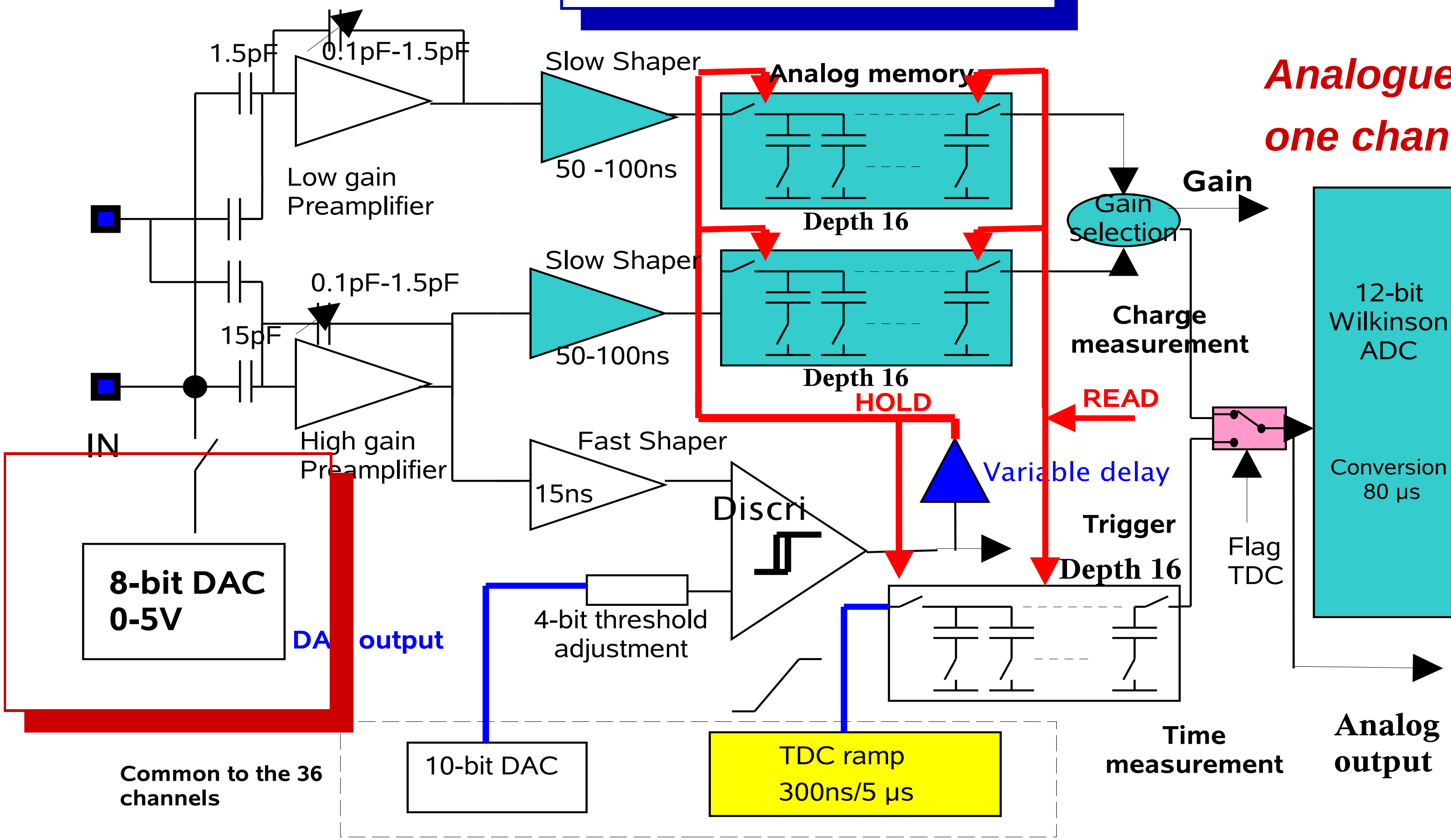
- **HEB (HCAL Endcap Board):**
  hosts DIF $CALIB$ $POWER$ modules

SPIROC Chip



Analogue part:
one channel layout
1.5pF
0.1pF-1.5pF
Low gain
Preamplifier
Slow Shaper
50 -100ns
Analog memory
Depth 16
Gain
Gain
selection
15pF
0.1pF-1.5pF
High gain
Preamplifier
Slow Shaper
50-100ns
Depth 16
Charge
measurement
12-bit
Wilkinson
ADC
Conversion
80 µs
IN
HOLD
READ
Fast Shaper
15ns
Variable delay
Discri
Trigger
Depth 16
Flag
TDC
8-bit DAC
0-5V
DAC output
4-bit threshold
adjustment
Time
measurement
Analog
output
Common to the 36
channels
10-bit DAC
TDC ramp
300ns/5 µs

SPIROC Chip

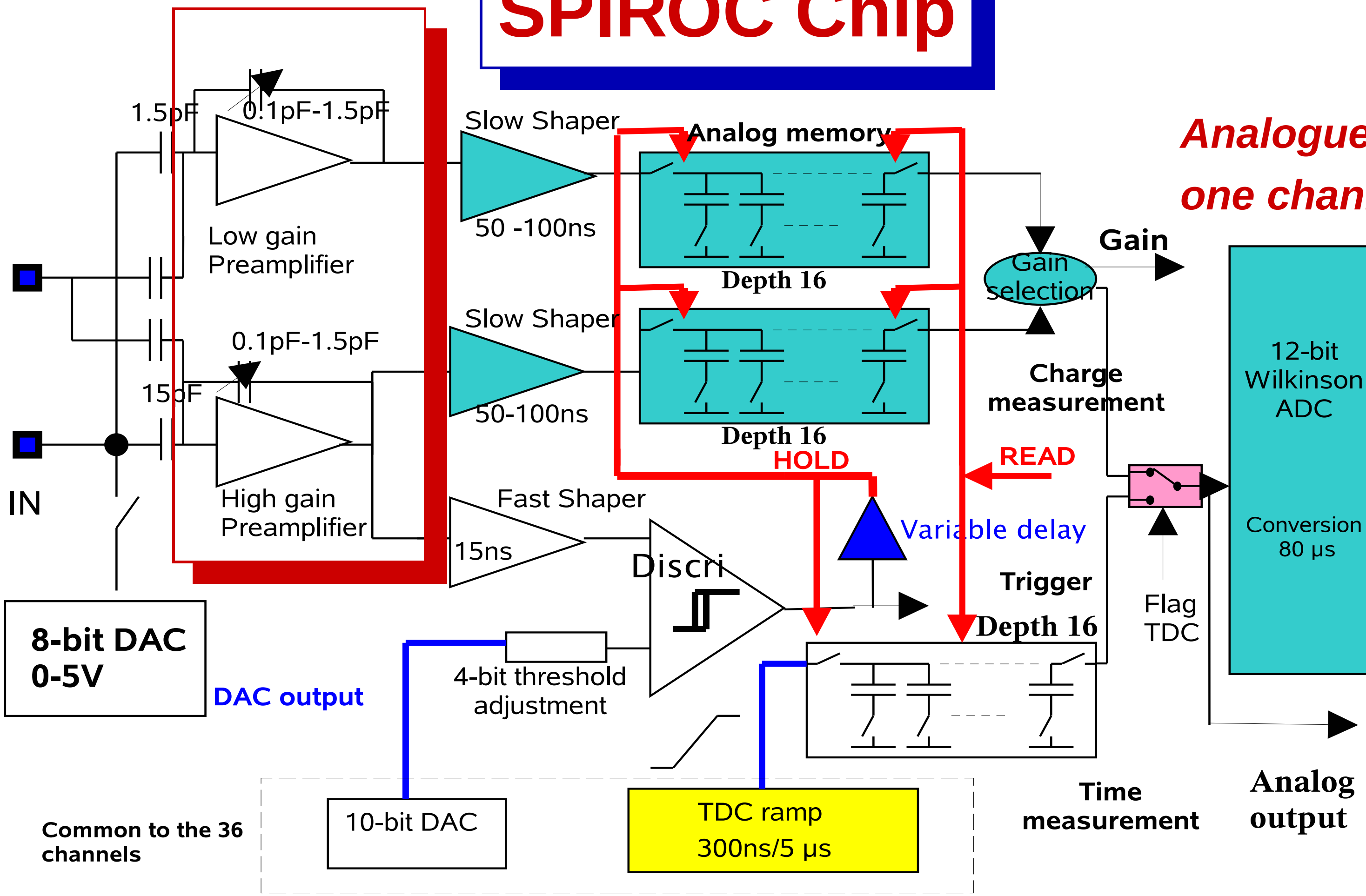


Analogue part:
one channel layout

Adjustable bias voltage for each SiPM

SPIROC Chip

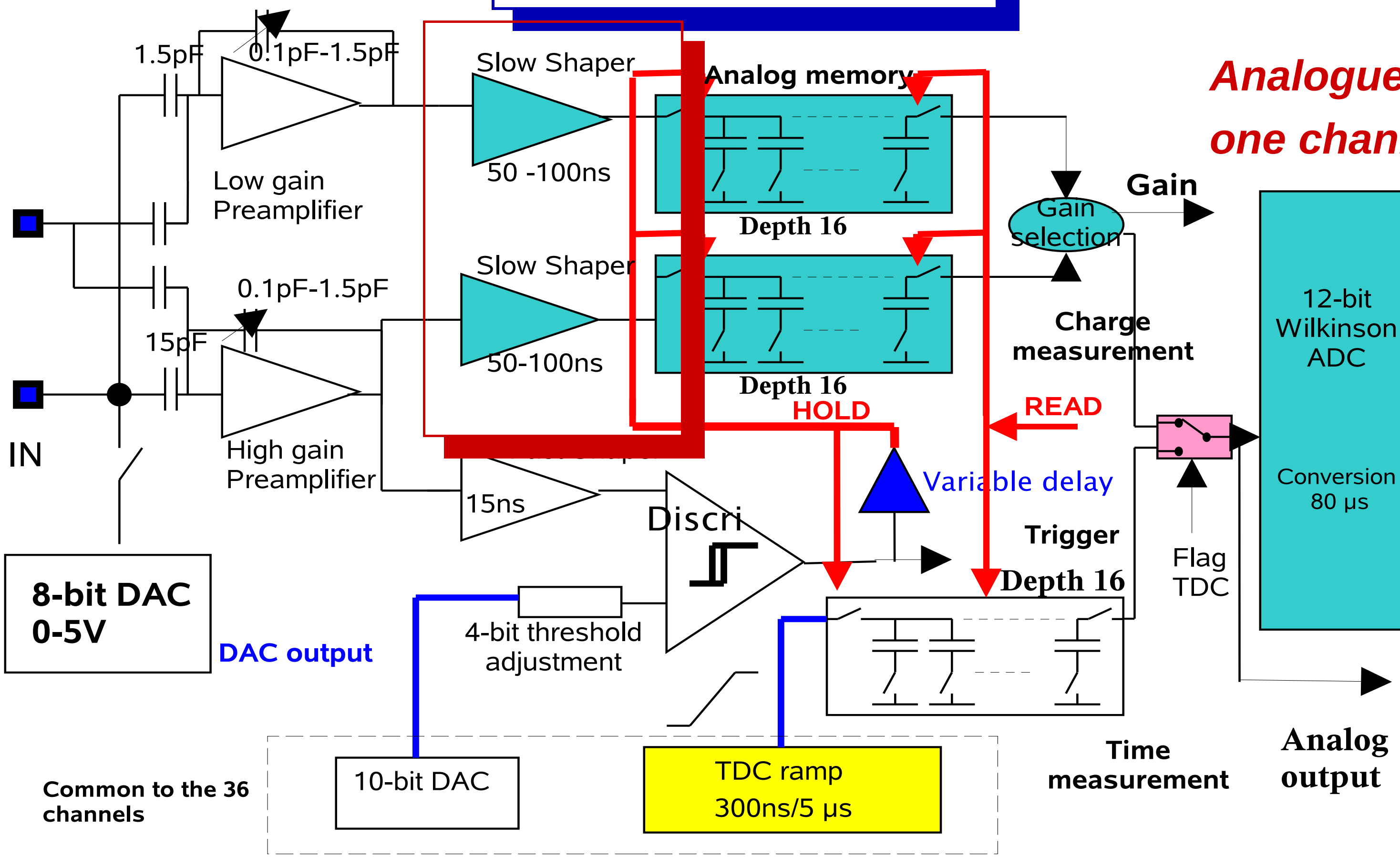
Analogue part: one channel layout



Separate channels for adjustable pre-amplification in low/high gain mode of input signal

SPIROC Chip

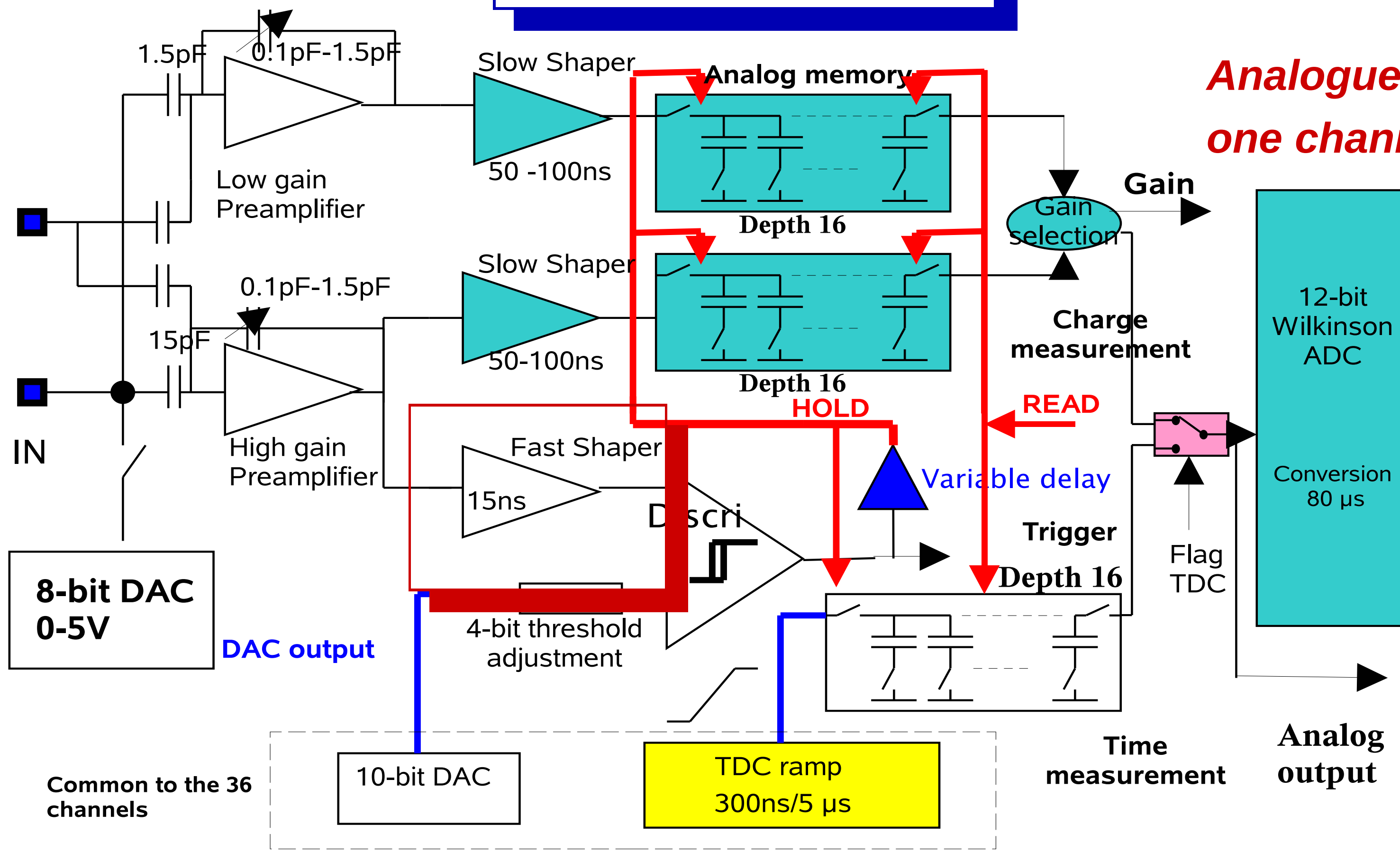
Analogue part: one channel layout



adjustable shaping time

SPIROC Chip

Analogue part: one channel layout



fast shaper for ...

SPIROC Chip

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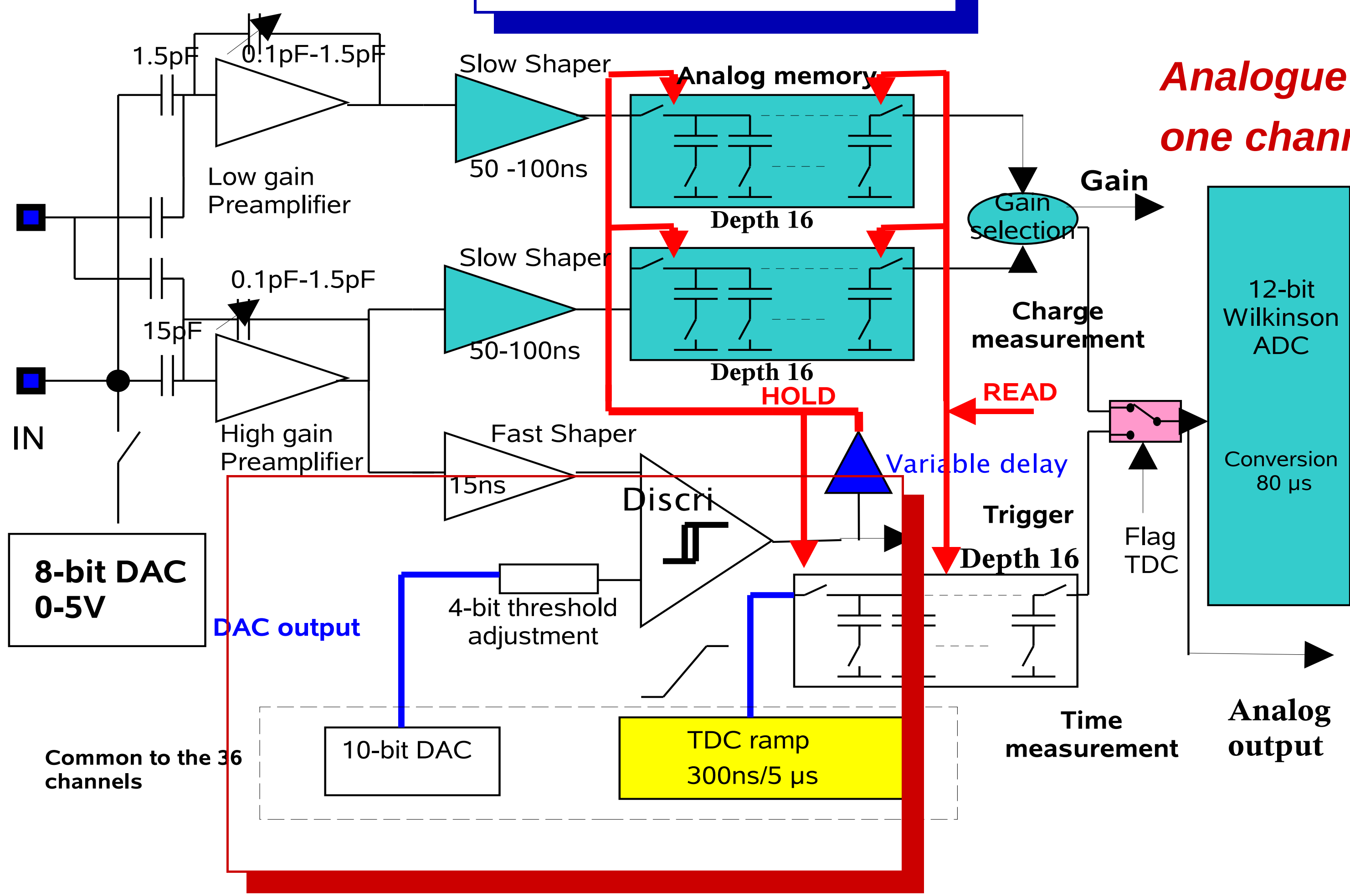

...autotrigger (to eventually hold the analogue shaped signal)

SPIROC Chip

Analogue part:
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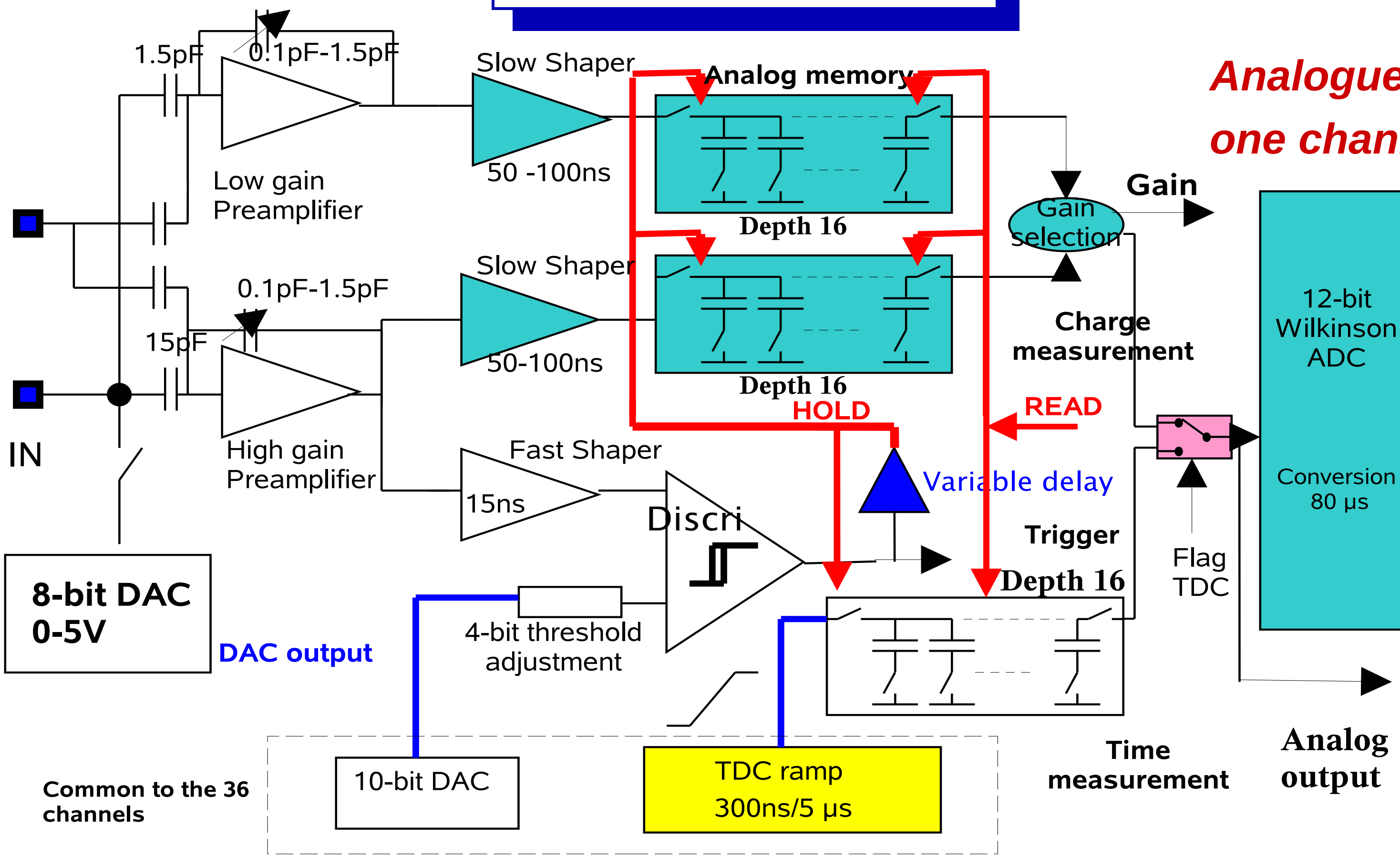
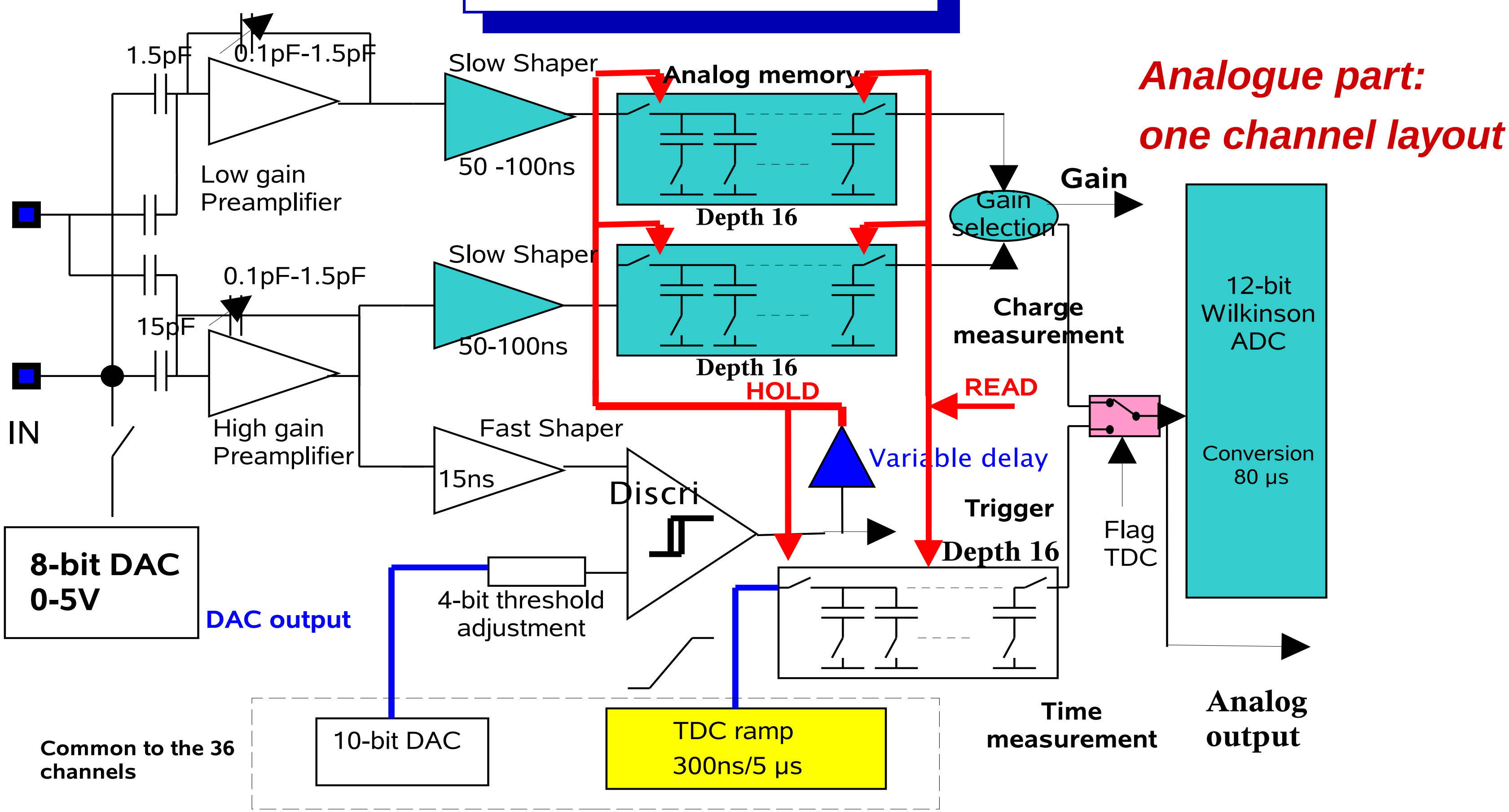


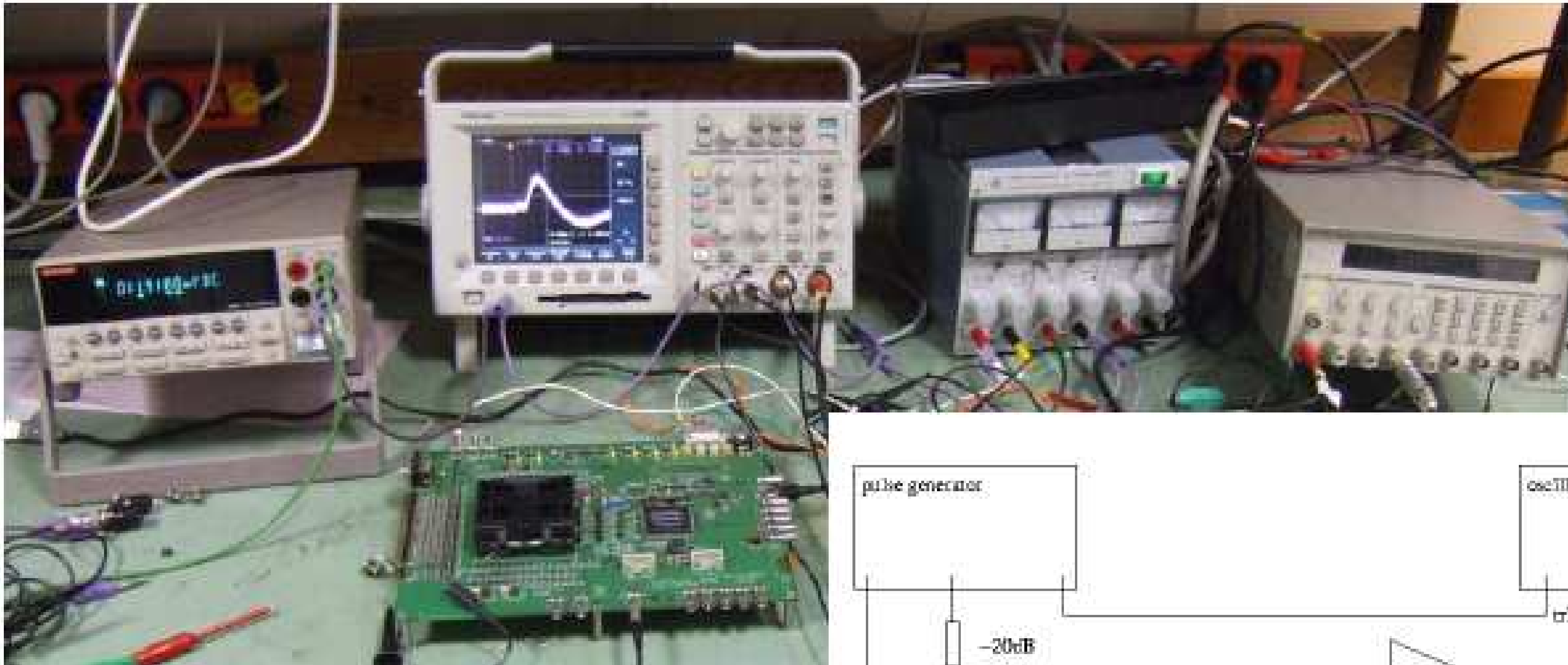
plus digital stage (not shown here) to synchronise acquisition/readout with ILC timing

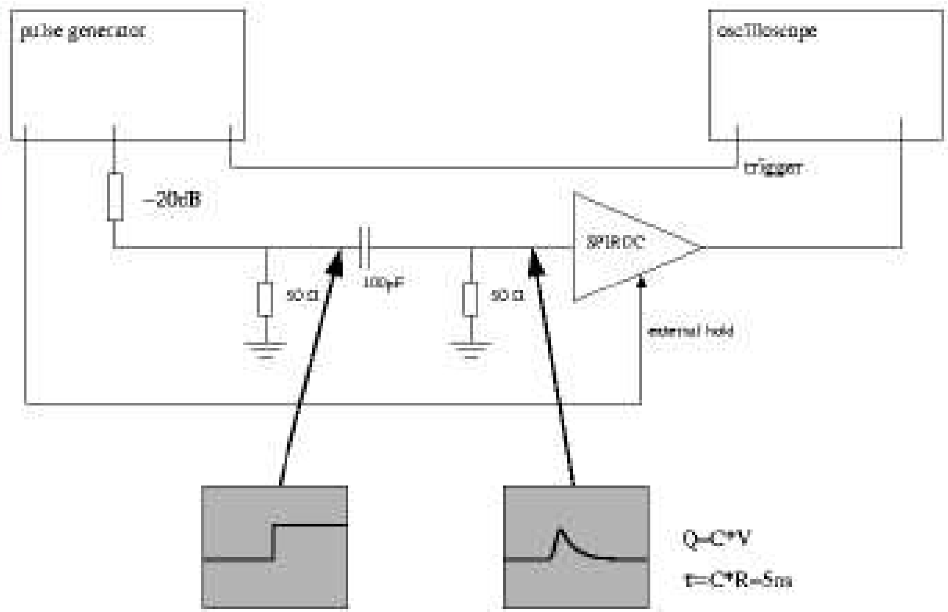
SPIROC Chip



- **Designed/developed by LAL (Paris)**
- **Should handle 36 input signals ($\longrightarrow 36$ SiPMs)**
- **Autotrigger: peak of input signal held by signal itself!**
- **Commissioning ongoing at DESY, with strong support from LAL and Heidelberg collegues**

Tests on SPIROC at DESY





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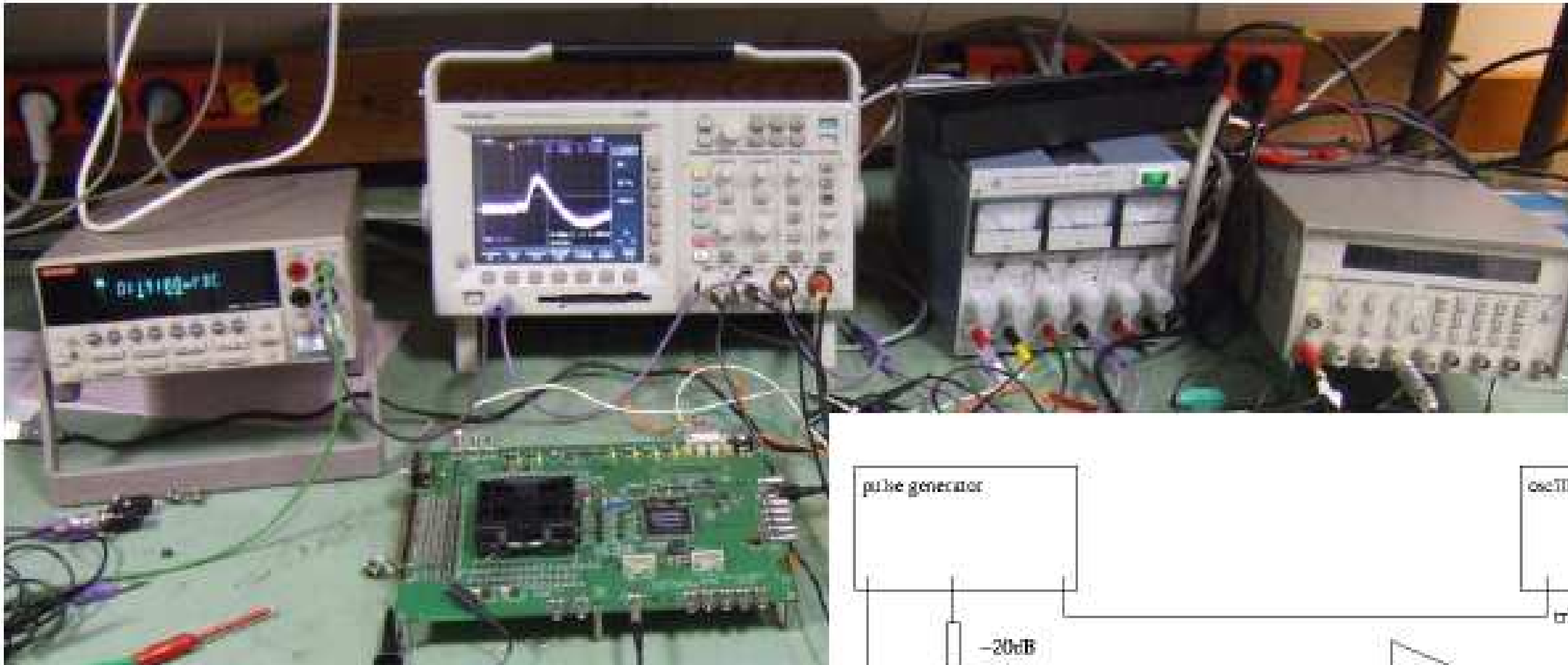
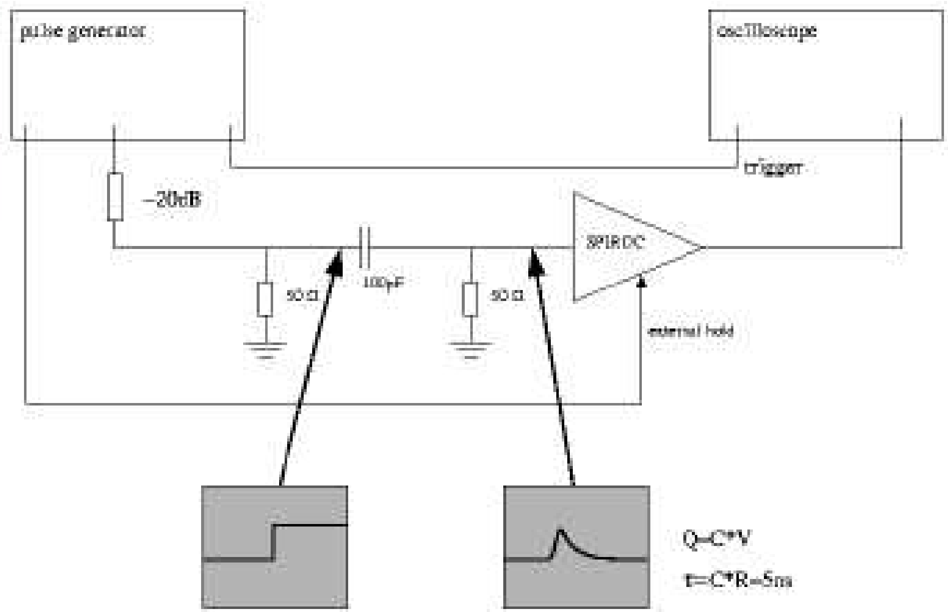
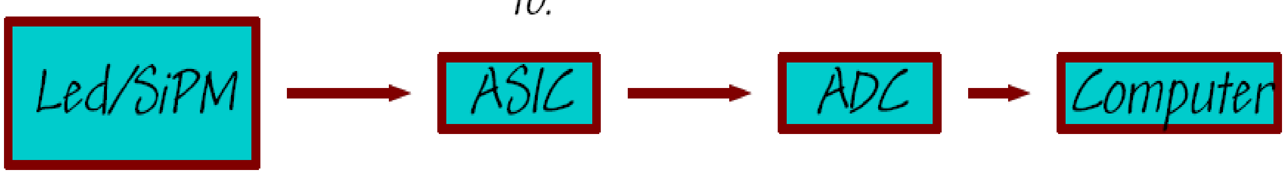




to:



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- **Linearity studies in low/high gain mode**

  $\Longrightarrow$ **at different shaping-time/variable capacitance**

Preliminary!

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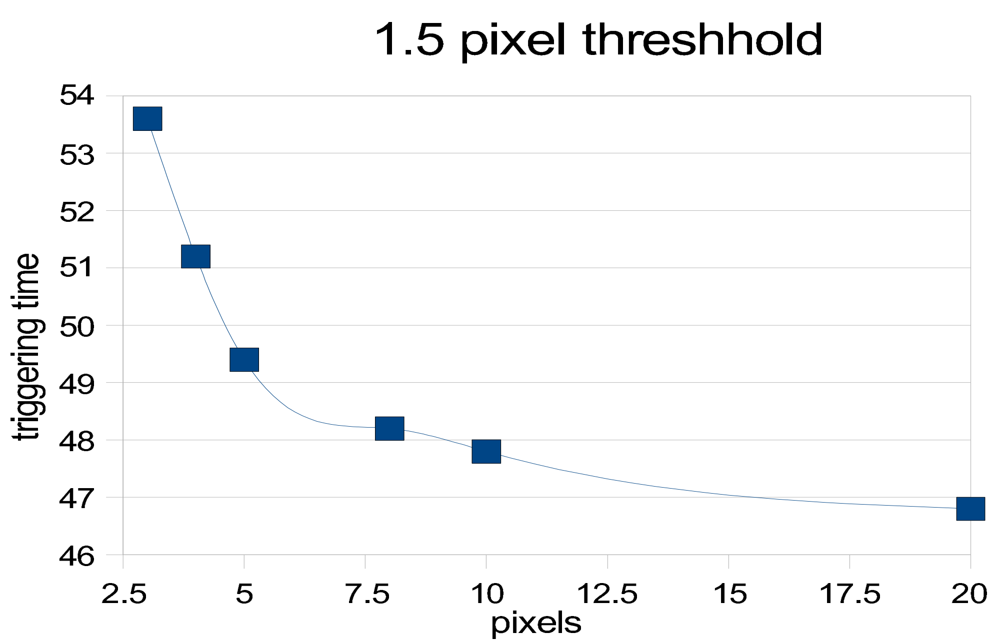

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- external trigger (to hold the signal)

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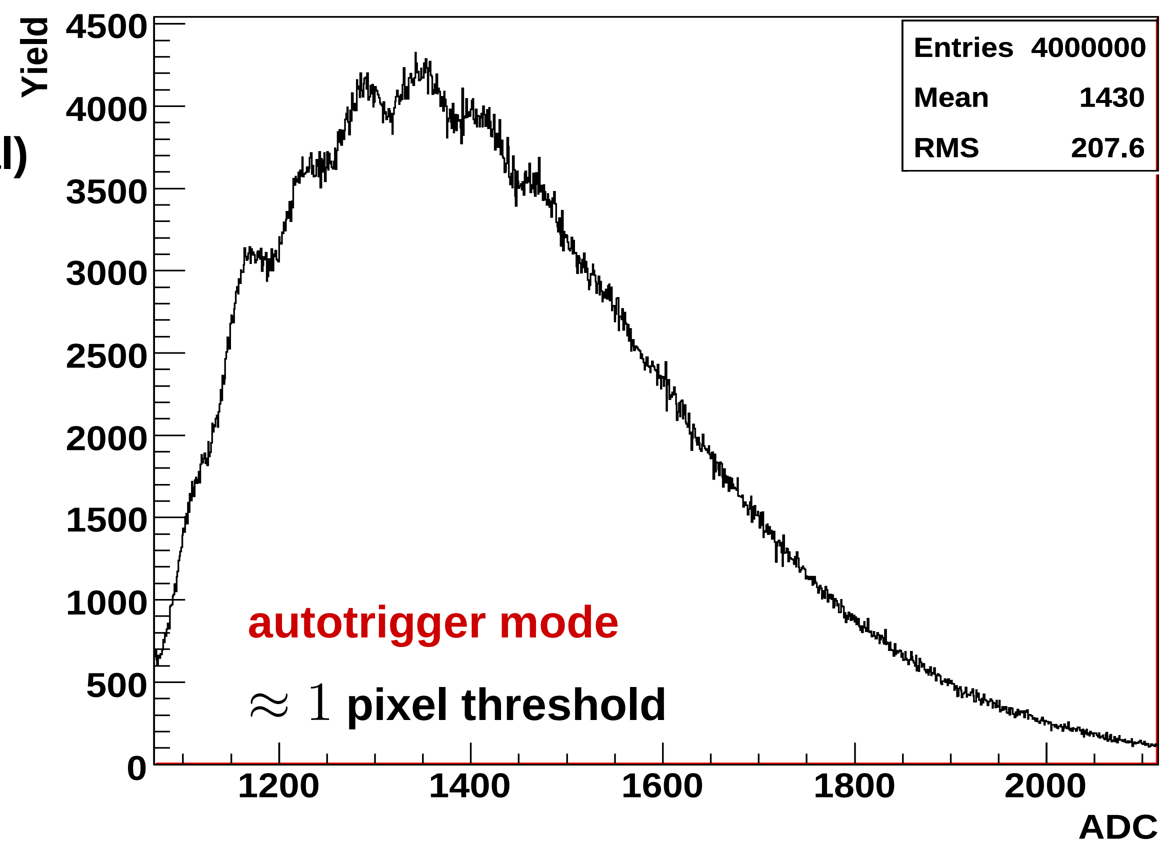
    $\Longrightarrow$ early to draw quantitative conclusions!



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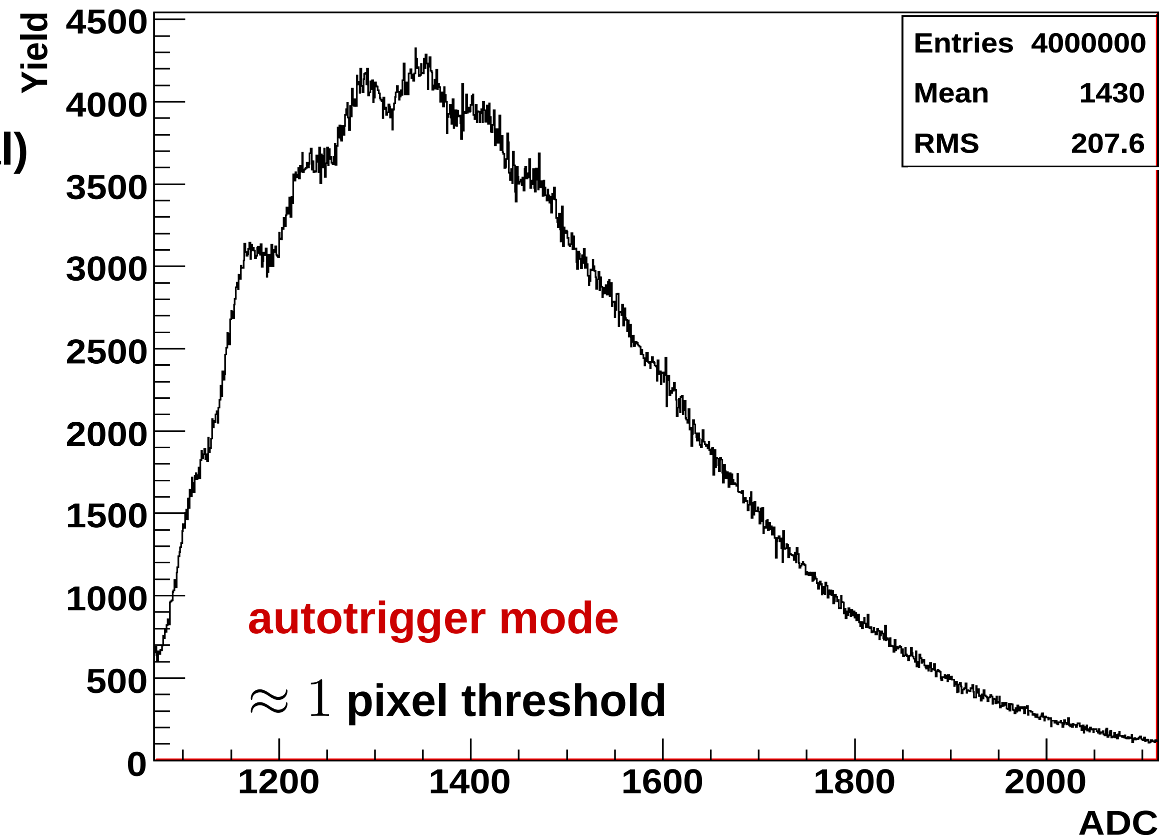
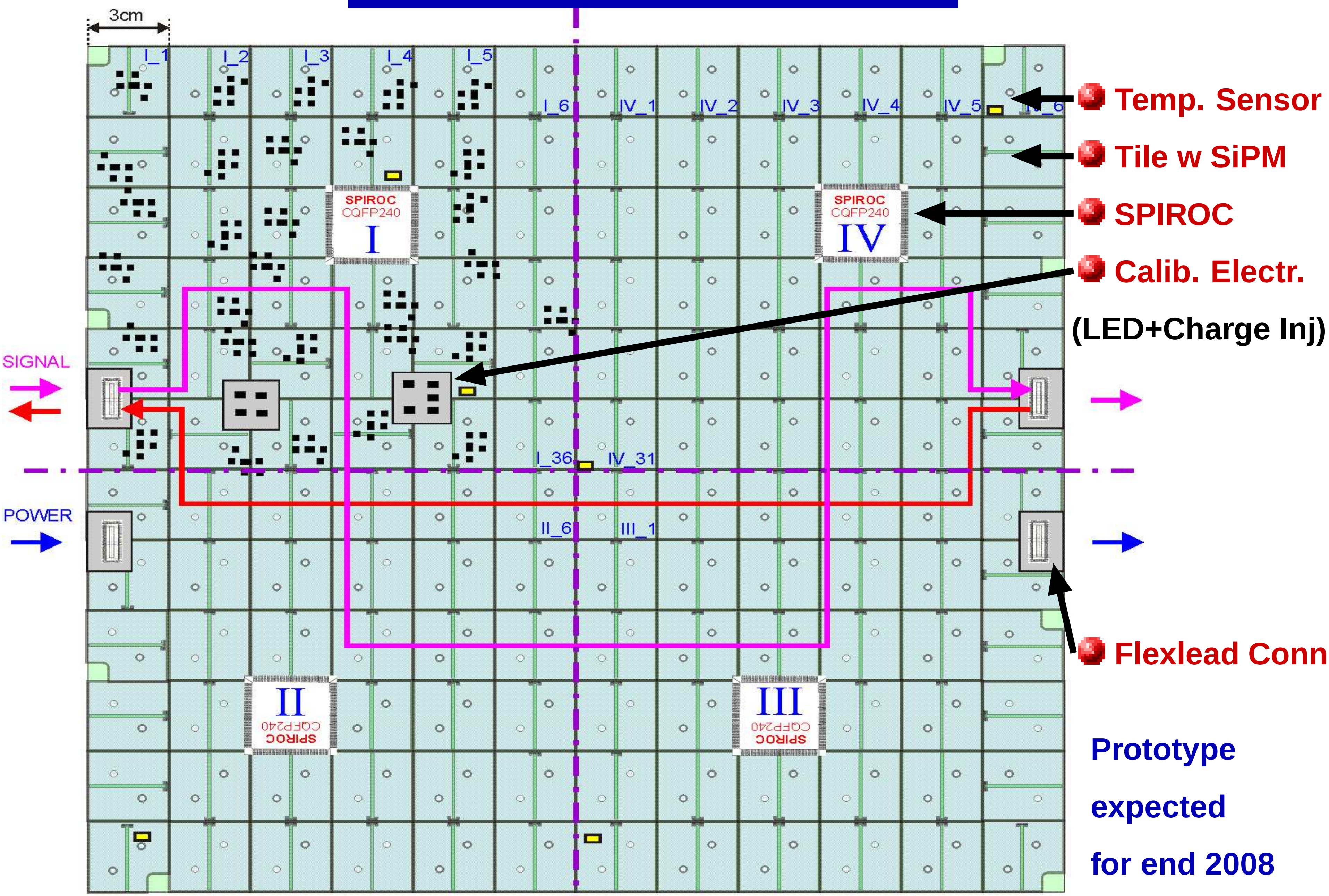


- **Improvement forseen when**
  - large jitter/time-walk understood
  - chip digital part (for autotrigger) fixed ($\longrightarrow$ SPIROC2)

HBU (HCAL Base Unit)



Prototype expected for end 2008

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Calibration system

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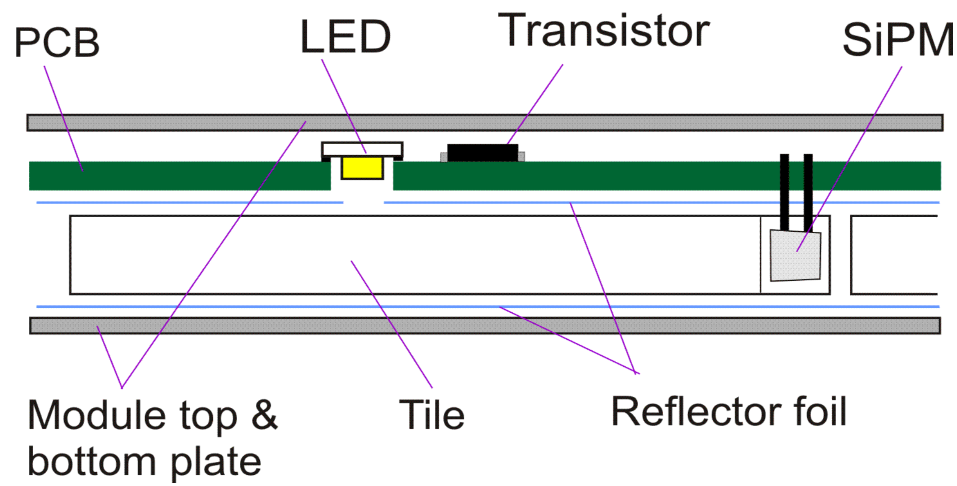
  $\Longrightarrow$ **Other option available from Praga group (see Polak's talk)**



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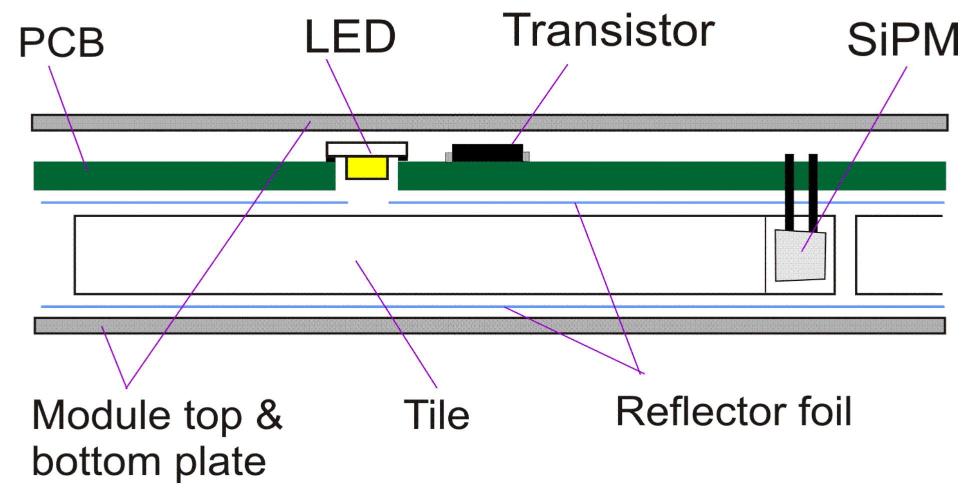

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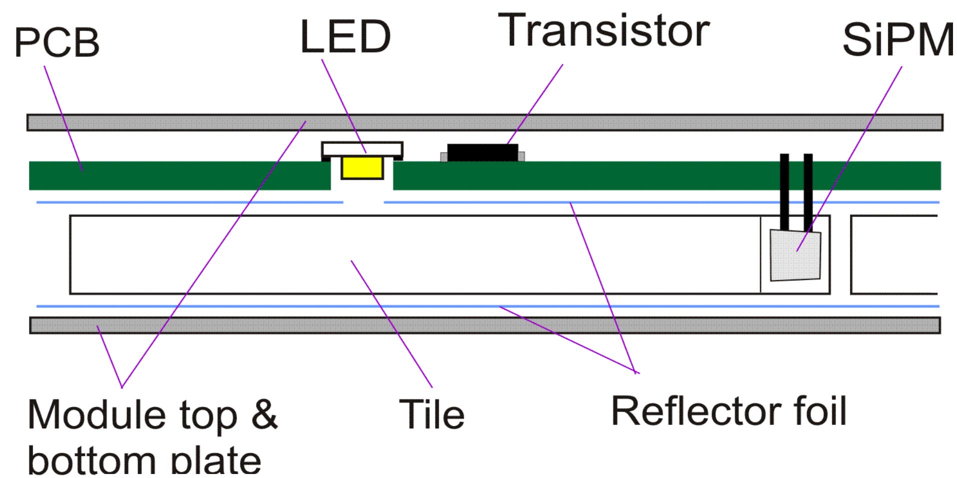

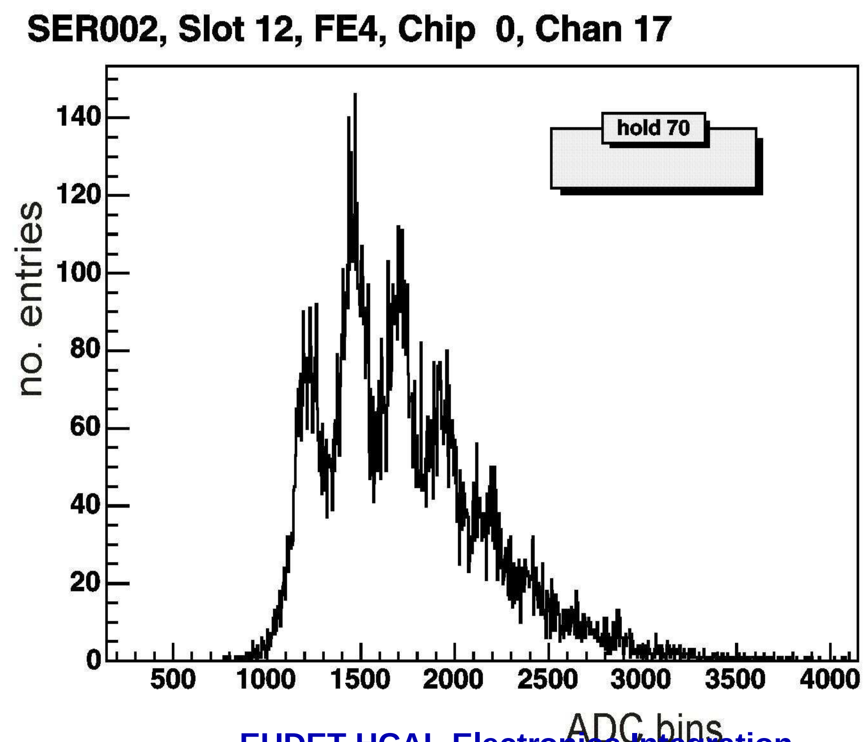

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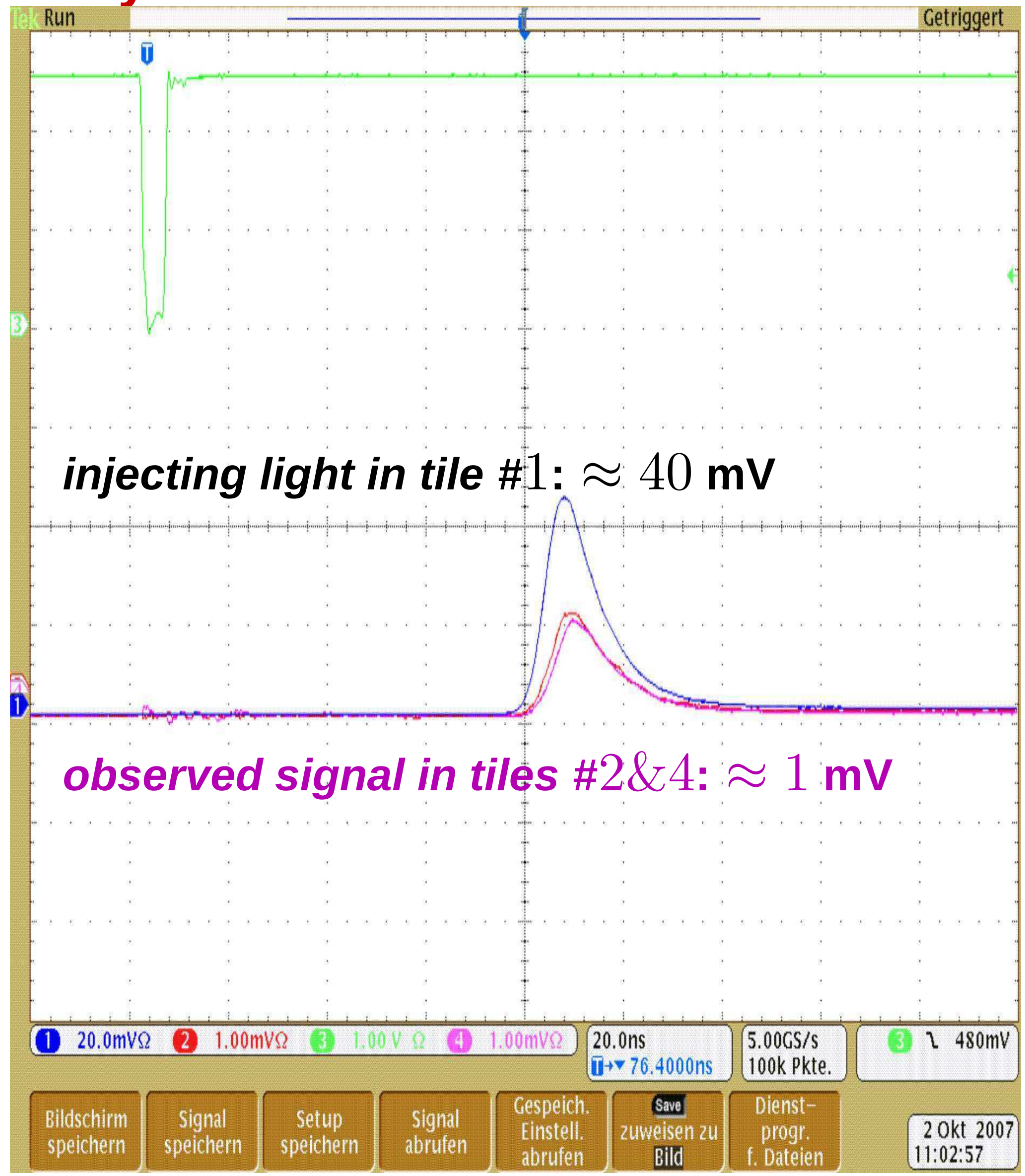
  - **cross-talk under investigation**

    cross-talk $\approx 2.5\%$

    $\Longrightarrow$ **possibly due to tile-tile coupling**



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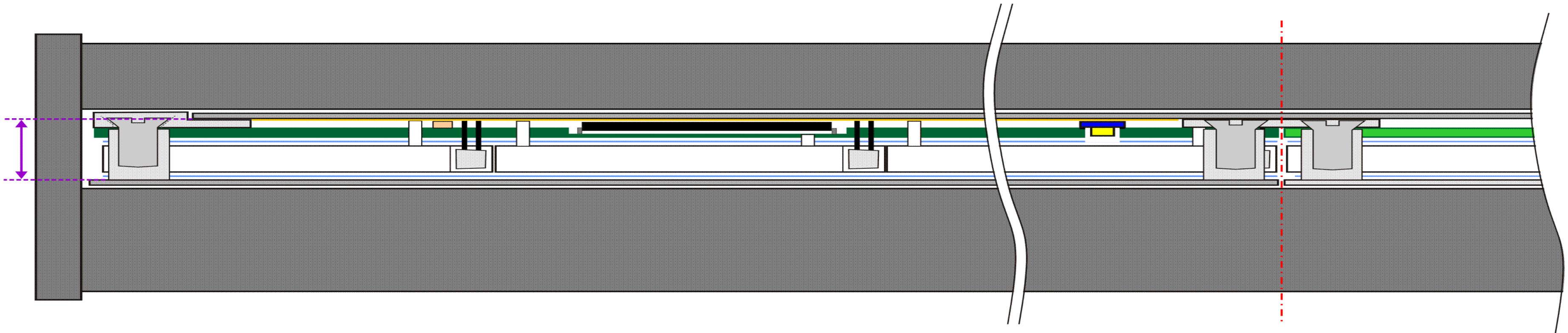

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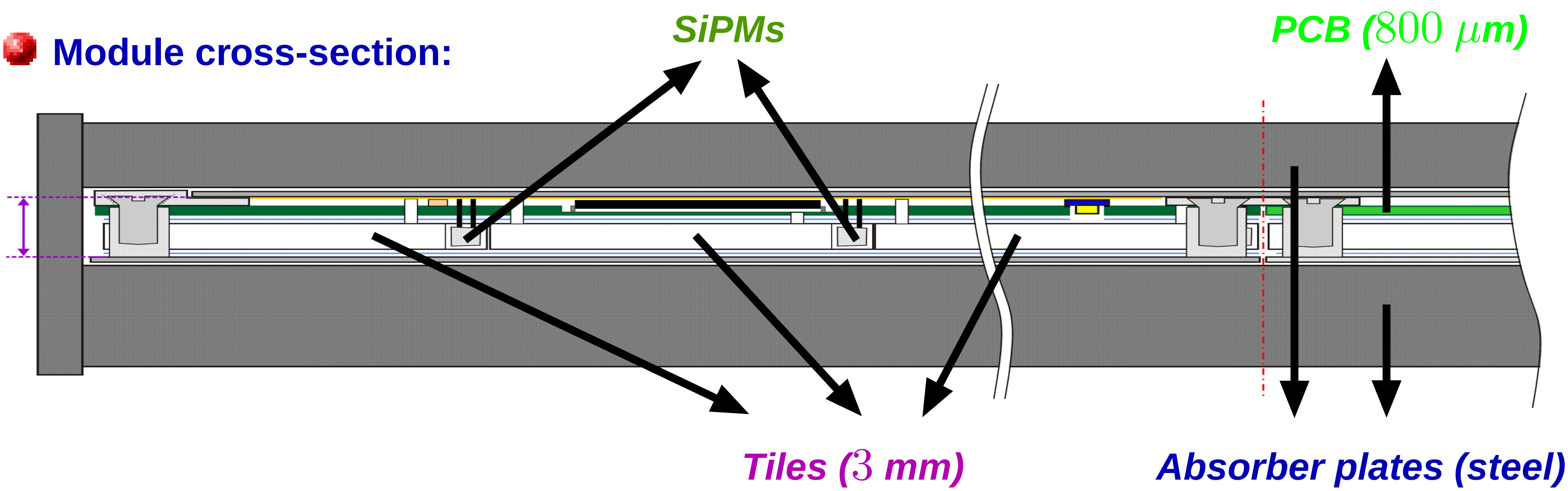

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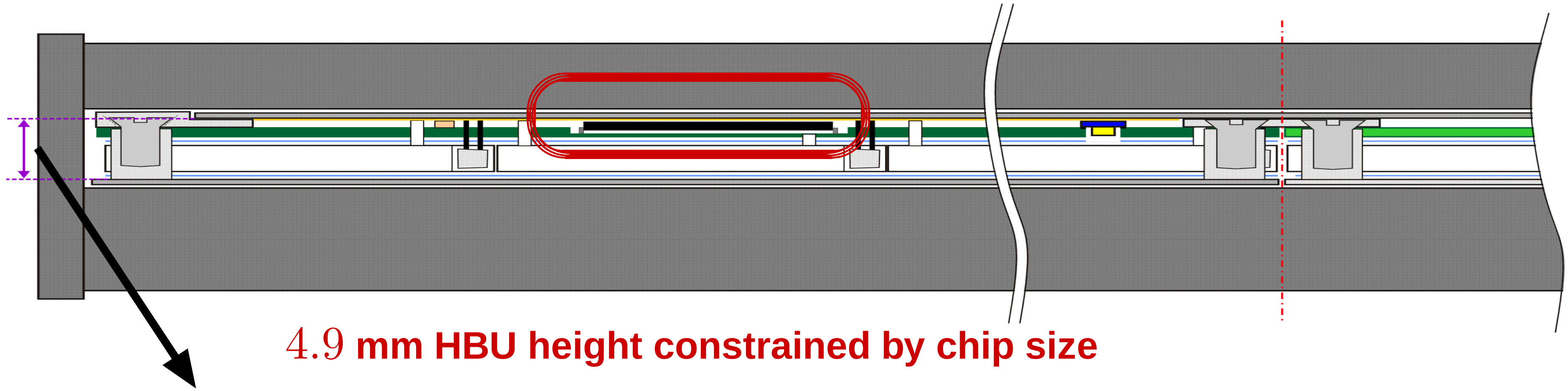

4.9 mm HBU height constrained by chip size

$\Longrightarrow$ reduction obtained using SPIROC2 (with height 1.4 mm)

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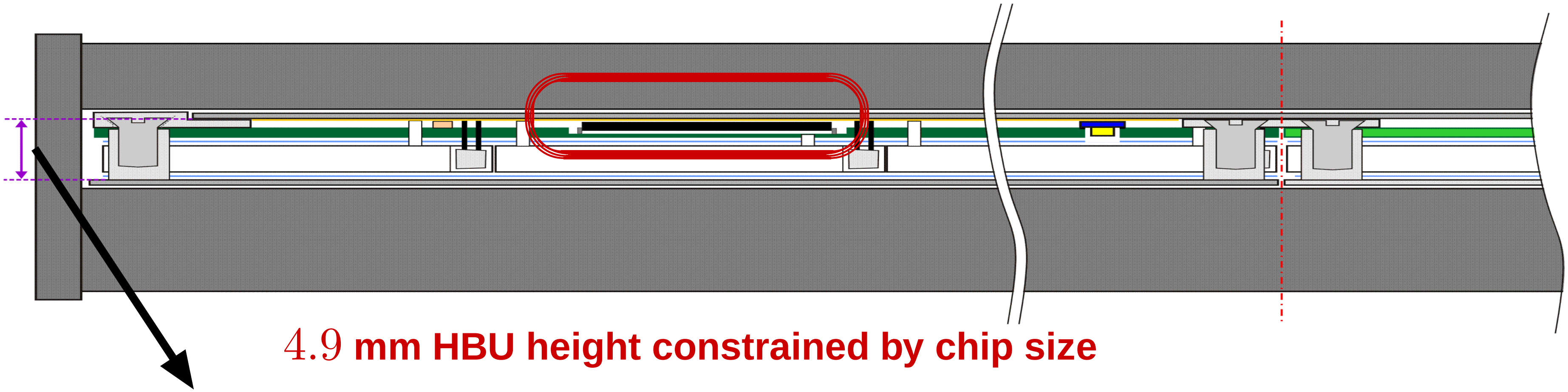

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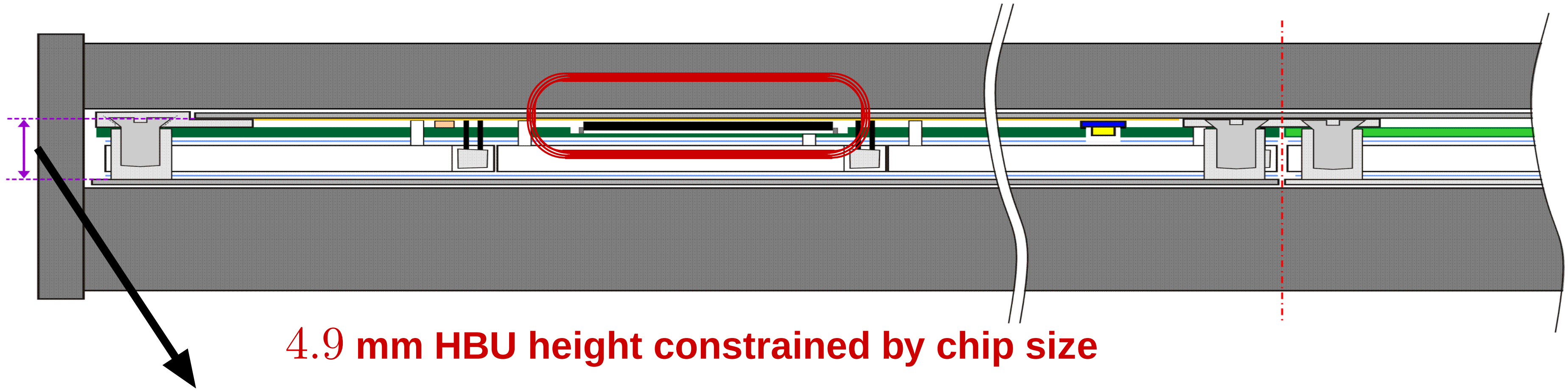

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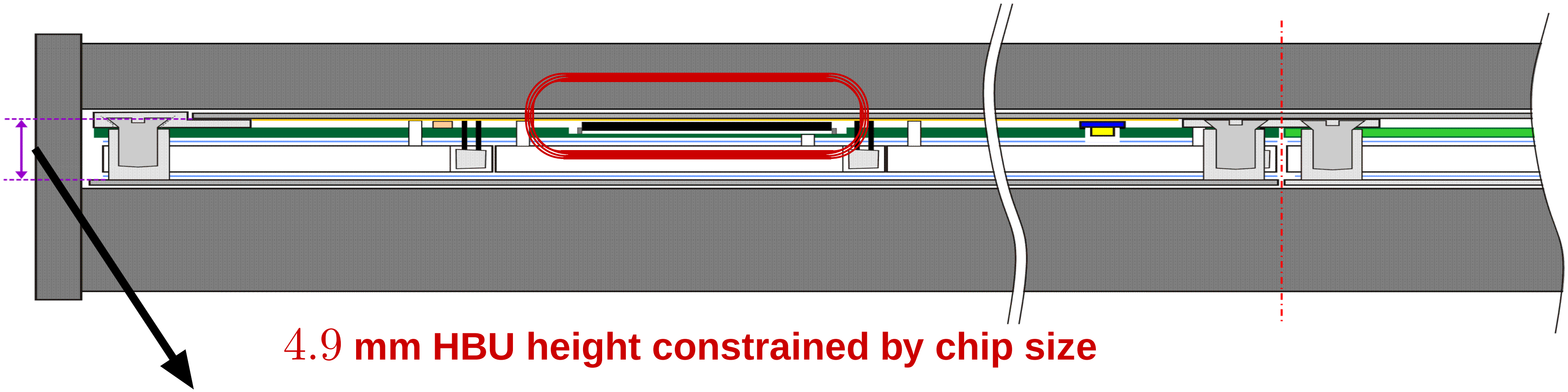

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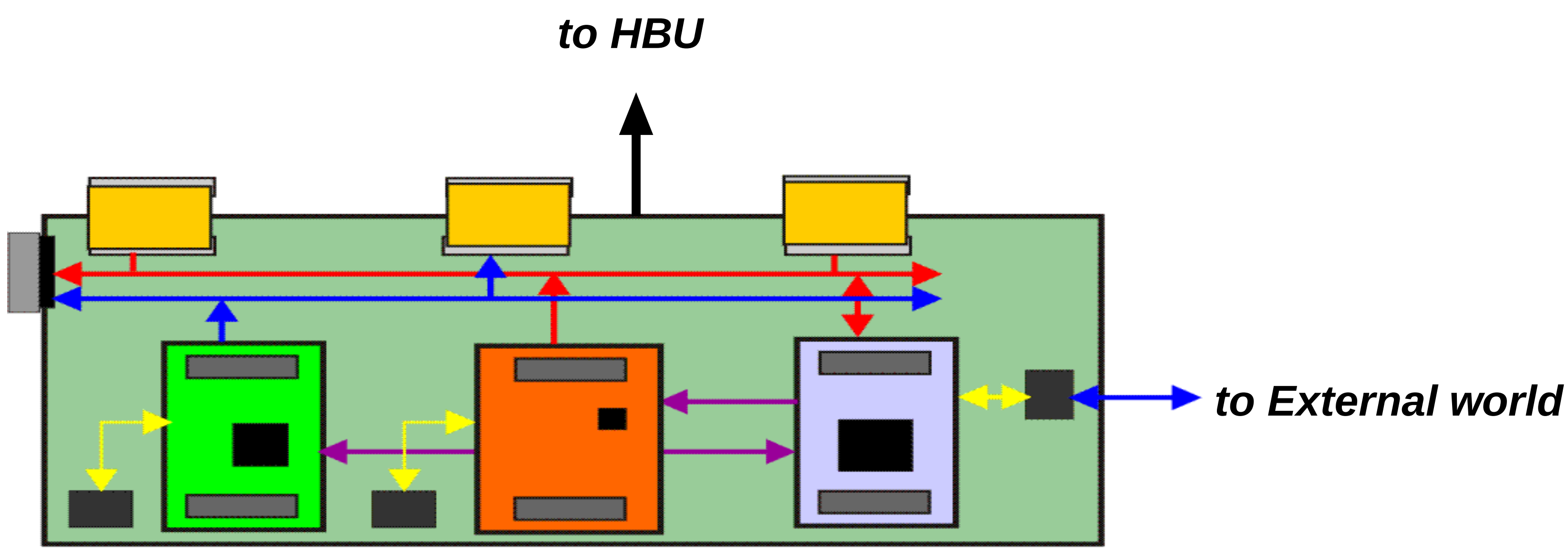
✔ **even more, considering calibrations done realistically only every few minutes**

HEB (HCAL Endcap Board)



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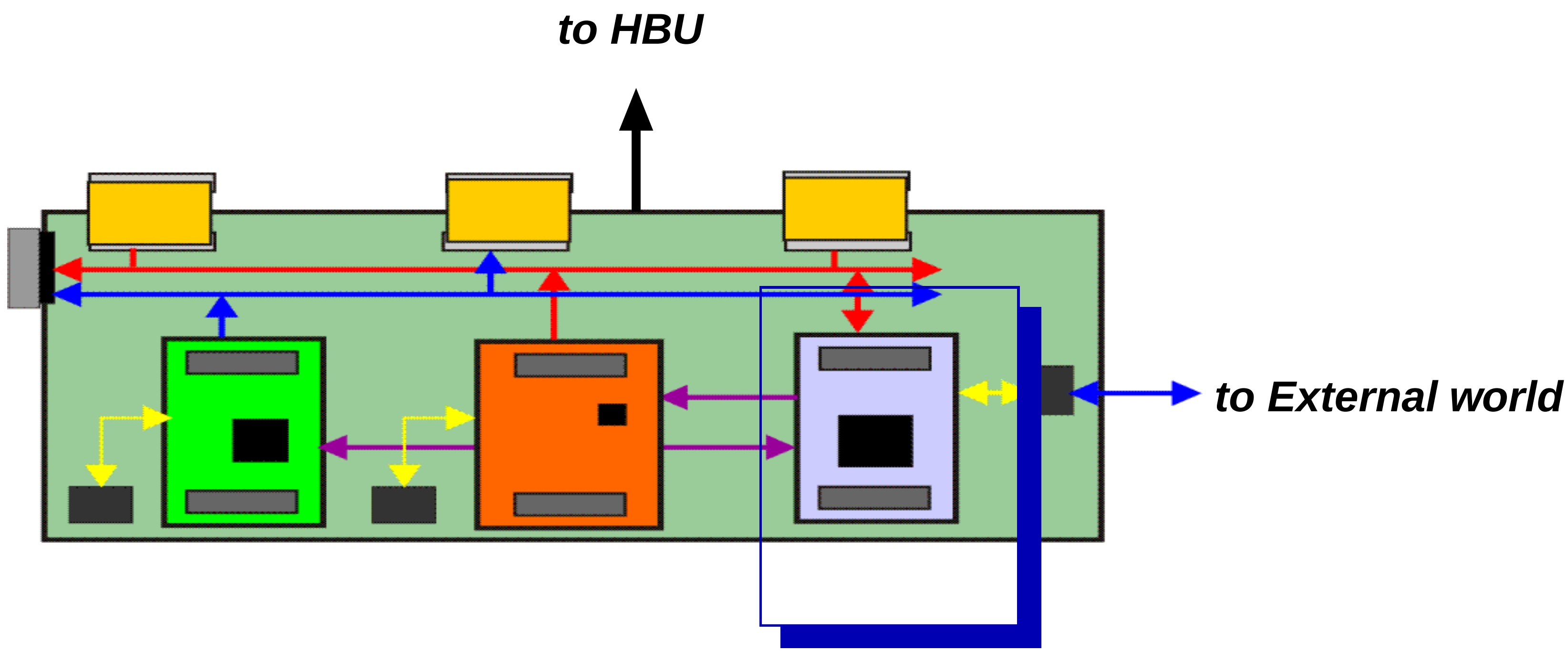

DIF module

— **External world ↔ HBU interface**

— **Readout/control of ASICs**

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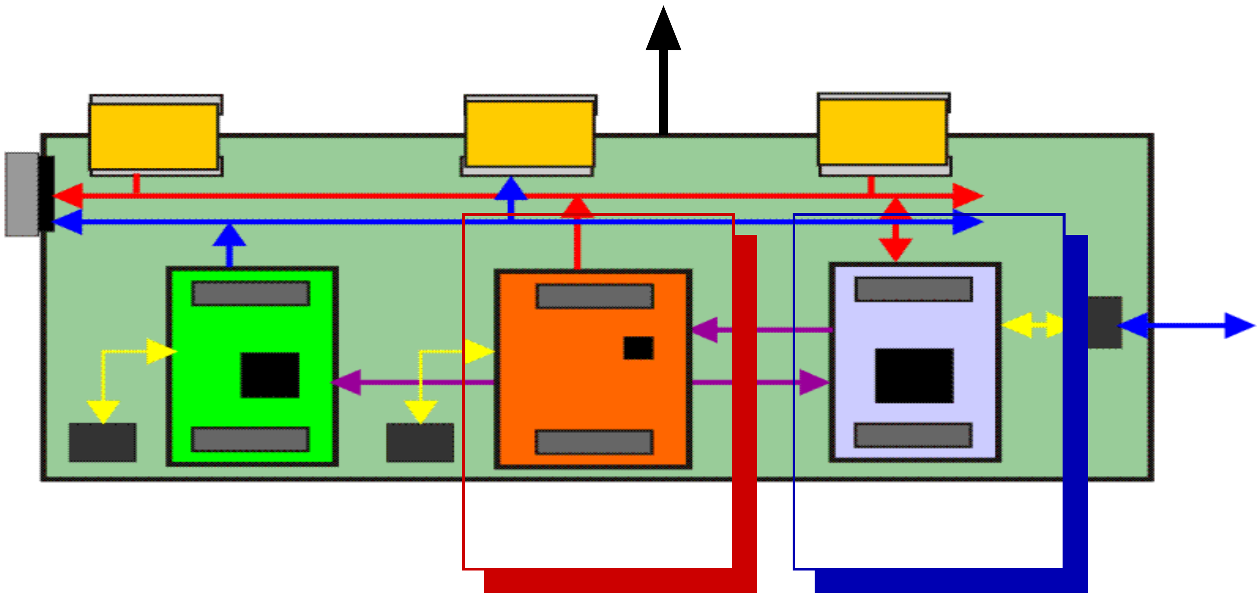

CALIB(ration) module

— Drives/regulates calibration electronics (LED + charge injection) inside HBUs

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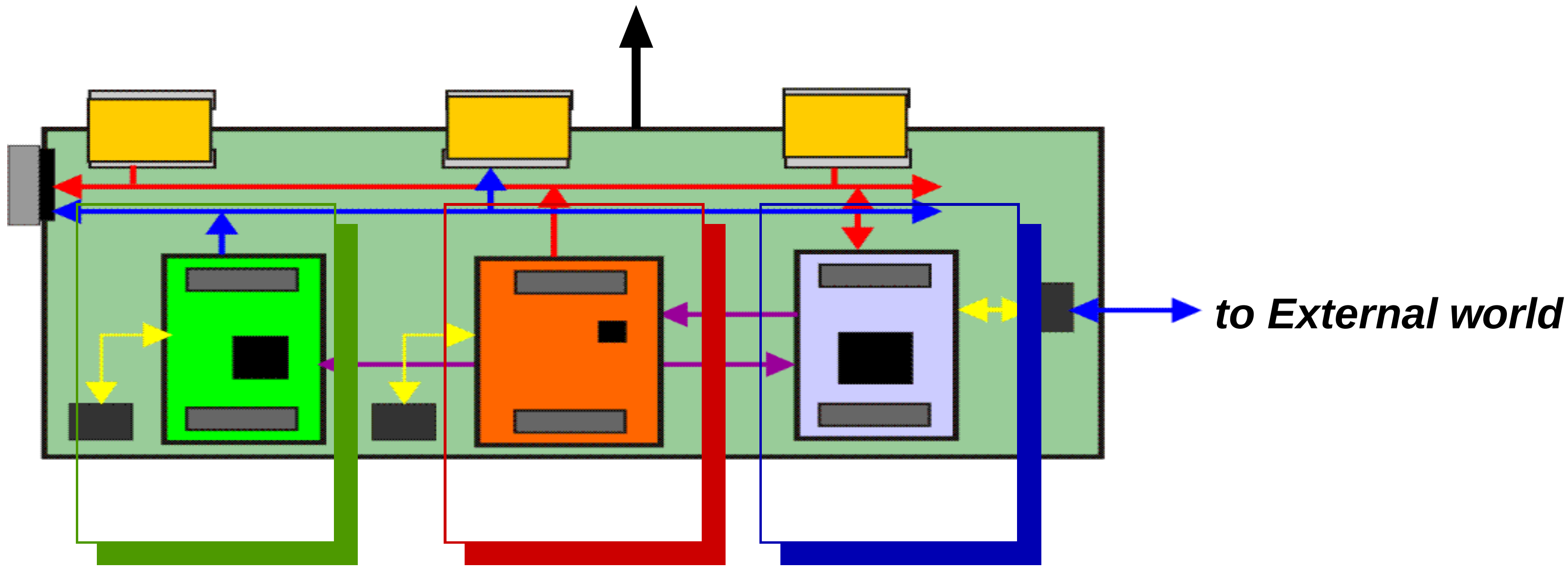

POWER module

— Provides $+3.5$, $+5$ V, bias voltages & ground to HBUs (and SiPMs therein)

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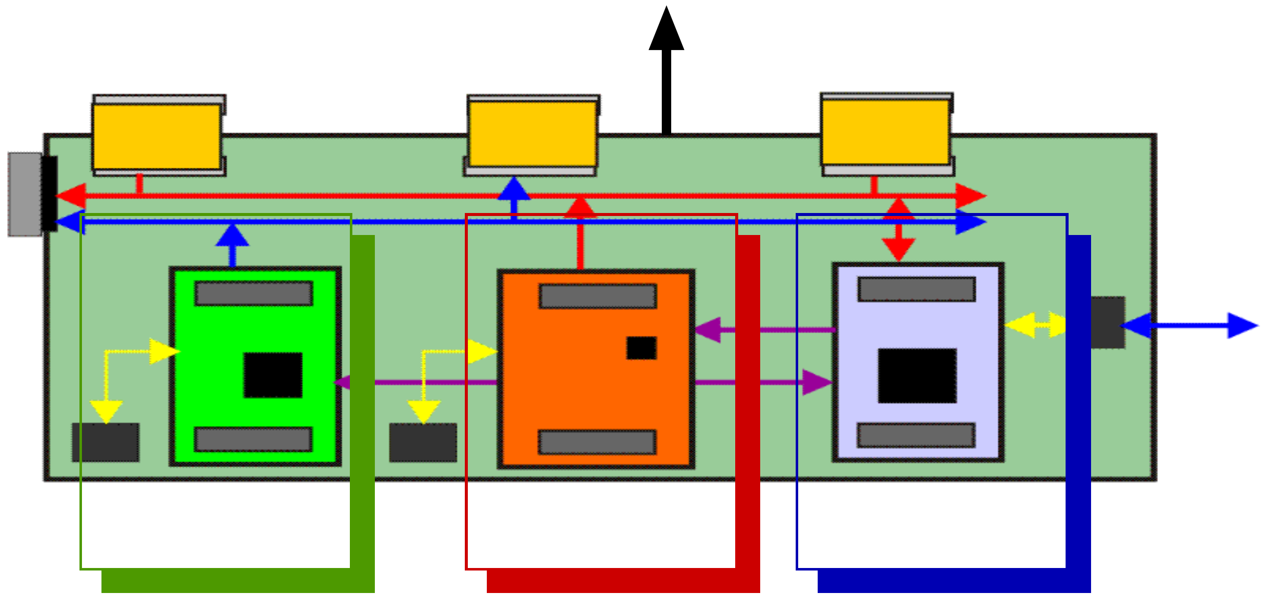

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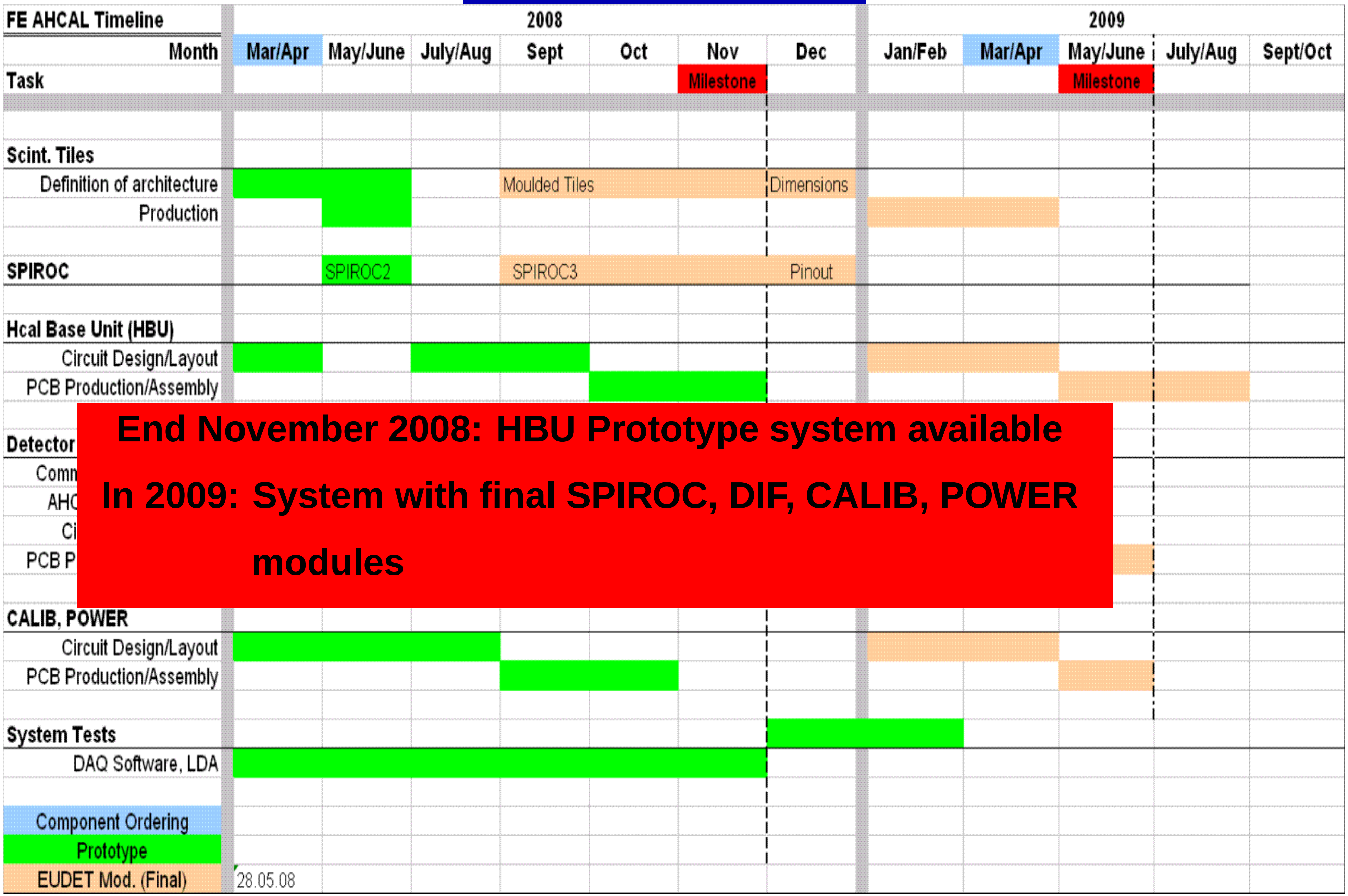
- Differently from HBU case, here cooling is forseen (it is located outside detector)

Time Schedule

Time Schedule



End November 2008: HBU Prototype system available

In 2009: System with final SPIROC, DIF, CALIB, POWER modules

Summary and Outlook

- SPIROC (to readout) commissioning on going
  - ⟹ DESY+Heidelberg+LAL sinergy
  - ⟹ SPIROC2 design done; chip expected for end 2008

- Elecronic unit HBU design in advanced stage
  - ⟹ module size driven by SPIROC height (reduced with SPIROC2)
  - ⟹ power dissipation optimized
    - — switching off SPIROC/calibration electronics when not needed

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- Time schedule for design and production of component prototypes ready

  ⟹ first version of all components expected by end of 2008

  ⟹ final version of system expected within 2009

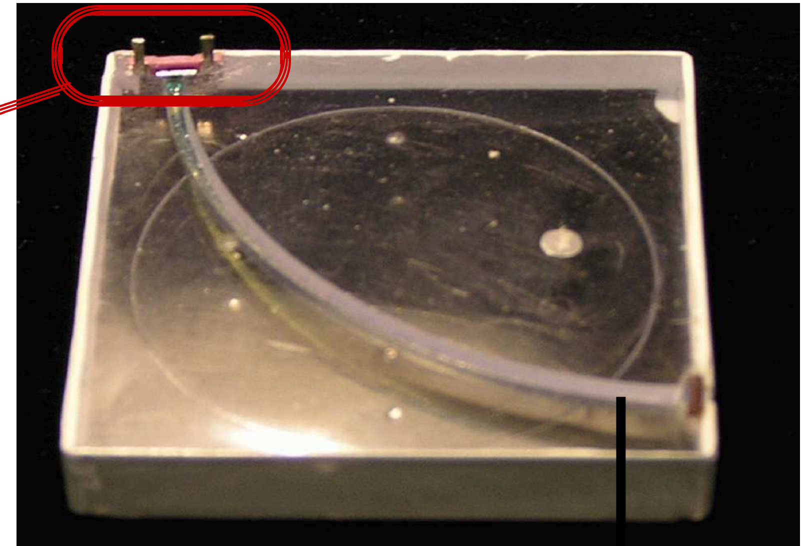
Back Slides

SiPM/Scintillator Characteristics

SiPM: novel multi-pixel photo-multiplier

operated in Geiger mode

$\Longrightarrow$ B-field proof, small



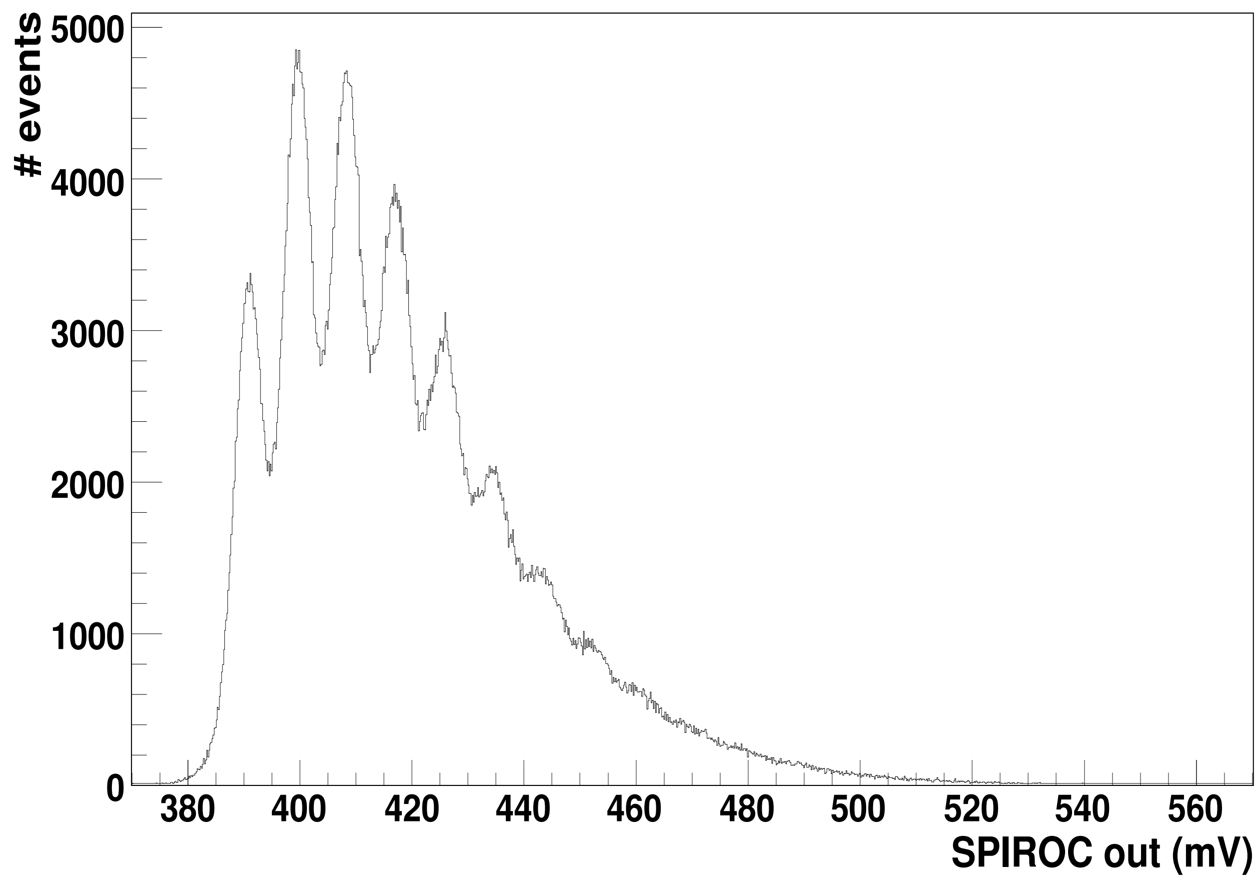
Optimization of scintillator size to $3x3$ cm^2

$\Longrightarrow$ confirmed by Monte Carlo simulation

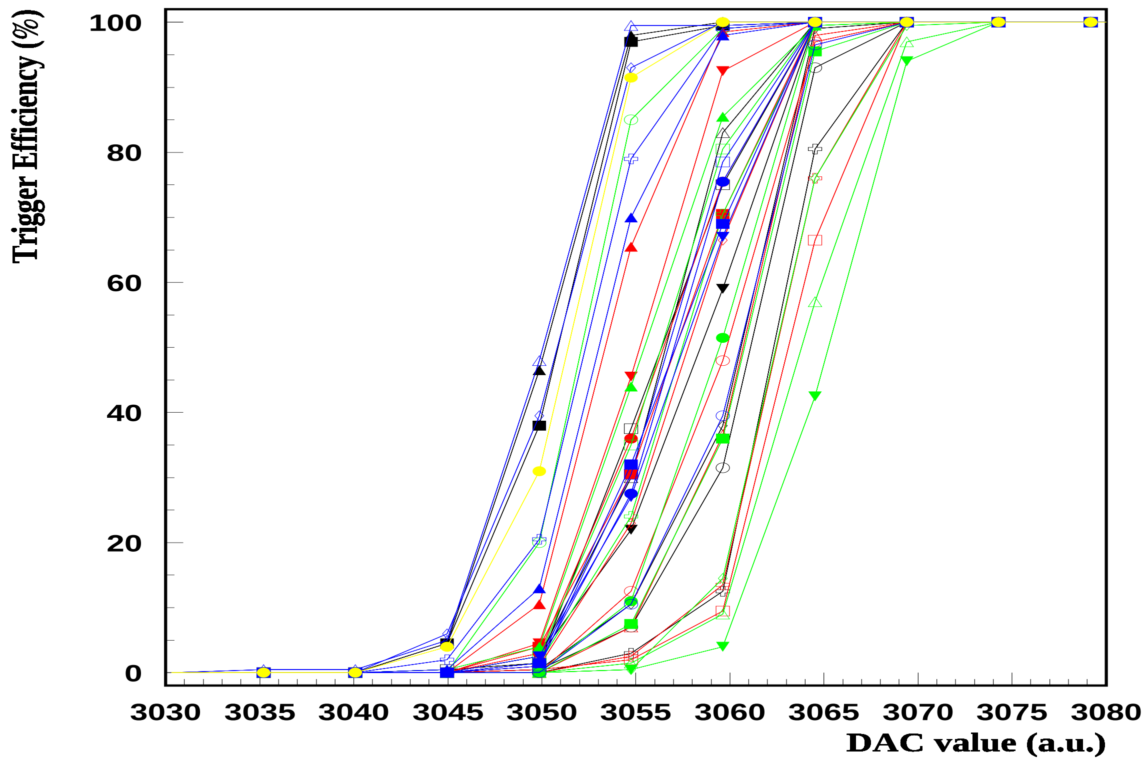
Wavelength shifter

SiPM: Single-peak spectrum with External Trigger

- **SiPM Nr. 753**
- **SPIROC operated in HG mode with $100fF$ variable capacitance and $25ns$ shaping time**
- **external hold (from pulse generator)**

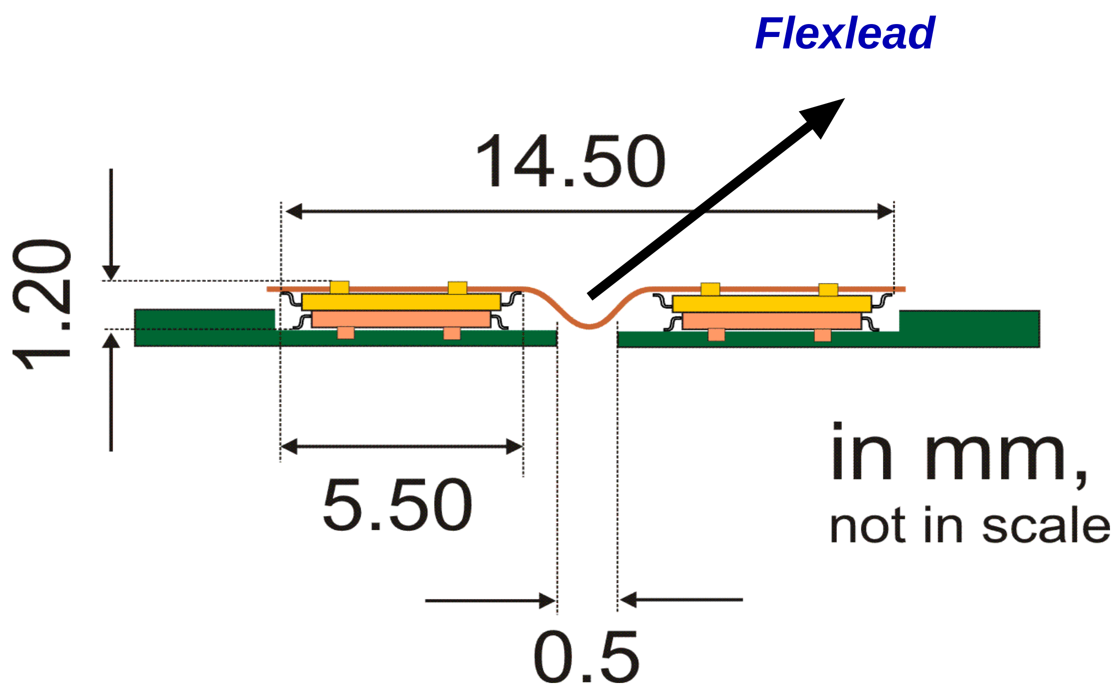


SPIROC: Noise Measurements



- Noise measured for all 36 input channels, separately, by counting the trigger efficiency while decreasing the voltage reference at the discriminator in SPIROC

HBU-HBU Interconnection



- **Flexlead:**
  - **– rigid at connector (80 pins) sides**
  - **– flexible in between HBUs**
  - **– bended flexlead allows HBU-HBU displacement of $\pm 100\mu$m**