# Development of FPCCD Readout ASIC

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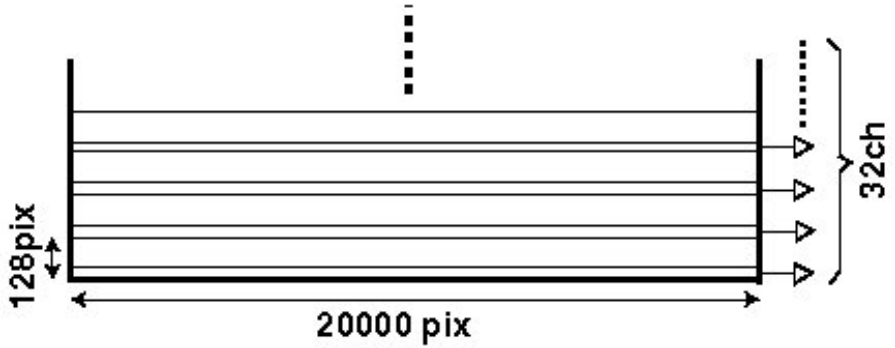
# Introduction

## FPCCD vertex detector

- Pixel size : 5μm
- Thickness : 15μm
- Signal level : <2000e
- Readout channel : 16 or 32 ch
  - ~20,000 x 128 pix/ch

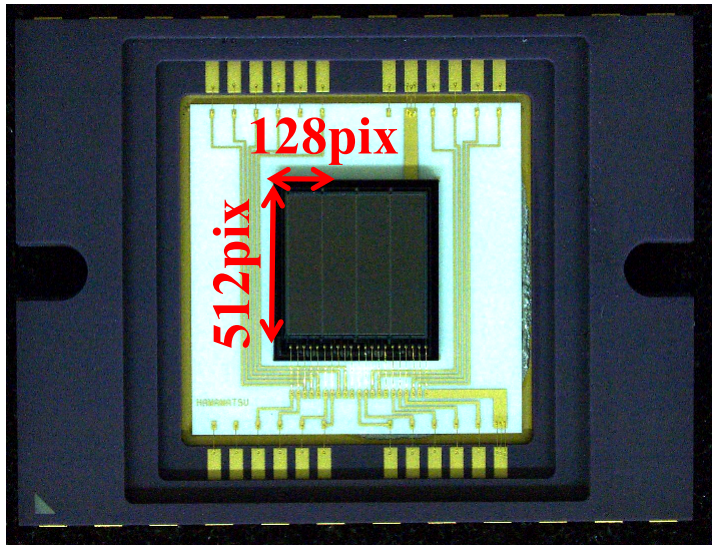



**Test-sample was delivered in Mar., 2008.**

- Pixel size : 12μm
- Readout channel : 4ch
  - 512 x 128 pix/ch

Development of the readout ASIC was started.

**Picture of FPCCD test-sample**



# Requirement to the readout ASIC

## Requirement to the readout ASIC

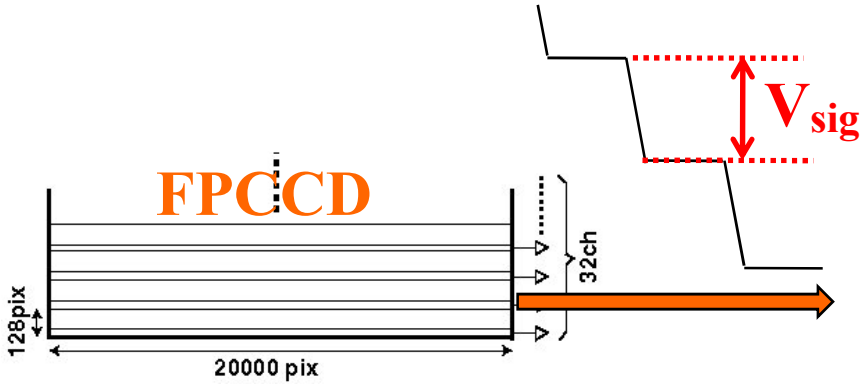
- All elements to read from FPCCD are contained in one chip.
- Readout rate : >10 Mpix/sec
  - [20000 x 128 pix]/[0.2 s]
- Noise level of the ASIC : < 30 electrons
  - Required total noise level including the CCD : <50 electrons
  - Noise level of FPCCD : ~30 electrons
- Power consumption : < 6 mW/ch
  - The power consumption in a cryostat should be <100 W.
  - Required total power consumption : <16 mW/ch (~100W/6000ch)
  - CCD : ~10mW/ch

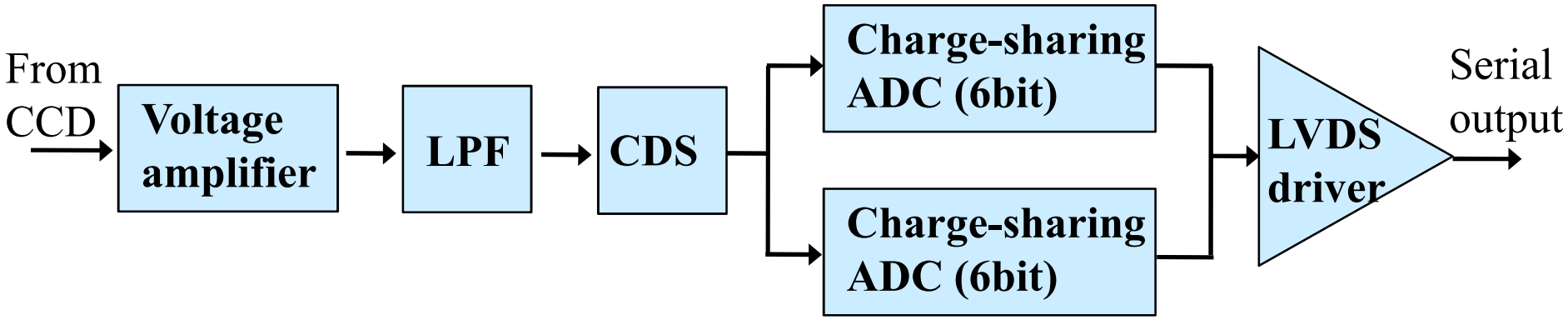
To achieve these requirement, readout ASIC was designed.

# Design concept of readout ASIC

## ASIC elements

- Voltage amplifier
- LPF (Low-pass filter)
- CDS (Correlated double sampling)
- ADC
  - 2 charge sharing ADC are used alternatively to achieve 10Mpix/sec.
- LVDS driver



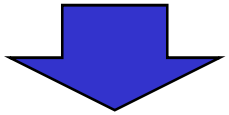



# Expected performance

## Expected performance

- Readout rate : 10 Mpix/sec ⟶ **OK!**
  - Data conversion rate : 10MHz (= 5x2 MHz)
  - 260 ms/ch : [20000 x 128 pix/ch] x [$10^{-7}$ s/pix]
- Power consumption < 5 mW/ch ⟶ **OK!**
  - Charge-sharing ADC realizes low power. (~10 μW)
- Noise level : ~10e ⟶ **OK!**
  - Estimation with SPICE simulation.

**The performance will satisfy our requirement.**



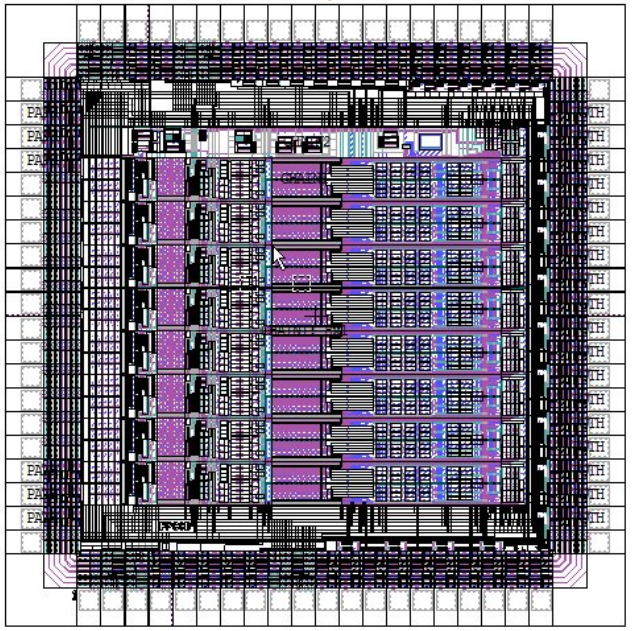
The prototype of the readout ASIC was produced.

# Readout ASIC

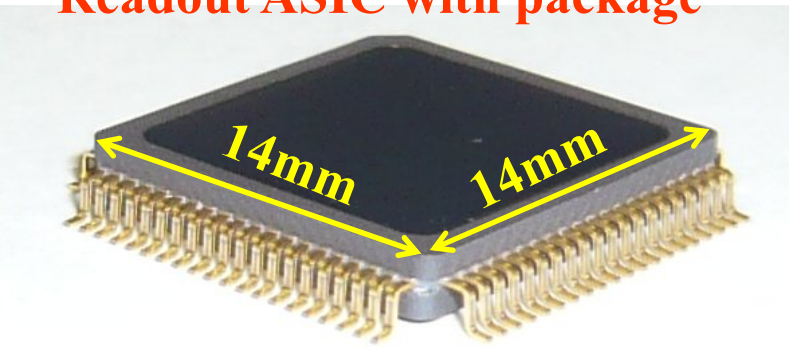
## Readout ASIC prototype

- The readout ASIC was delivered in Jan., 2008.
- The chip was produced by MOSIS.
  - Size : 2.85 x 2.85 $mm^2$
  - # of pad : 80
  - Readout channel : 8
- The chip was covered by QFP-80pin package.

ASIC layout



Readout ASIC with package

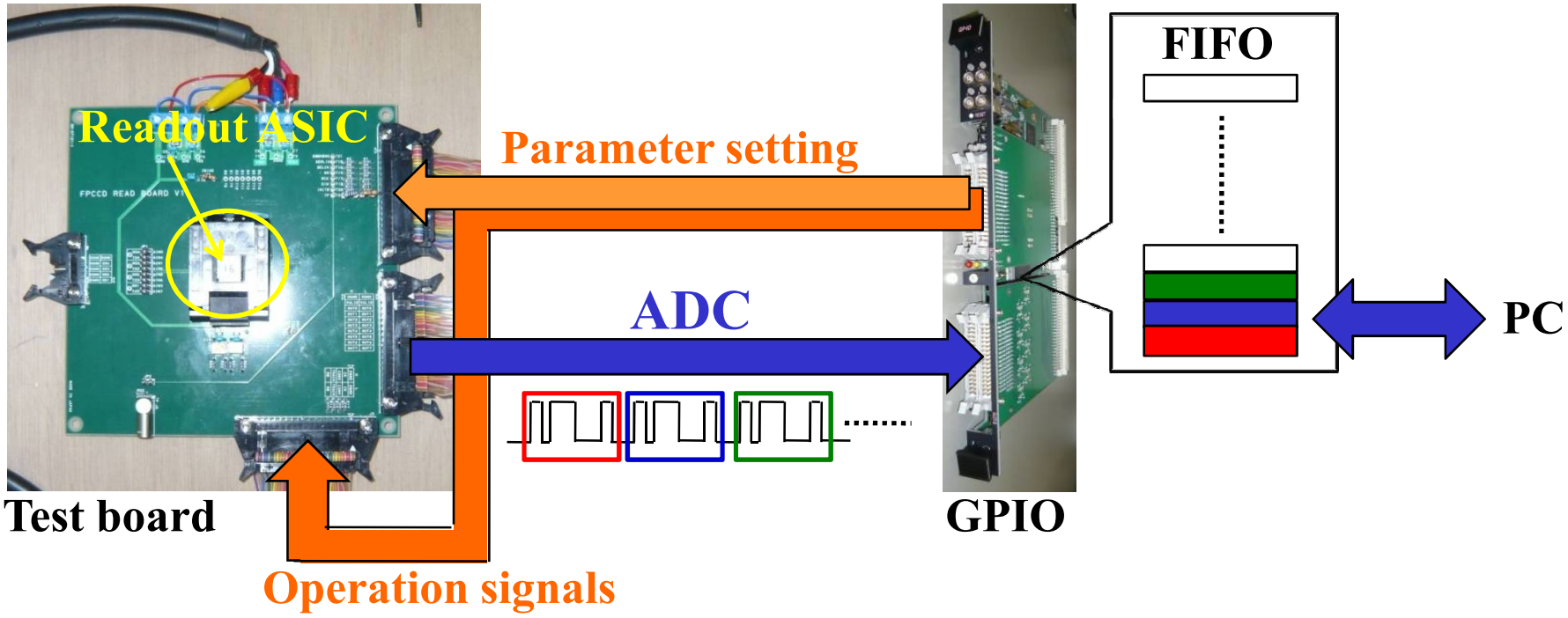



Readout system was constructed to perform the response test.

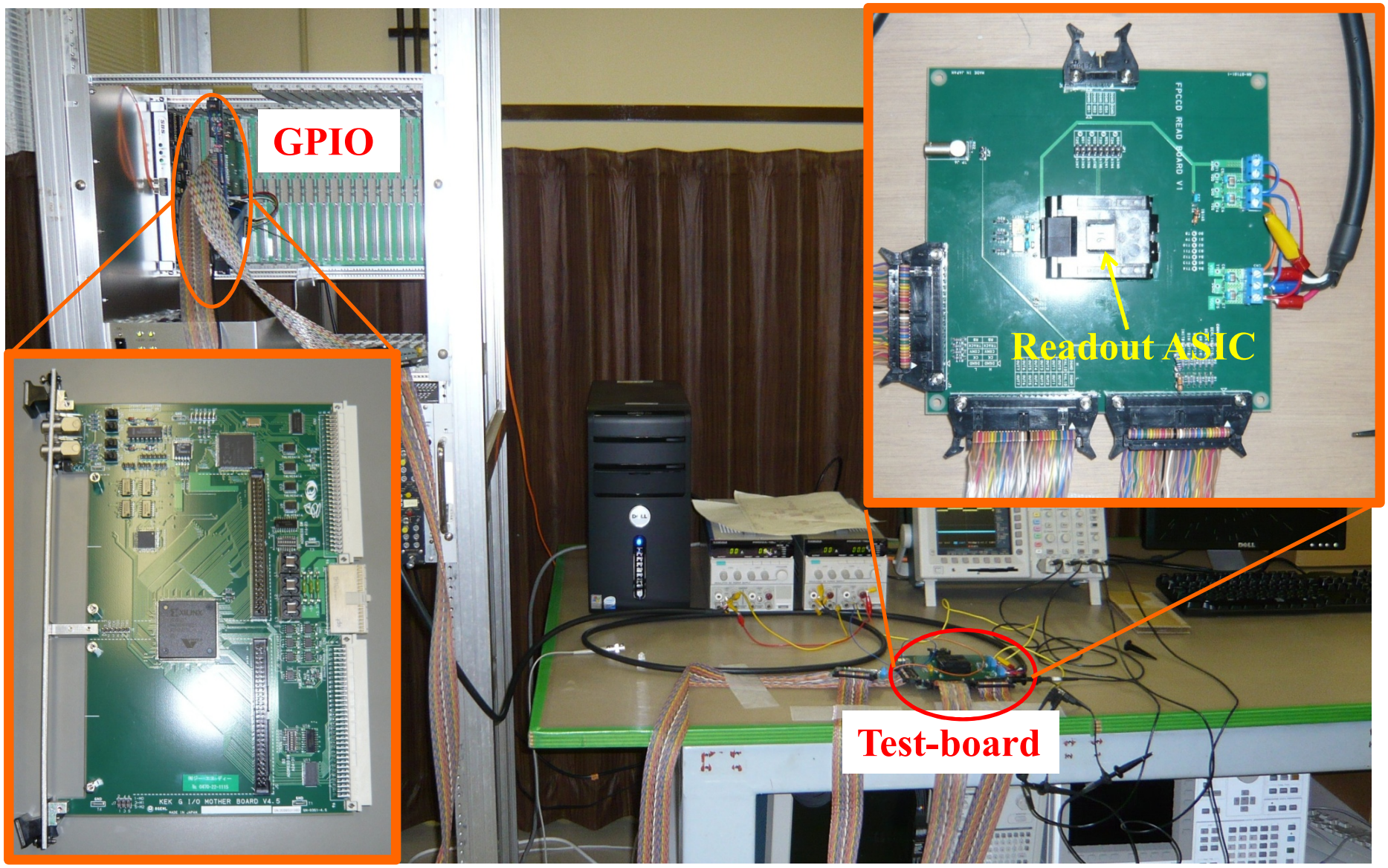
# Readout system

## Readout system

- Operation and data-acquisition is done by VME-GPIO module.
- ADC serial pulse is analyzed by a FPGA on the GPIO module.
- The ADC information is sent to PC.



# Picture of readout system



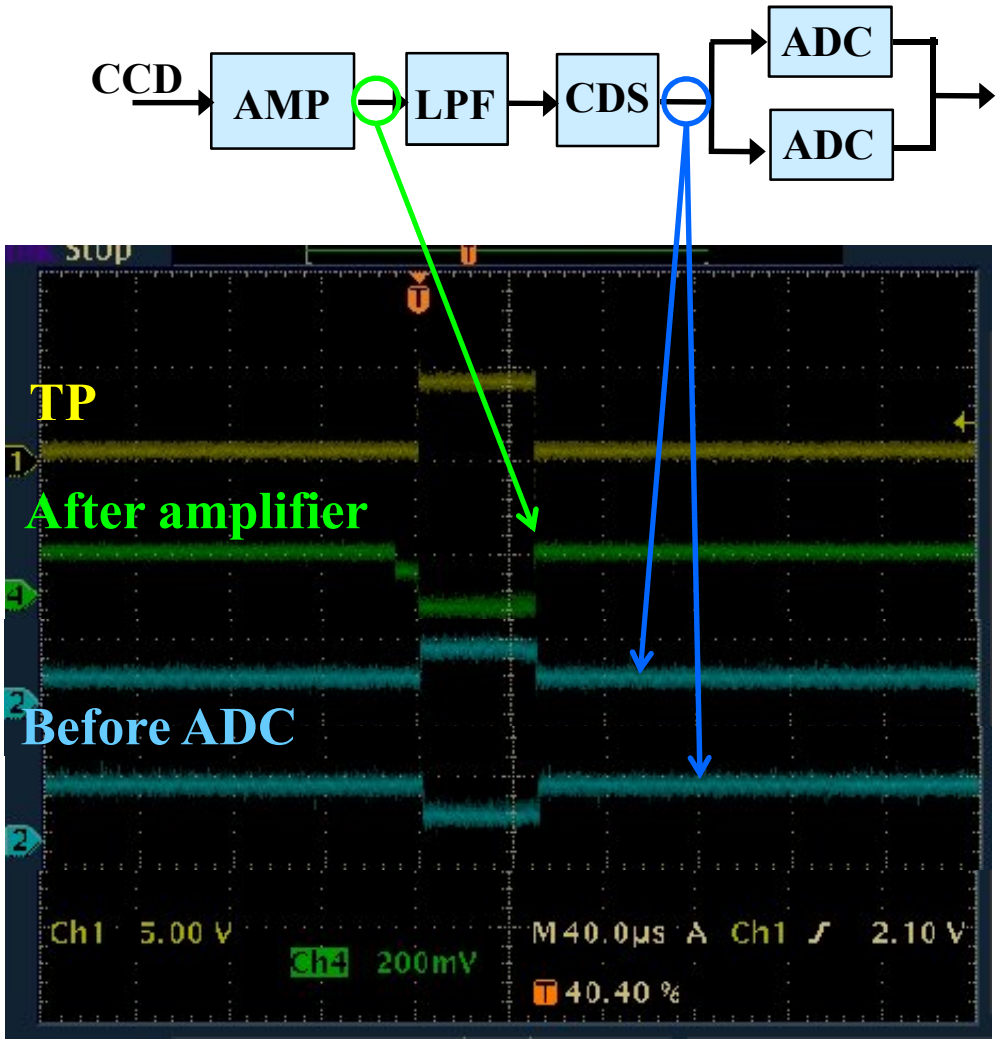
# Internal signals

Internal signals in the readout ASIC were check by the monitor output.

- The monitor is prepared after amplifier and before ADC.
- All monitor output was observed.

→ **The amplifier, LPF, and CDS are working.**

ADC output was checked.

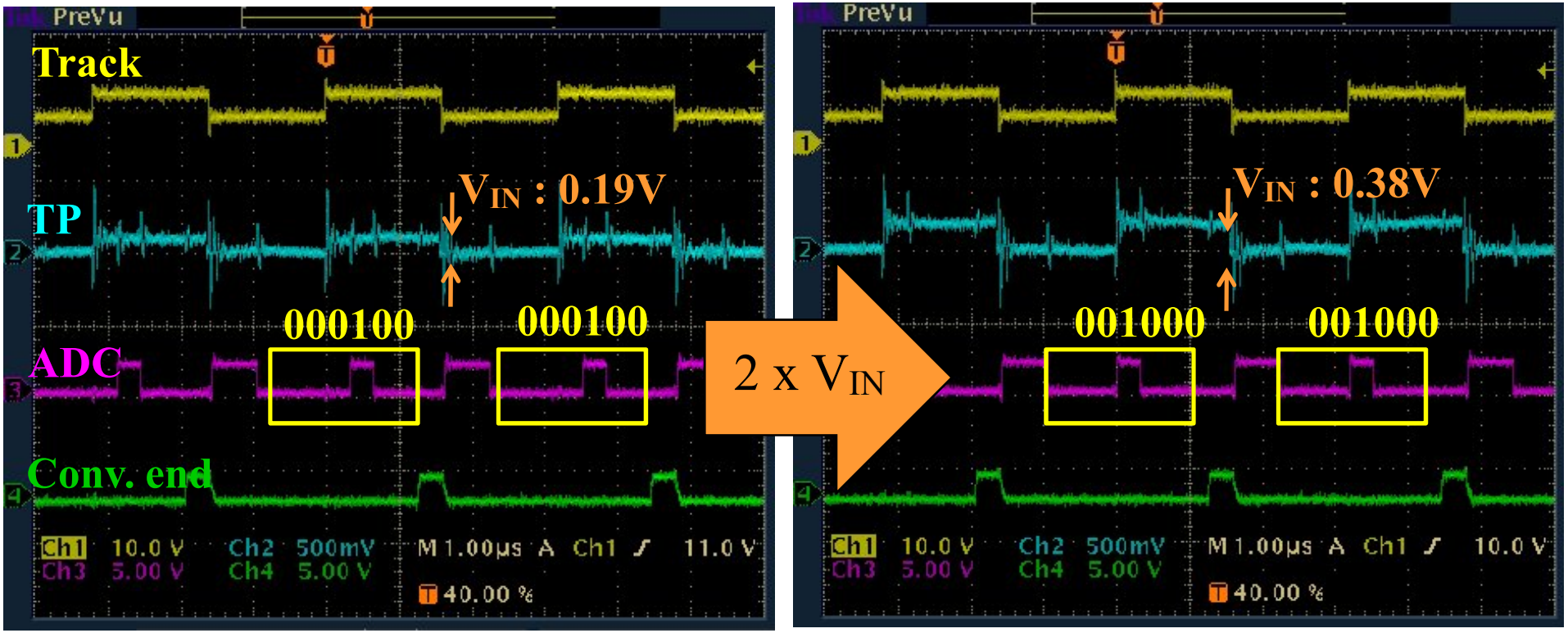


# ADC output

Output signals from the ADC were checked by an oscilloscope.

- ADC output : sign-bit + 6bit (: -64~+64 ADC-count)
- The ADC seems to work correctly.

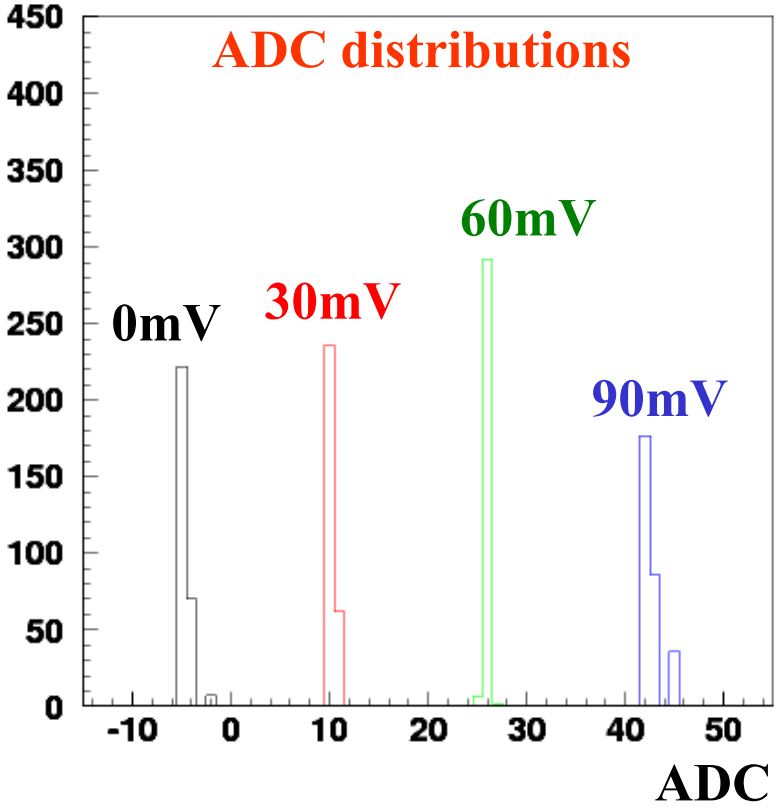
  → ADC output was read by the readout system.

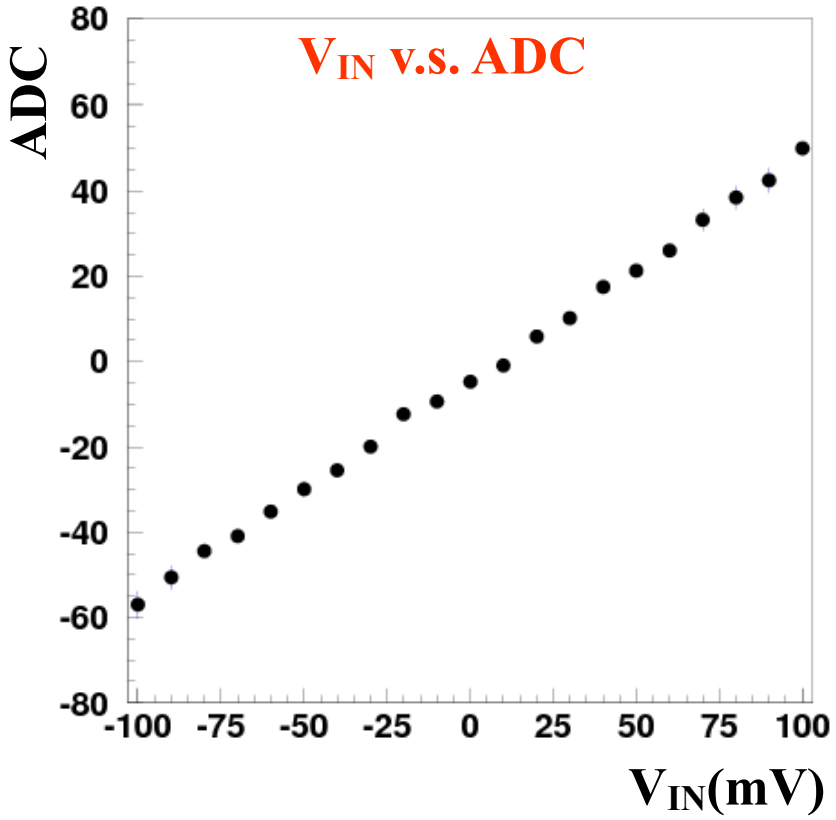


# ADC distributions

ADC value was investigated, inputting the test-pulse.

- The rate of A/D conversion : 10kHz
  - The conversion rate will be risen to 10MHz.
- The ADC value increases linearly with $V_{IN}$.

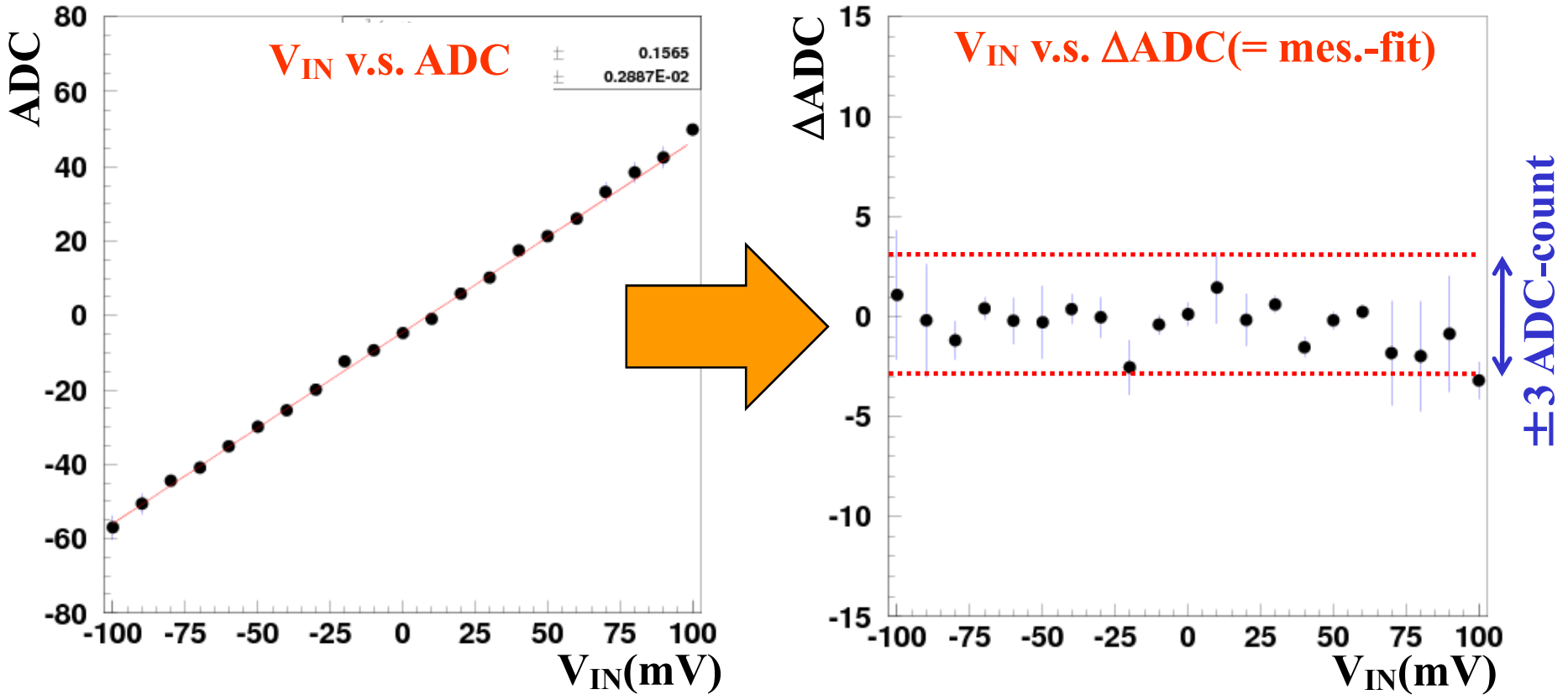


# ADC linearity

The ADC linearity was checked, fitting with a linear function.

- The linearity was within ±3 ADC-count.
- The improvement of the linearity will be tried.

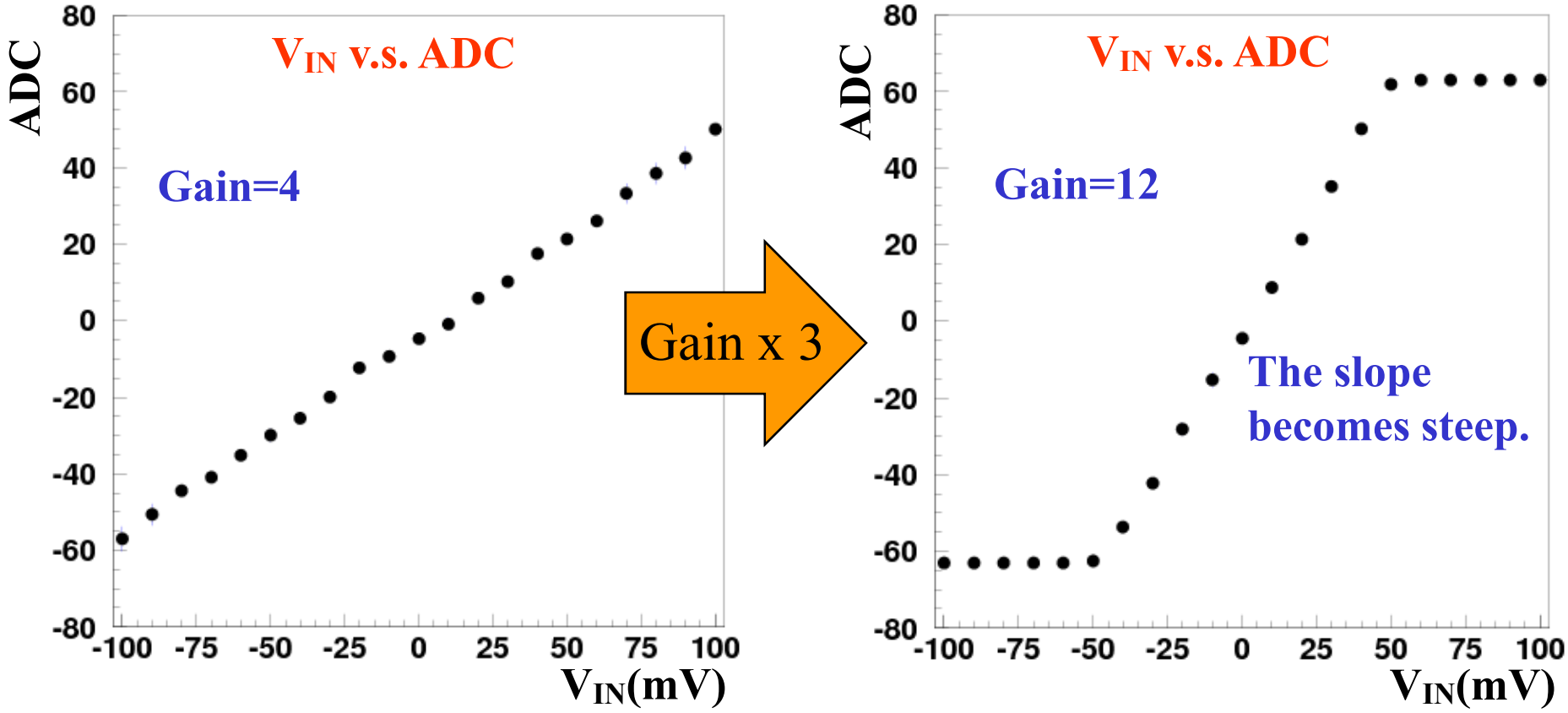


# Effect of amplifier-gain

The response of the ADC output to the amplifier-gain was checked.

- The gain can be adjusted for 1~64.
- The slope becomes steep for larger gain.

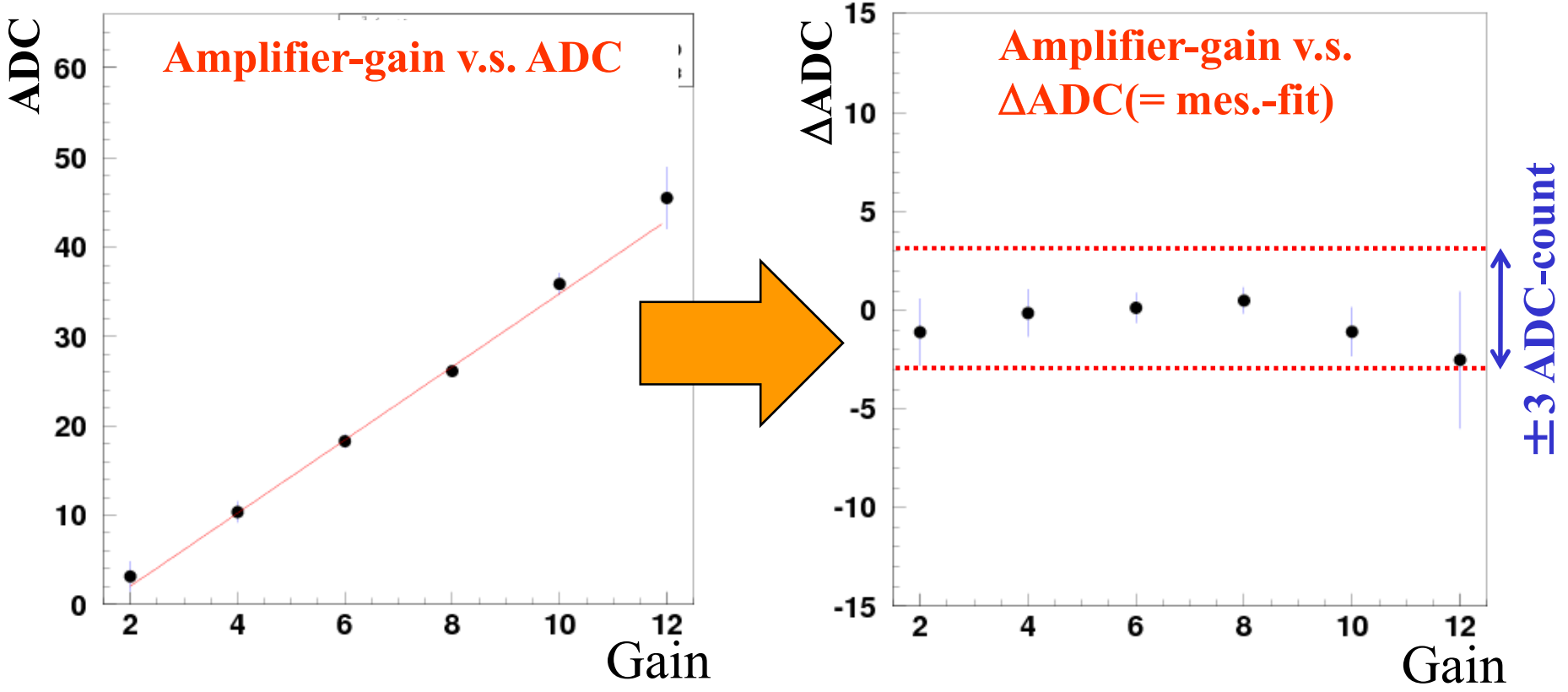
→ The ADC linearity against the amplifier-gain was investigated.



# Amplifier-gain v.s. ADC

The ADC output was studied as a function of the amplifier-gain.

- The linear dependence on the amplifier-gain was obtained.
  - The amplifier-gain can be adjusted correctly.
- The linearity is within ±3 ADC-count.



# Summary

- The readout ASIC for FPCCD was developed.
- Response test of the readout ASIC was started.
- ADC output was investigated.
- The ADC value was increased with the input voltage.
  - The linearity was within ±3 ADC-count.
- The ADC response for the amplifier-gain was checked.
  - The ADC output was gained linearly with 3 ADC-count precision.
- The next step is to improve the ADC linearity.

# Parameter setting

FPCCD < 2000e

- 5uA/e
- Output voltage <10mV

The current parameter setting

| | Gain : 2 | Gain : 4 | Gain : 16 |
|---|---|---|---|
| 64 ADC : | 200mV | 100mV | 25mV |
| Maximum range : | ~40,000e | ~20,000e | ~5,000e |