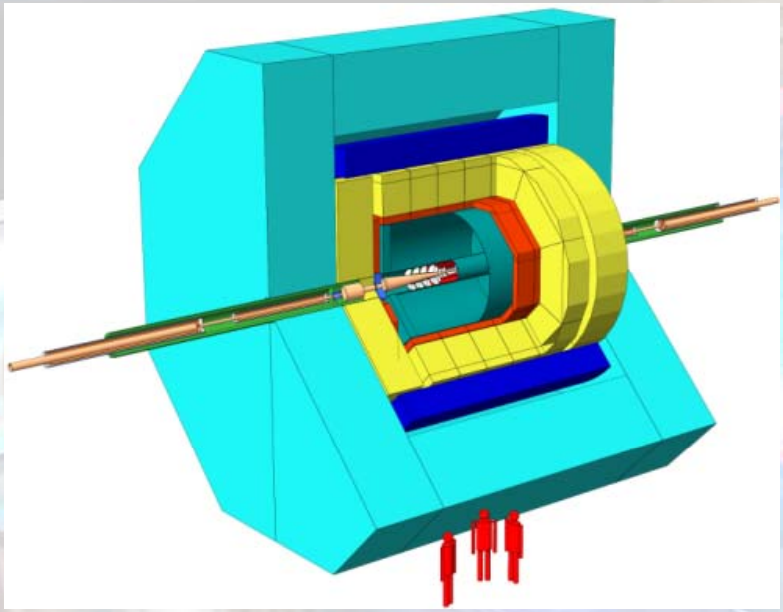
Data Acquisition for the ILD



G. Eckerlin

ILD Meeting
ILC ECFA Workshop,
Warsaw, June 11th 2008

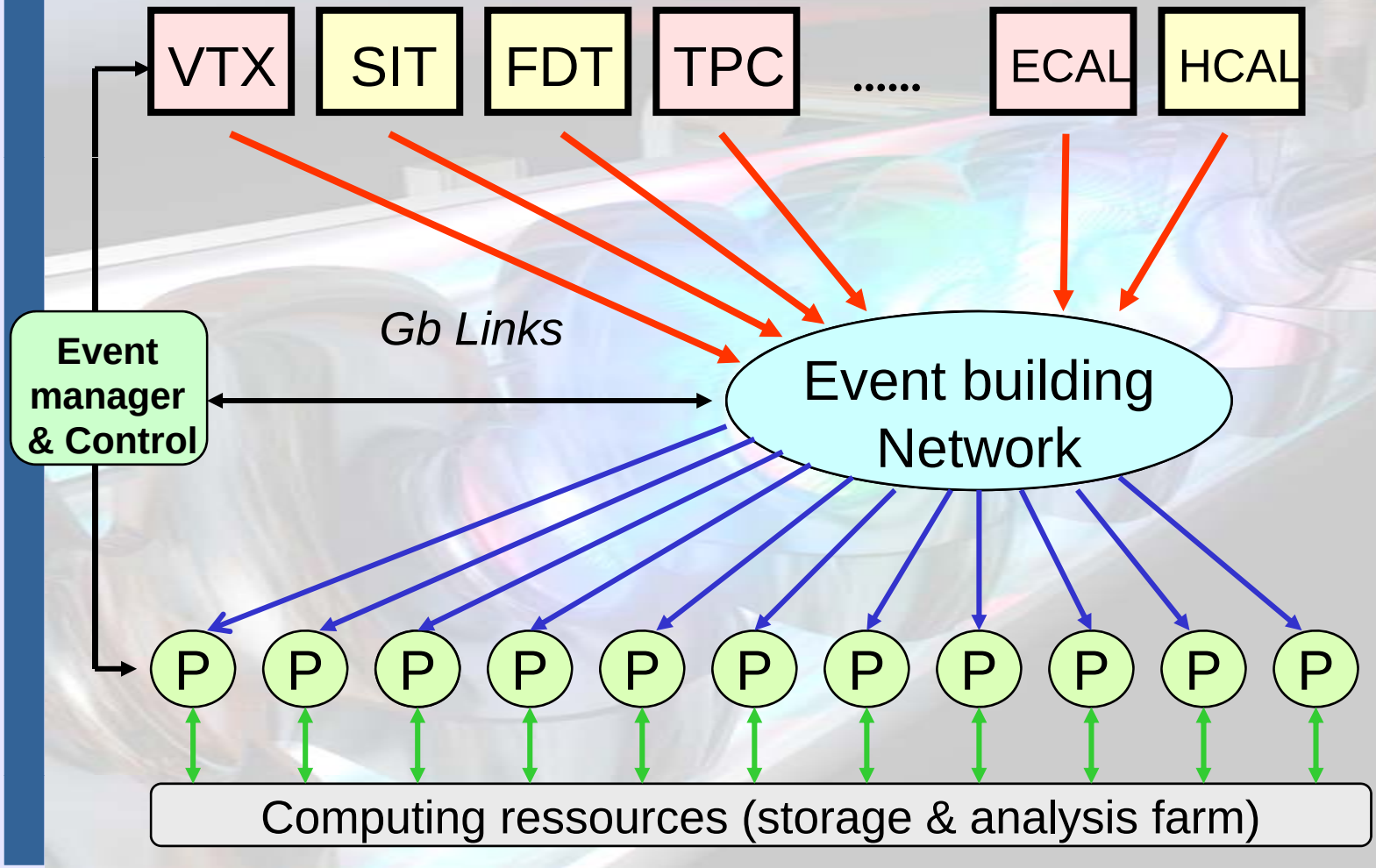
DAQ Concept

Current DAQ R&D

Towards the LOI

The DAQ Concept

General concept unchanged since Tesla TDR



~ 10^9 channels
no hardware trigger
1 ms pipeline

readout between trains
~ 200 ms
commercial hardware

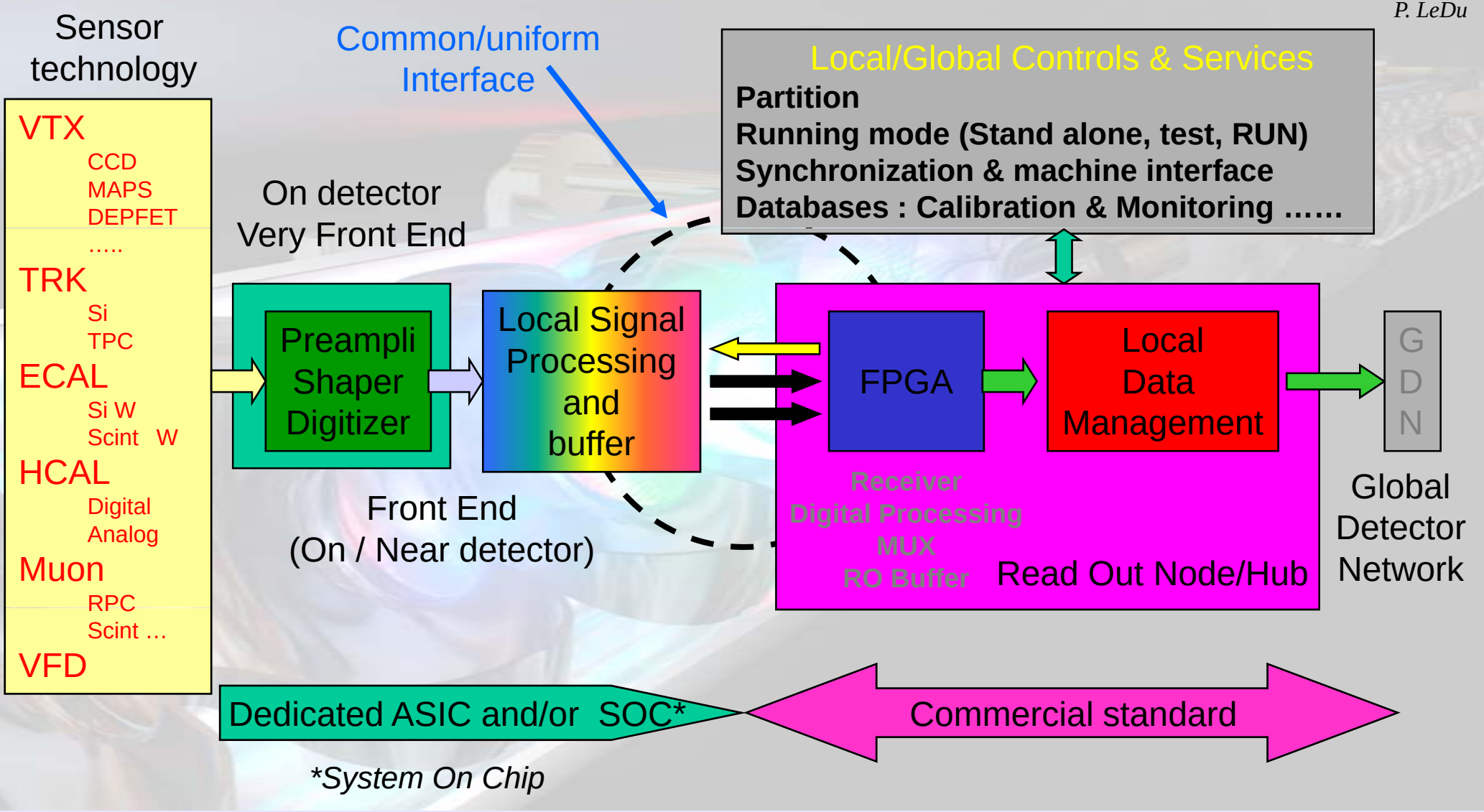
software event selection
- full train data to 1 node
- full detector information
- full train information

-> flexible & efficient

DAQ Architecture

ECFA Study
Physics and Detectors for a Linear Collider

P. LeDu



Status of DAQ R&D

- Thanks to R&D collabrations quite some progress on

  Front end readout electronics on or near the detector

  (presentations from SiLC, LCTPC, CALICE/EUDET in the DAQ session)

  But also an ‘ILC like’ test beam DAQ design now (EUDET)

- Take EUDET/CALICE as an example

  On detector ASIC with shaping, sampling, digitizing, hit detection

  Near detector electronics for data collection, clock distribution, etc

  Off detector electronics and DAQ software

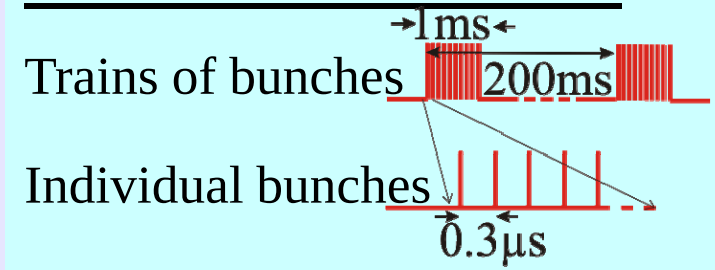
ILC Calorimeter DAQ (Valeria Bartsch)

- ILC Calorimetry will use particle flow algorithms to improve energy resolution
  - => 1cmx1cm segmentation results in 100M channels with little room for electronics or cooling
- Bunch structure *interesting:*
  - ~200ms gaps between bunch-trains
  - Trains 1ms long, 300ns bunch spacing
- Triggerless

=> ~250 GB of raw data per bunch train need to be handled

M. Anduze

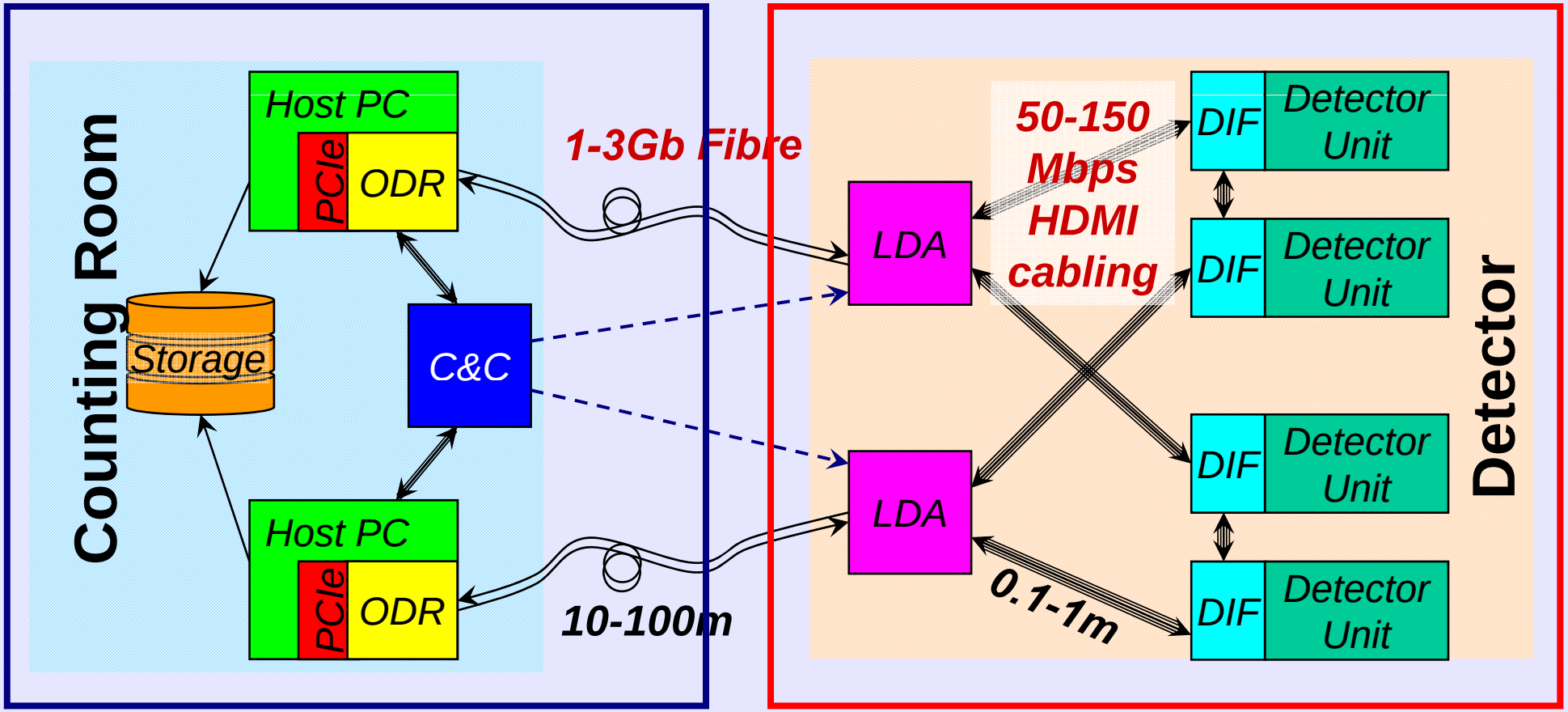
Time structure of bunches



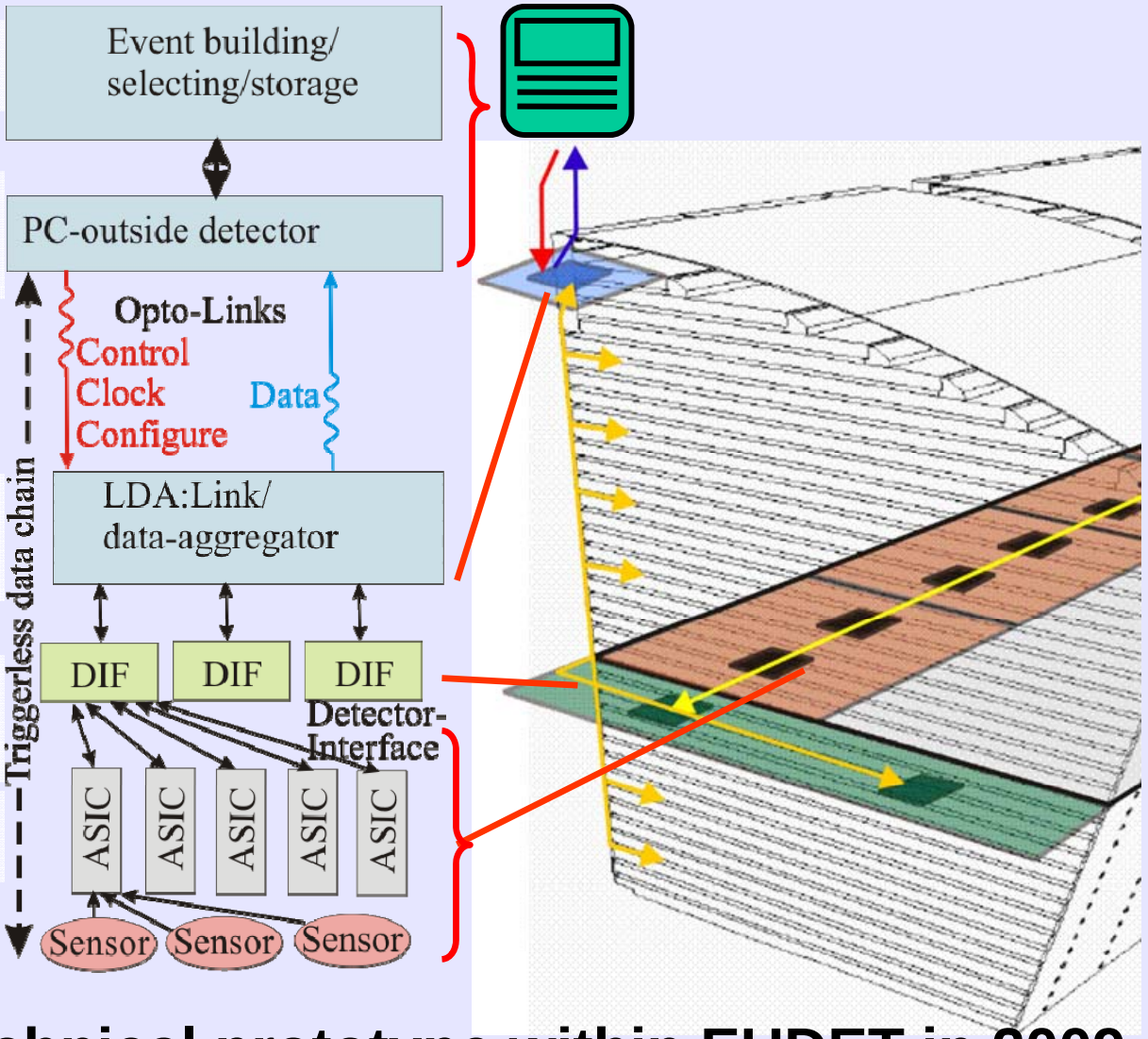
DAQ Architecture of CALICE/EUDET

Presented by Tao Wu

Presented by Valeria Bartsch



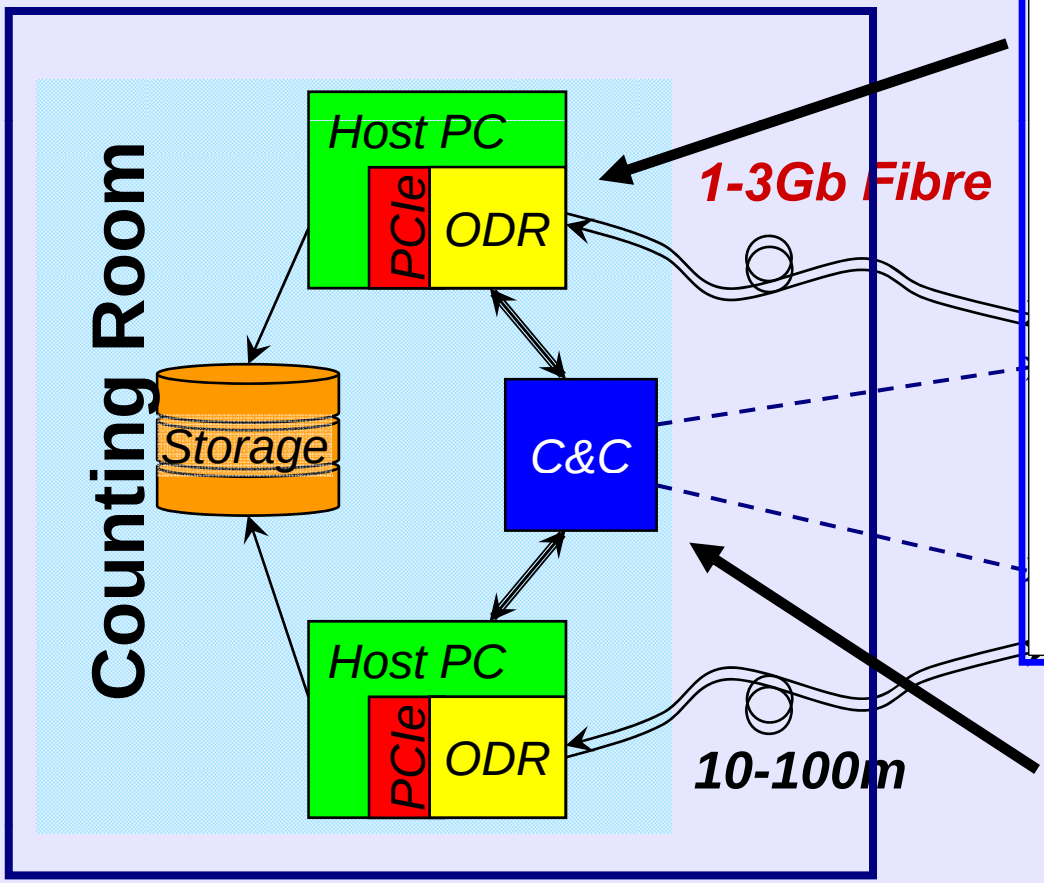
CALICE DAQ architecture (Valeria Bartsch)



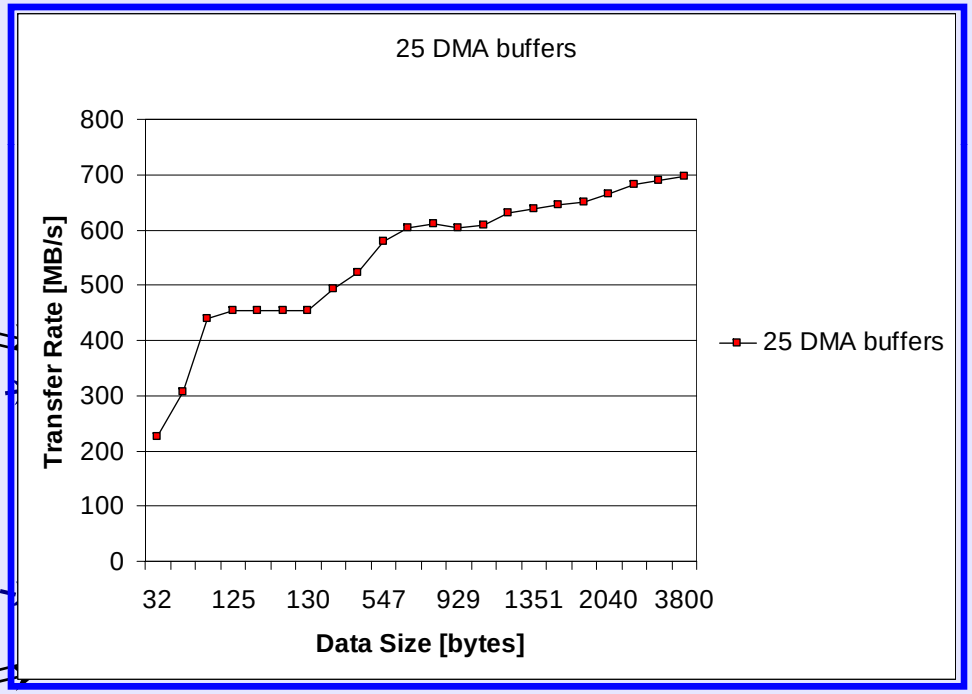
Preparing for the technical prototype within EUDET in 2009

Off detector DAQ of CALICE (Tao Wu)

covered in Tao's talk



Data transfer from ODR to user program (memory) at ~ 700 MByte/sec



Clock & Control board is designed will be built soon

EUDET DAQ will use DOOCS (Tao Wu)

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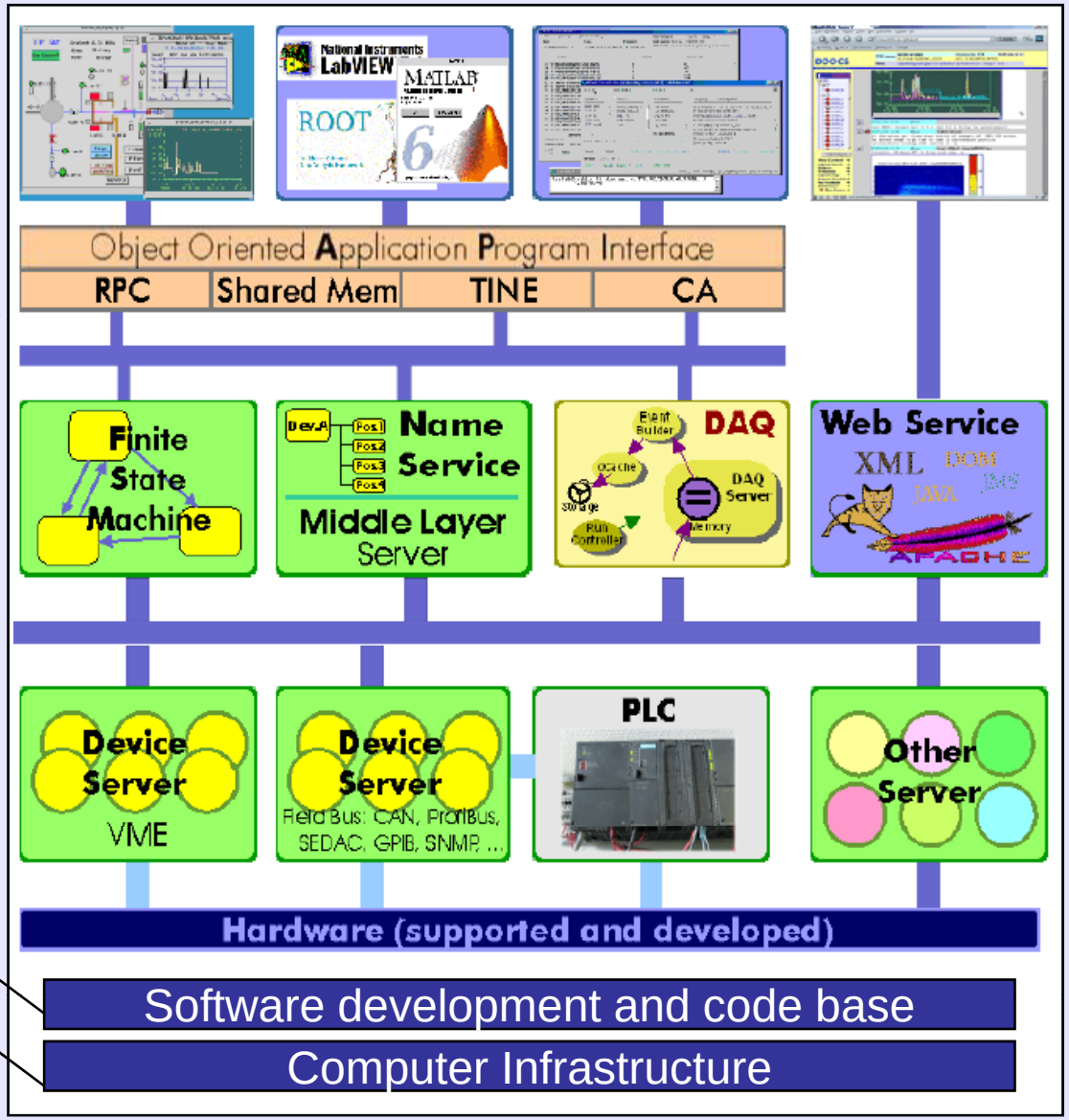
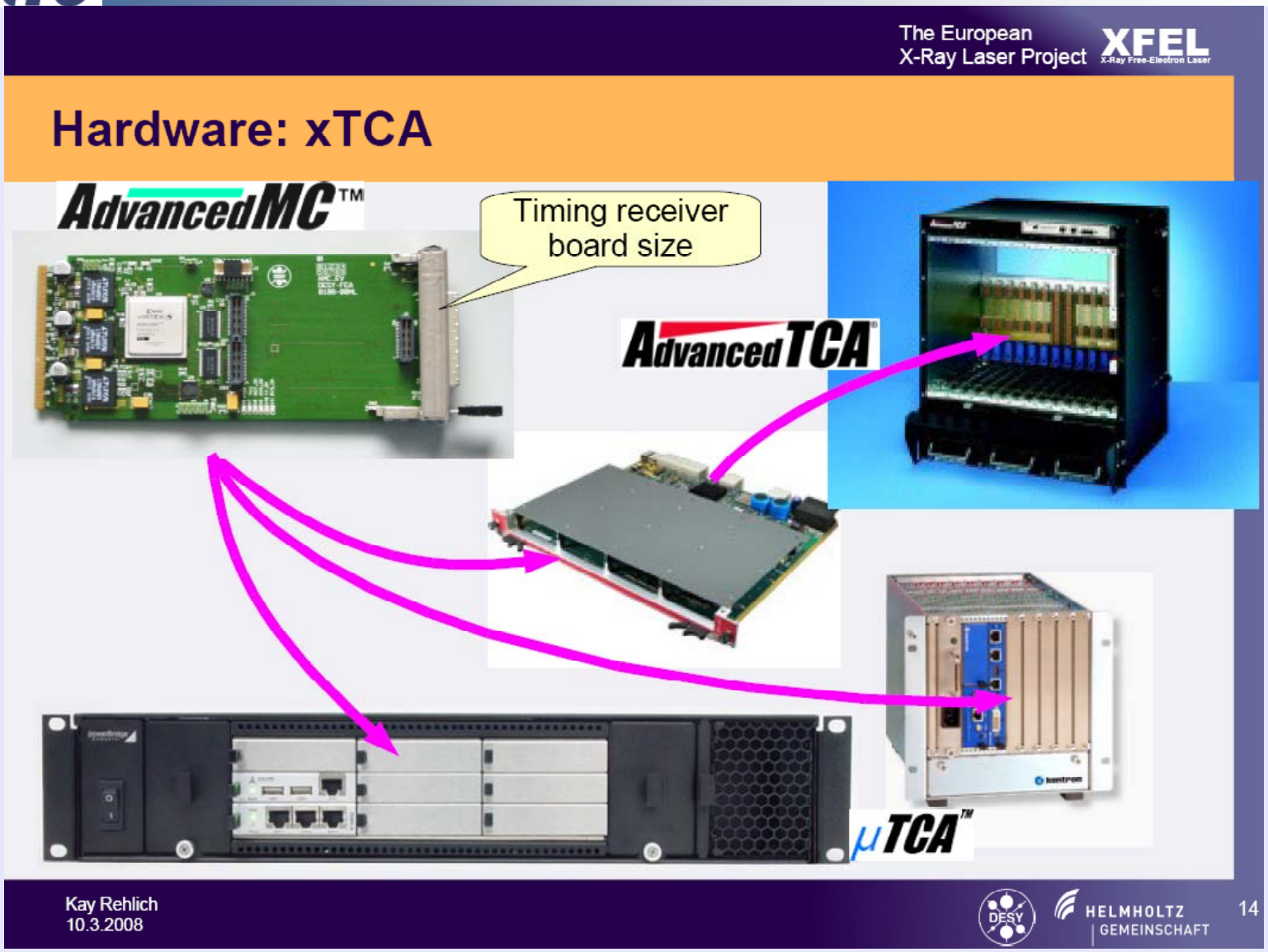
Physics and Detectors for a Linear Collider



The Distributed Object Oriented Control System will also be used for XFEL Control and DAQ.

May also learn from XFEL how to use xTCA



K. Rehlich at the workshop on XFEL DAQ and Control for photon beam systems

2d pixel detectors for photon science have similar data rates.

Large Pixel Detector :
(by J Coughlan/RAL)
512 FEM with
32MB @ 10 Hz
-> 150GB/sec

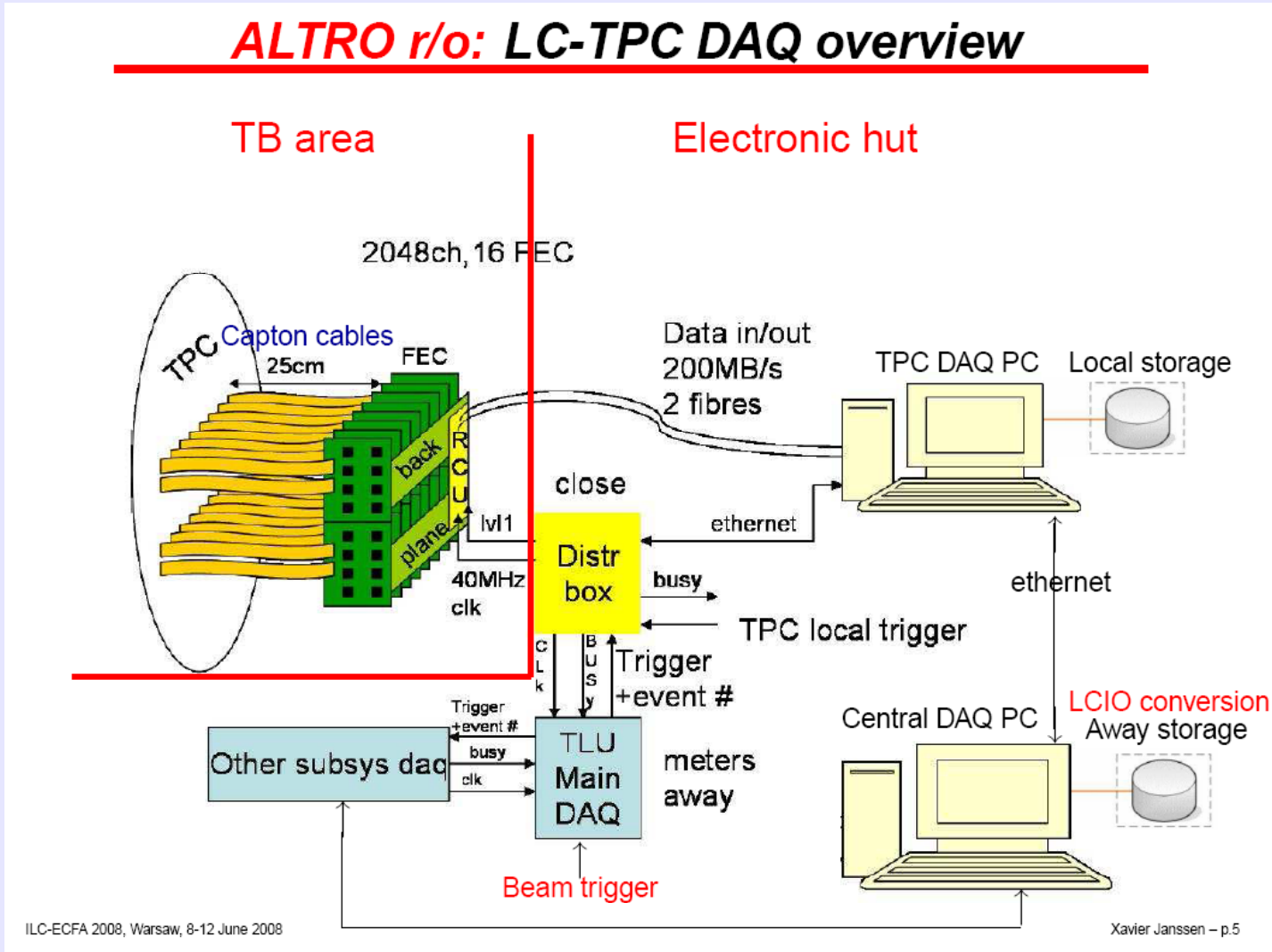
Towards LOI and beyond

- Too early for a full data model, but
  - need to learn how to profit best from new technologies (like ATCA/µTCA/AMC)
  - need event building for test systems with 'ILC like architecture'
  - need to define standards and common interfaces for different detectors
  - need to think about online data formats (offline software expects LCIO)
  - good example : EUDET (FP6) ! maybe DEVDET (FP7) ?
- Newly developed test beam readout getting closer to reality
  - make sure the readout interfaces do not diverge
  - encourage all R&D groups to use a common interface
  - address further common issues (calibration, commissioning, detector ctrl)

Thank you !

Some more examples of R&D Work

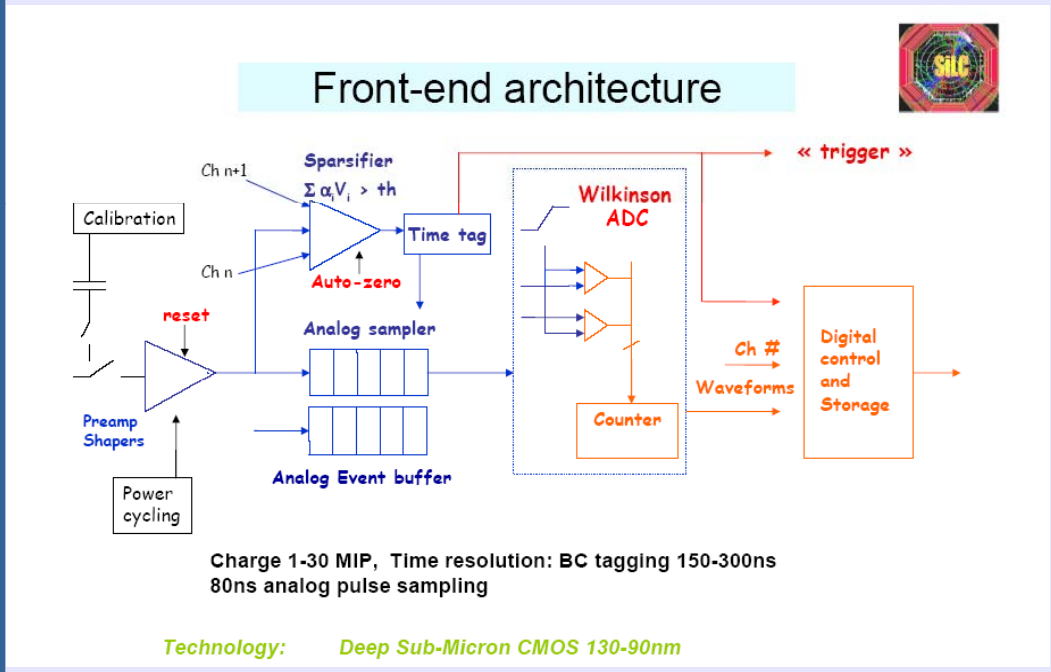
LC TPC Testbeam DAQ (X. Janssen)



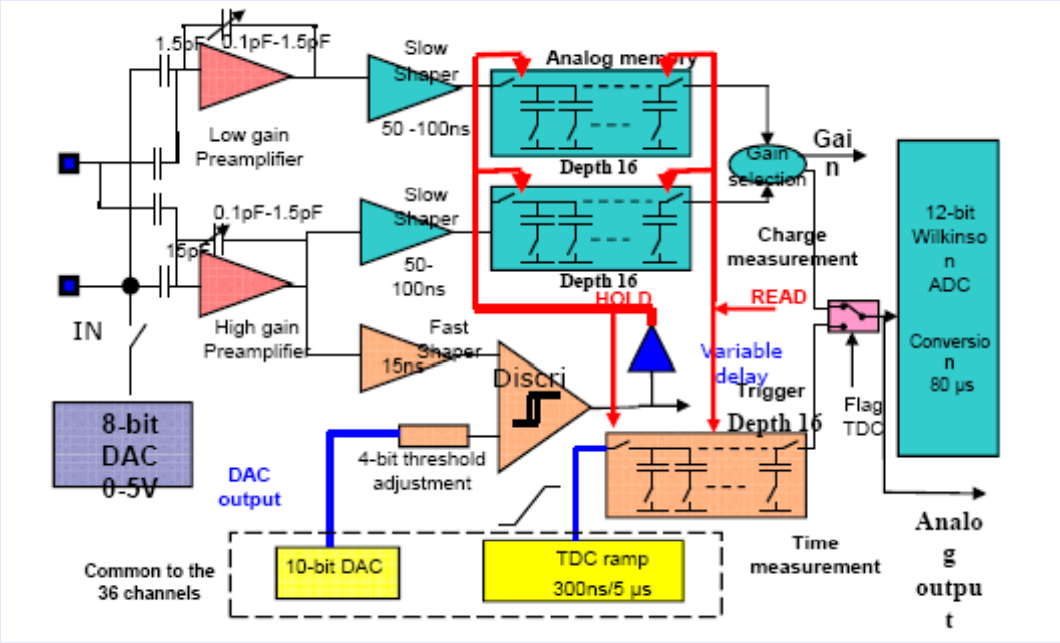
Front End R&D Examples

ECFA Study
Physics and Detectors for a Linear Collider

Architecture of CMOS readout chip of Silicon Strips (A. Savoy-Navarro for SiLC in the tracking session)



New ASIC readout chip for analog HCAL tests (F. Sefkow for CALICE in the Calorimeter session)



Many designs now fully integrate shaping, digitizing, hit detection, processing and digital buffering.
Getting closer to a real design for the ILC operation.
Output mostly digital via serial links (LVDS)