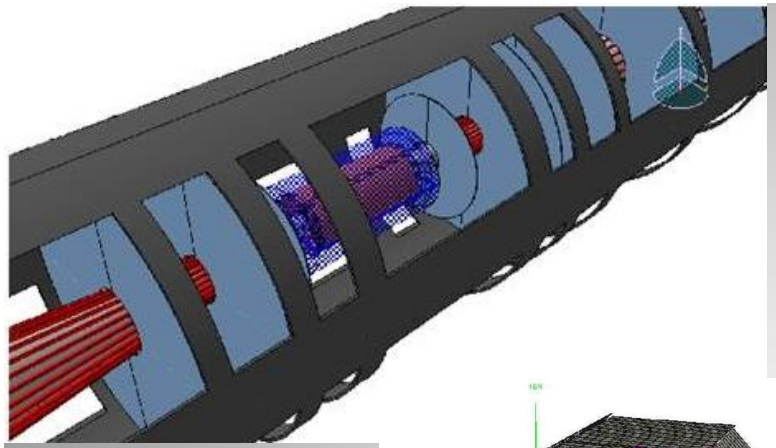
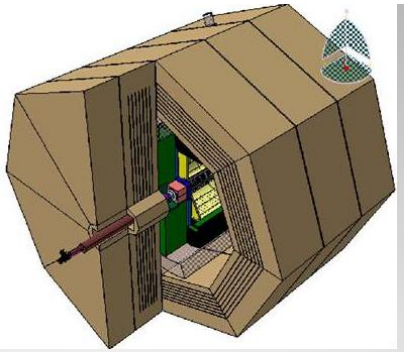
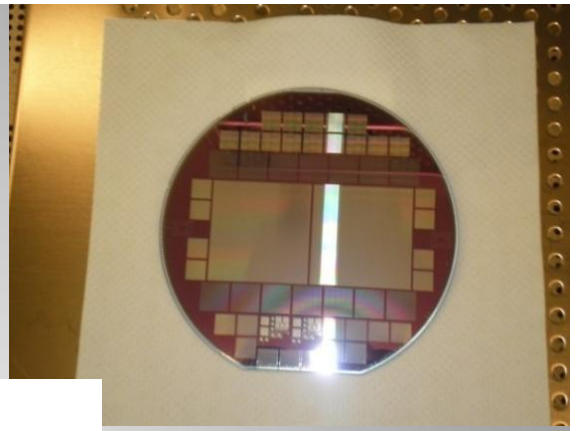
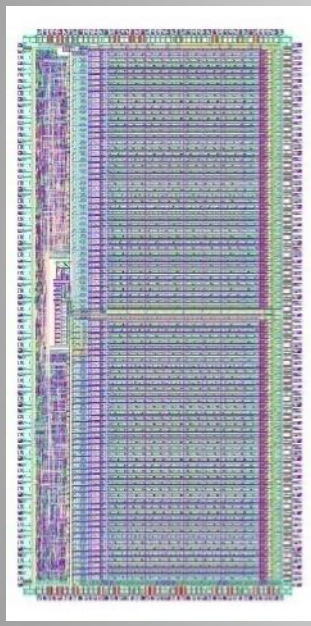
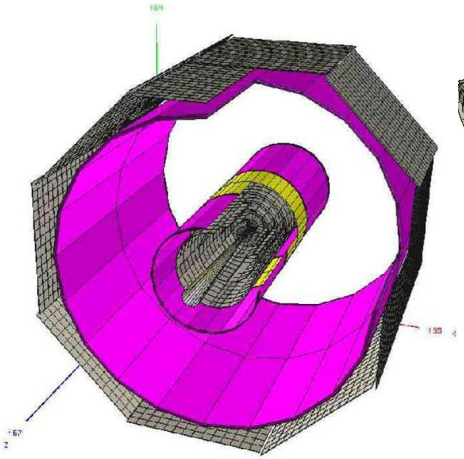
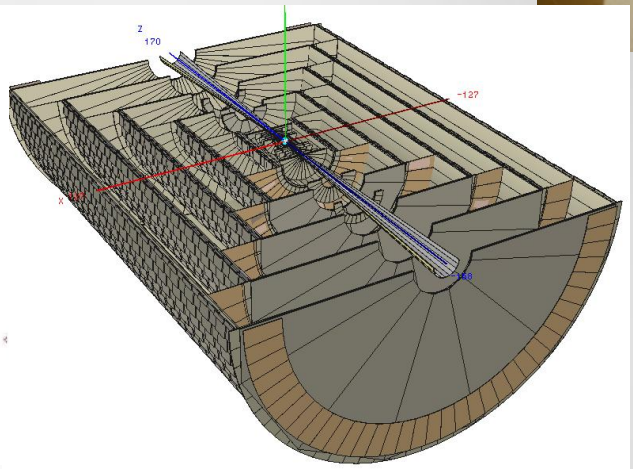
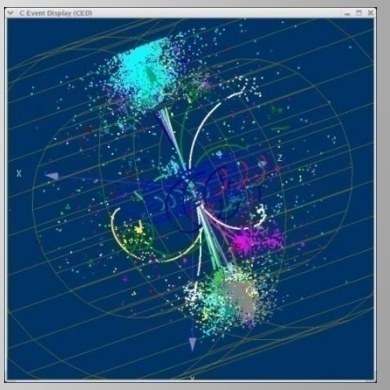








Silicon tracking for Linear Collider

A. Savoy-Navarro, LPNHE UPMC/IN2P3-CNRS

ECFA ILC Meeting at Warsaw, June 9-12, 2008

TOPICS

- SILICON TRACKING@ILD: GOALS and SET-UP
- BASELINE and R&D ROADMAP
- OPTIMIZATION and INTEGRATION TOOLS
- PROPOSED WORKPLAN

Silicon Tracking at ILD: Goals

Take major benefit from the Silicon tracking assets:

- High spatial resolution
- High momentum resolution
- Providing full coverage
- Easy merging of electronics on detector (by definition)
- Evolving fast with related high technology(ies)
- (*indeed a very active & successful high tech field*)
- Easy to operate and calibrate
- Can be used with (ILD or 4^{th} concept) or without (SiD) gaseous central tracker.

Work on the major issue: improving overall material budget
(this is an issue not only for this detector technology)

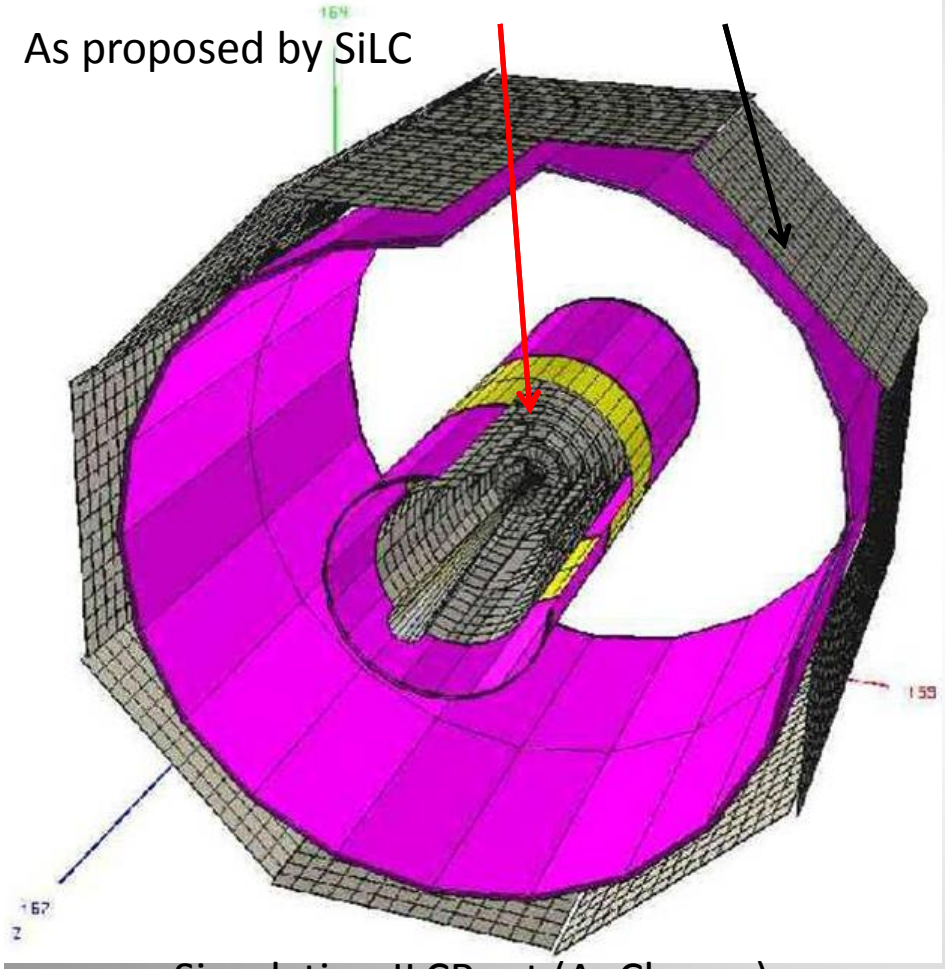
The ILD Silicon tracking development is done within the SiLC R&D Collaboration, to which all the Si tracking groups from GLD (esp. Korean teams) are part of.

ILD Silicon tracking: Set-up

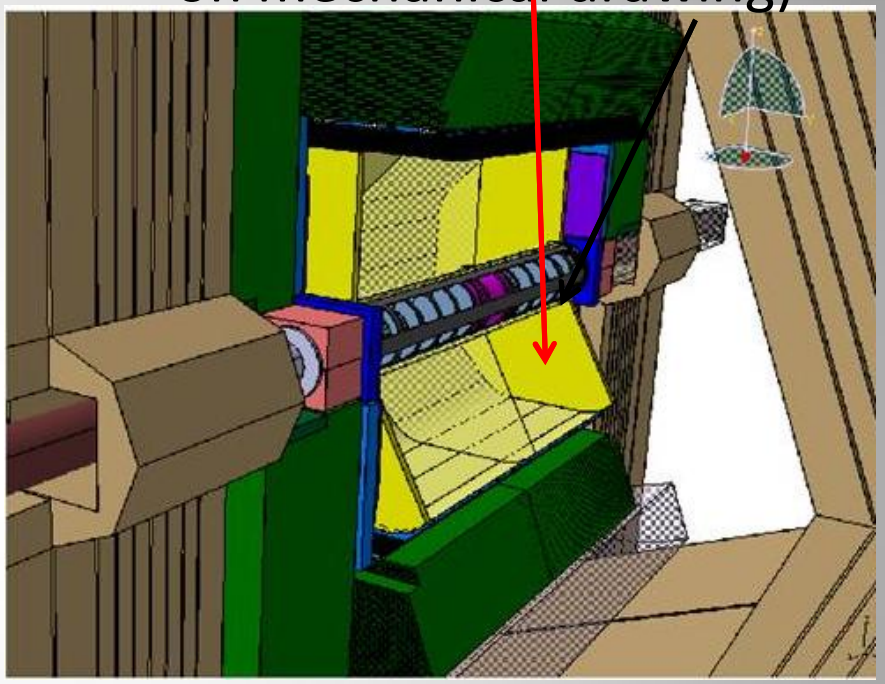
Barrel: SIT and SET

End Caps: FTD and ETD (to be added on mechanical drawing)

As proposed by SiLC

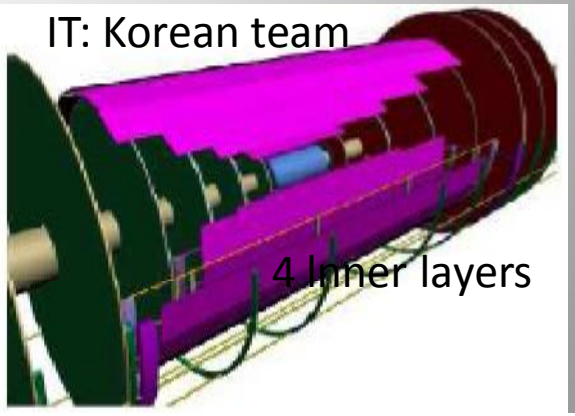


Simulation ILCRoot (A. Charpy)



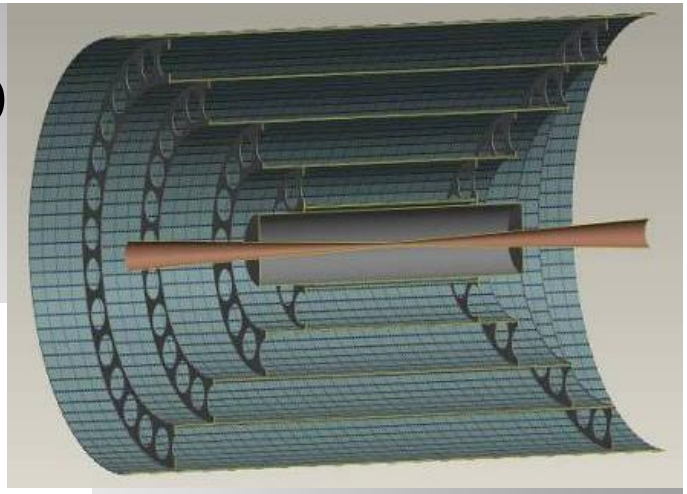
Mechanical CAD: Anduze+Jorre)

IT: Korean team

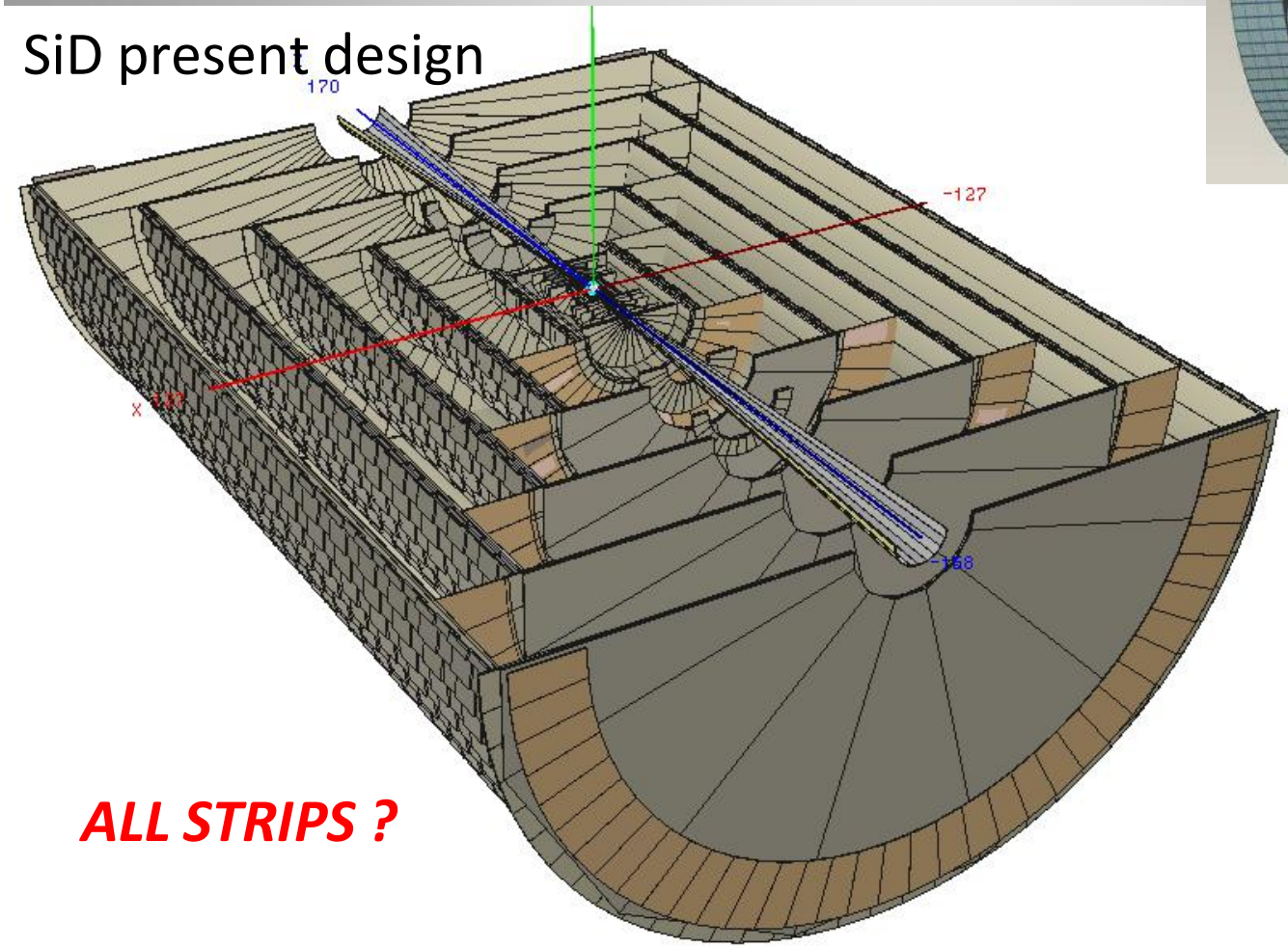


4 Inner layers

All Silicon tracking: how do we (ILD) compare with it?



SiD present design



ALL STRIPS ?

ALL PIXELS ?

(C. Damerell)

Baseline and Roadmap

Two timescales are foreseen:

- Be ready to build in 2012 (baseline & R&D)
- Be ready to build ≥ 2015 (R&D)

Baseline: based on microstrips and DSM FE bump bonded onto the detector (as proposed by SiLC in collaboration with Industry = HPK)

R&D: pursue on technological developments and use/keep an eye on more modern available solutions

R&D: Technological choices and issues

Sensors: edgeless, higher granularity, thinner

- Si-strip
- Pixel technologies
- New Sensors technologies (mainly driven by 3D on strips and pixels or ??)

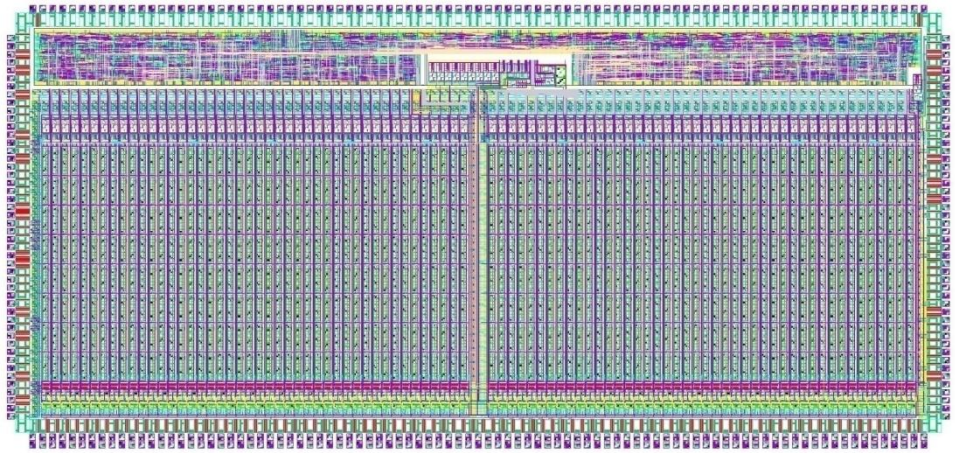
Electronics: low noise, low power consumption, power cycling, high processing level, high multiplexing, fault tolerant

- DSM FEE
- direct connection to the Silicon sensor (strip or pixel), 3D vertical interconnect
- integration to the overall readout and DAQ

Integration Technologies:

mechanical support and construction of elementary module (tile), cooling, connection of electronics to detector, cabling, alignment, mechanical integration of these components within the overall detector

Hand in hand with LHC upgrades or other facilities R&D and in collaboration with Industrial firms



Basic elements of the Silicon tracker:
Sensors
FEE readout system
Direct connection between them
- Bump bonding (HPK)
- 3D interconnect (starting within global effort)

OPTIMIZATION, INTEGRATION
and
SIMULATION TASK FORCE
First objectives: the ILD LOI's

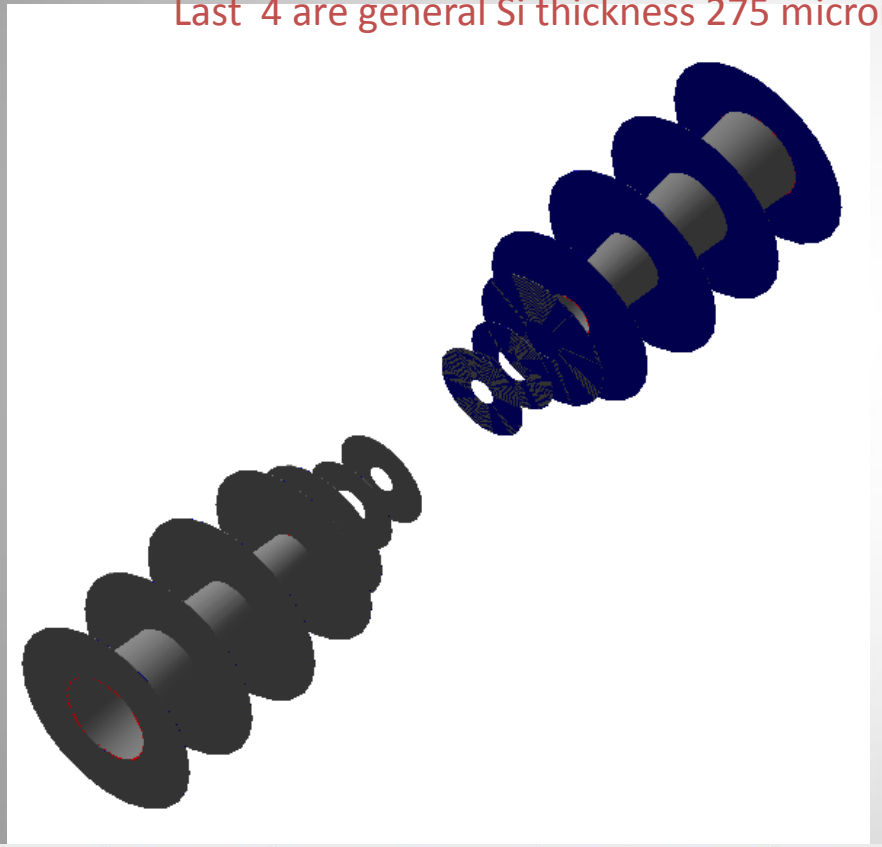
All Silicon tracking have been included in the MOKKA framework

Optimization: FTD Geometry

FTD: 7 Disks

First 3 pixel technology Si thickness 50 microns + Carbon Fiber support thickness 1 mm ,

Last 4 are general Si thickness 275 microns + Carbon Fiber Support 1 mm



Database ftd04 - table disk

Showing records 0 - 7 (7 total)

Show : 30 rows starting from 0 Full Texts

disk_number	z_position	inner_radious	outer_radious
1	220	29	140
2	350	32	140
3	500	35	210
4	850	51	270
5	1200	72	290
6	1550	93	290
7	1900	113	290

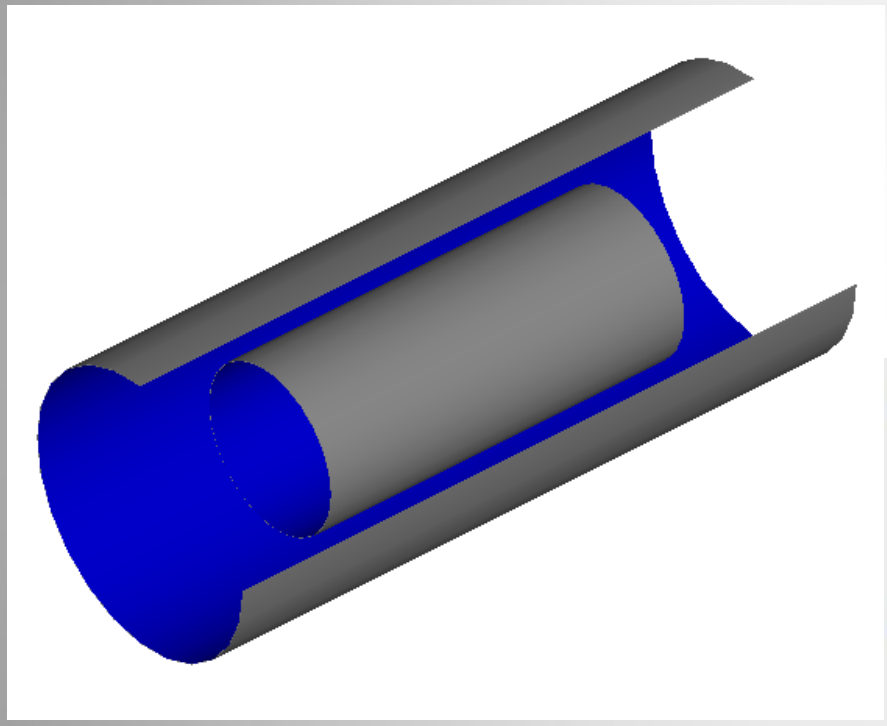
Show : 30 rows starting from 0 Full Texts

Insert new row

id	Si_thickness	Si_thickness_2	inner_support_thickness	inner_support_length	outer_support_thickness	outer_support_length	outer_cylinder_total_thichness	cables_thichness
0	0.05	0.275	1	4	2	4	1	0.08

Optimization: SIT Geometry

SIT: 2 barrel detectors Si thickness 275 mk + Carbon Fiber Support - thickness 1mm



Database sit02 - table sit

Showing records 0 - 2 (2 total)

Show : 30 rows starting from 0 Full Texts

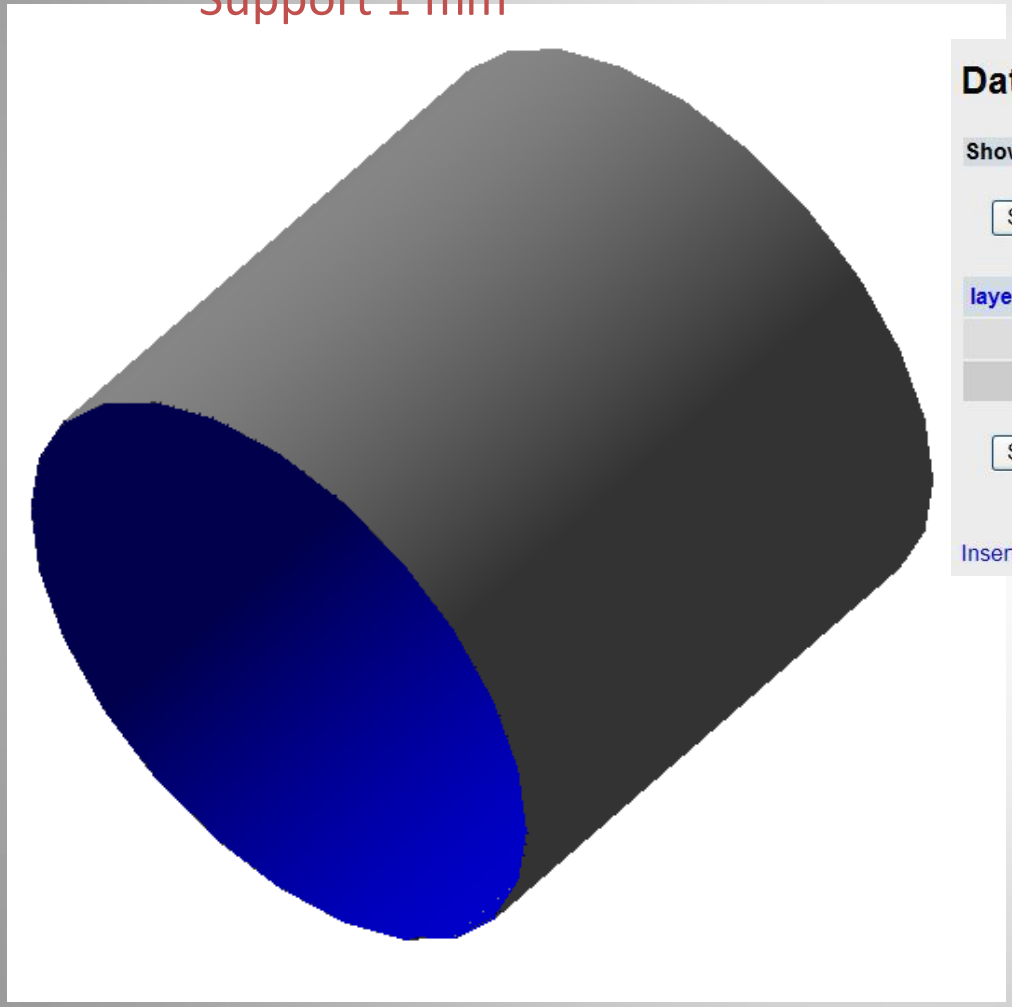
layer_id	inner_radious	half_z	sensitive_thickness	support_thickness
1	160	380	0.275	1
2	270	660	0.275	1

Show : 30 rows starting from 0 Full Texts

Insert new row

Optimization: SET Geometry

SET: 2 barrel detectors Si thickness 275 microns + Carbon Fiber Support 1 mm



Database SET01 - table EST

Showing records 0 - 2 (2 total)

Show : 30 rows starting from 0 Full Texts

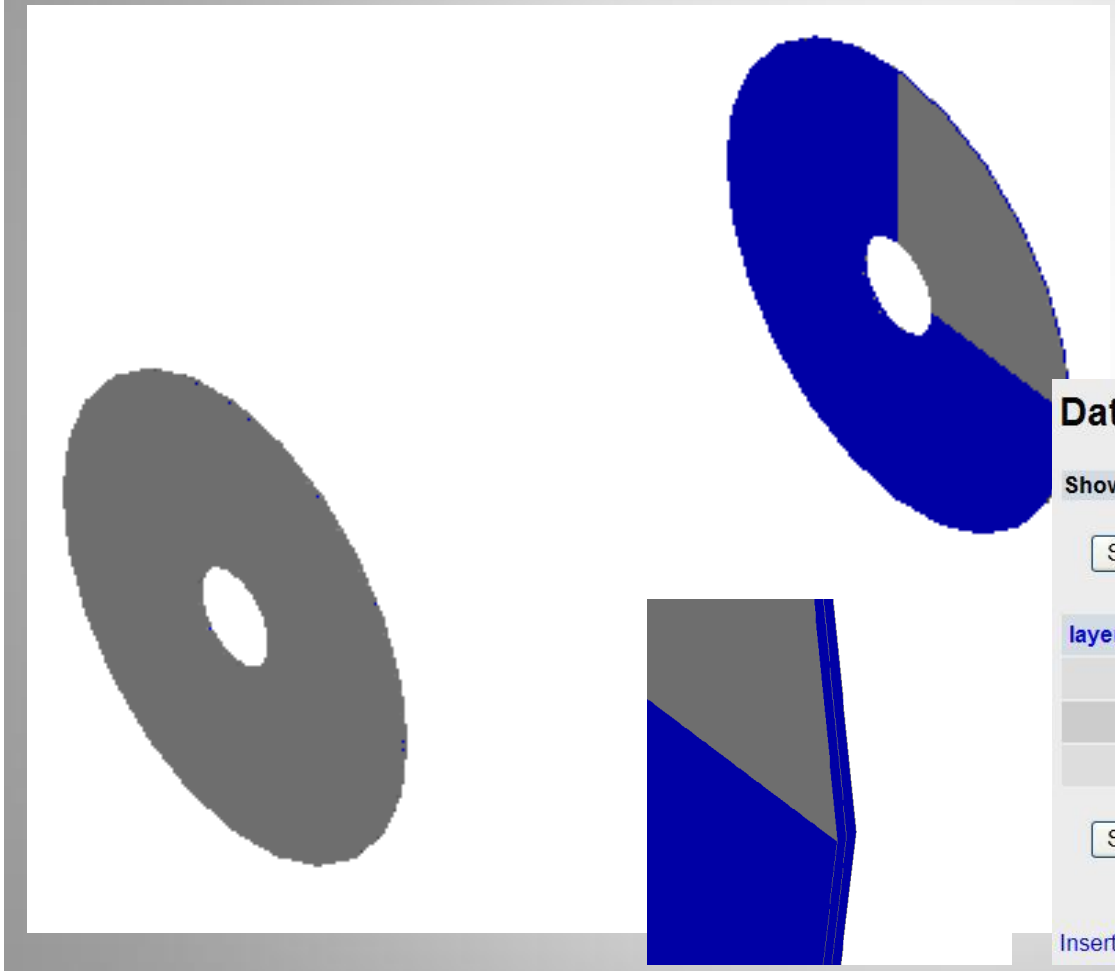
layer_id	inner_radious	half_z	sensitive_thickness	support_thickness
1	1592.5	1500	0.275	1
2	1587.5	1500	0.275	1

Show : 30 rows starting from 0 Full Texts

Insert new row

Optimization: ETD Geometry

ETD: 3 disks, XUV plane, Si thickness 275 microns + Carbon Fibers Support 1 mm,



Database etd01 - table ETD

Showing records 0 - 3 (3 total)

Show : 30 rows starting from 0 Full Texts

layer_id	inner_radious	half_z	sensitive_thickness	support_thickness
1	305	2368	0.275	1
2	305	2368	0.275	1
3	305	2368	0.275	1

Show : 30 rows starting from 0 Full Texts

Insert new row

Simulation & reconstruction with IlcROOT framework

- Introduction of ILD concept in IlcRoot (in collaboration with C. Gatto's team - 4th concept – INFN Lecce)
- IlcRoot: based on ALICE framework

  GEANT3/4, FLUKA support

  Simulation -> Hits -> Digitization -> Reconstruction (F. Ignatov et al)
- Idea: introduce the MOKKA data base parameters (Collaboration with V. Saveliev)

Database sit02 - table sit

Showing records 0 - 2 (2 total)

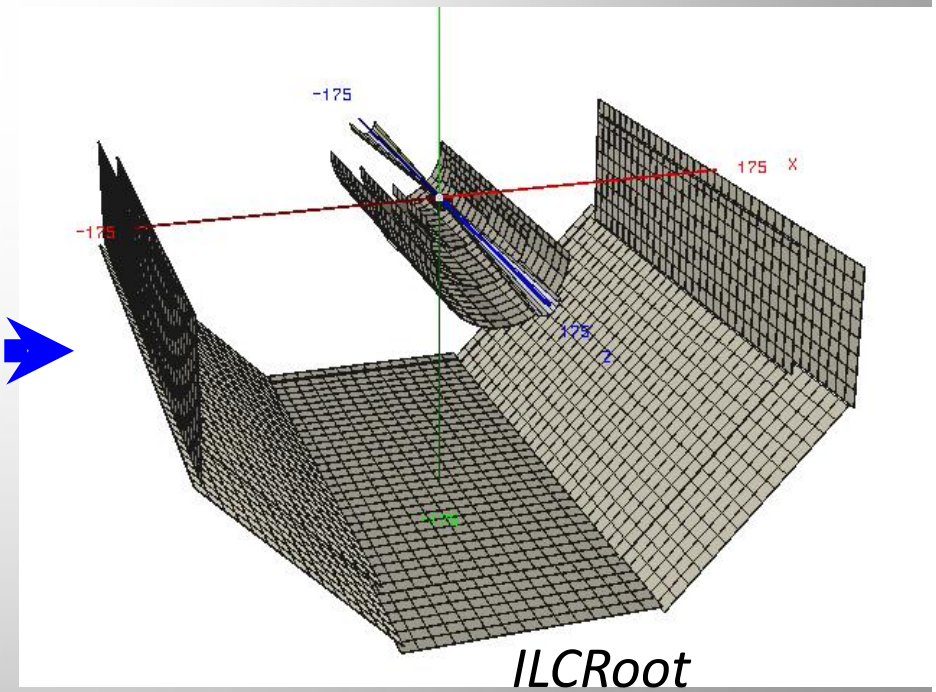
Show : 30 rows starting from 0 Full Texts

layer_id	inner_radious	half_z	sensitive_thickness	support_thickness
1	160	380	0.275	1
2	270	660	0.275	1

Show : 30 rows starting from 0 Full Texts

Insert new row

MOKKA DB

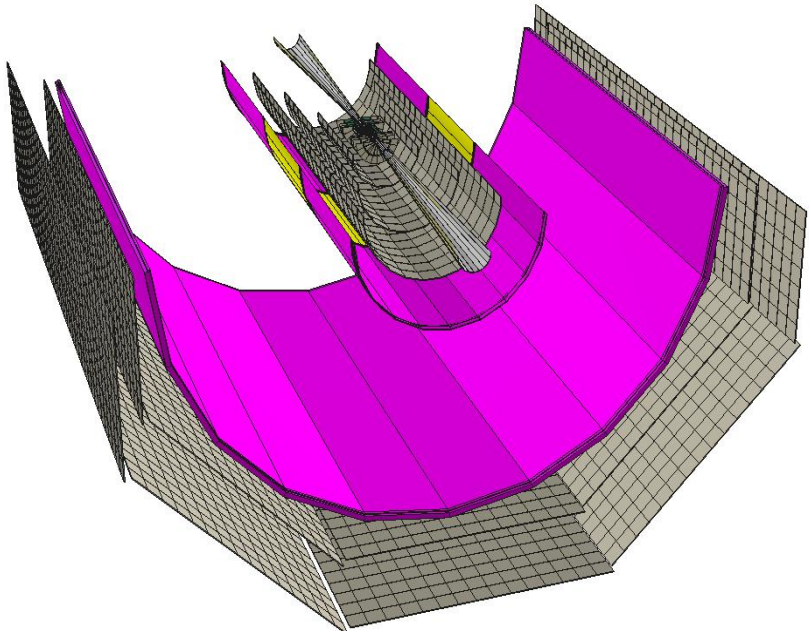


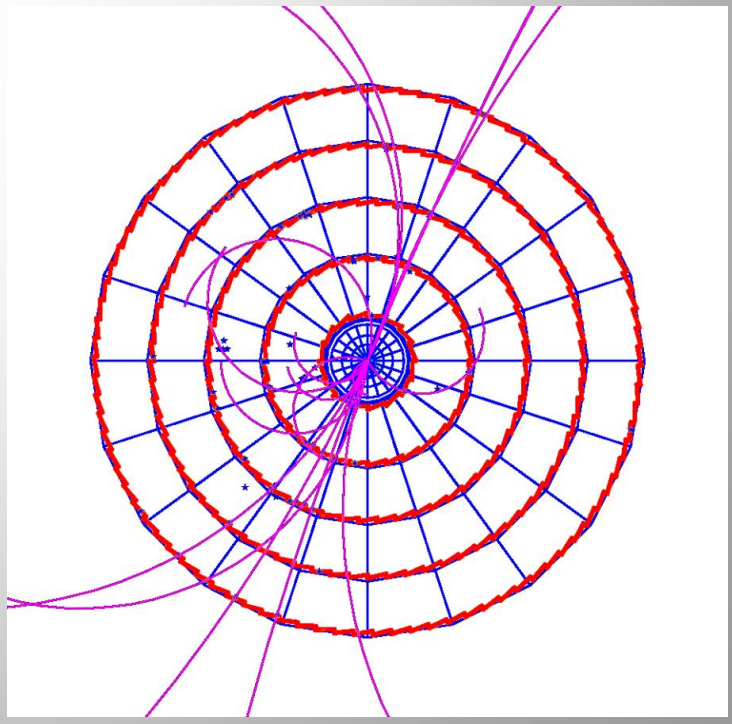
ILCRoot

Simulation and reconstruction with IlcROOT framework

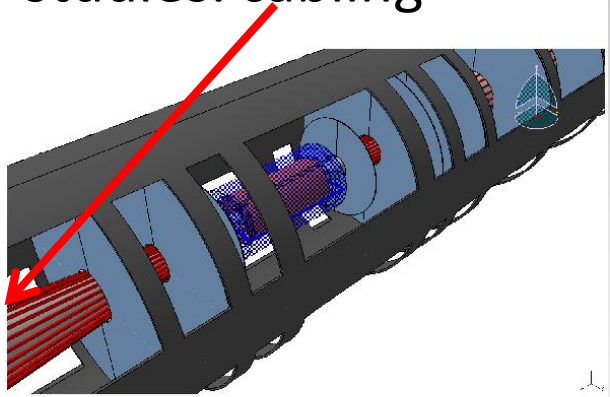
Comparison between different configurations:

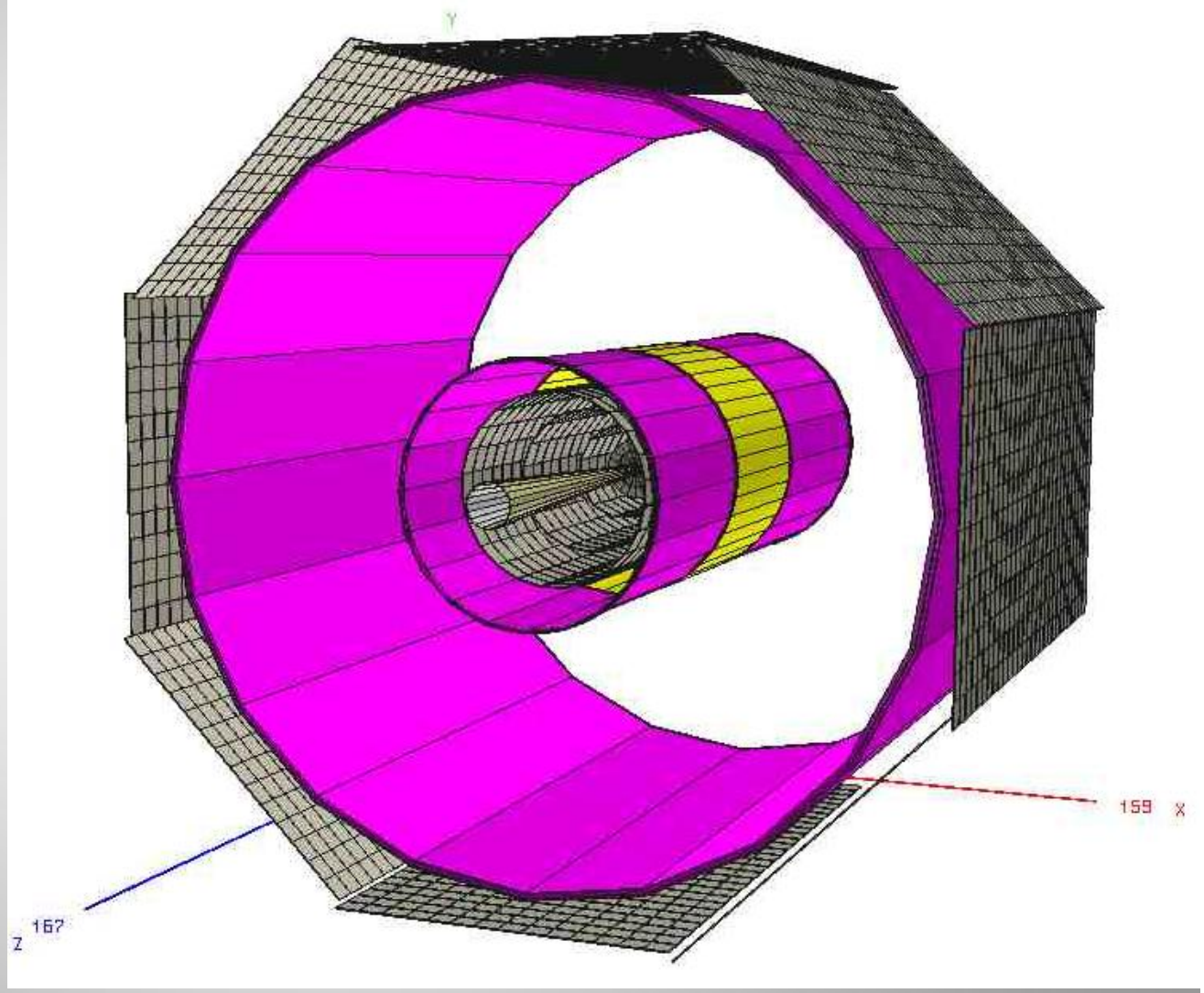
- Barrel silicon detector / Silicon trackers (SIT+SET) +TPC
- Overlapping/adjacent sensors in central barrel
- Projective/XUV at end caps
- Sensors technologies (pixels, SSD strips, DSSD strips)





Mechanical integration studies: cabling

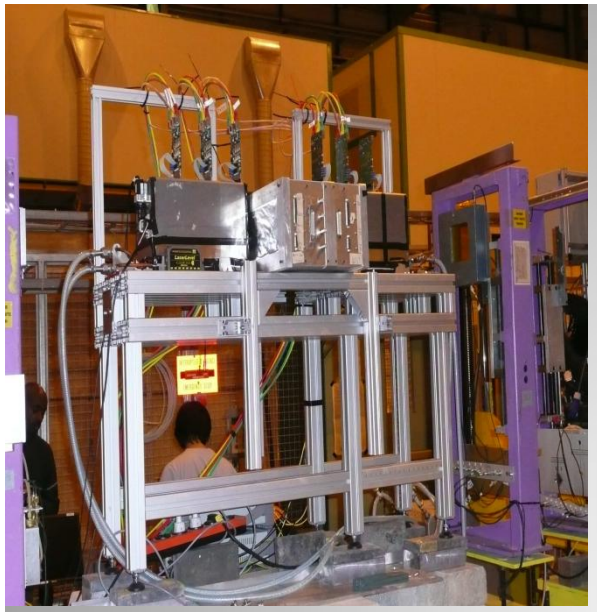


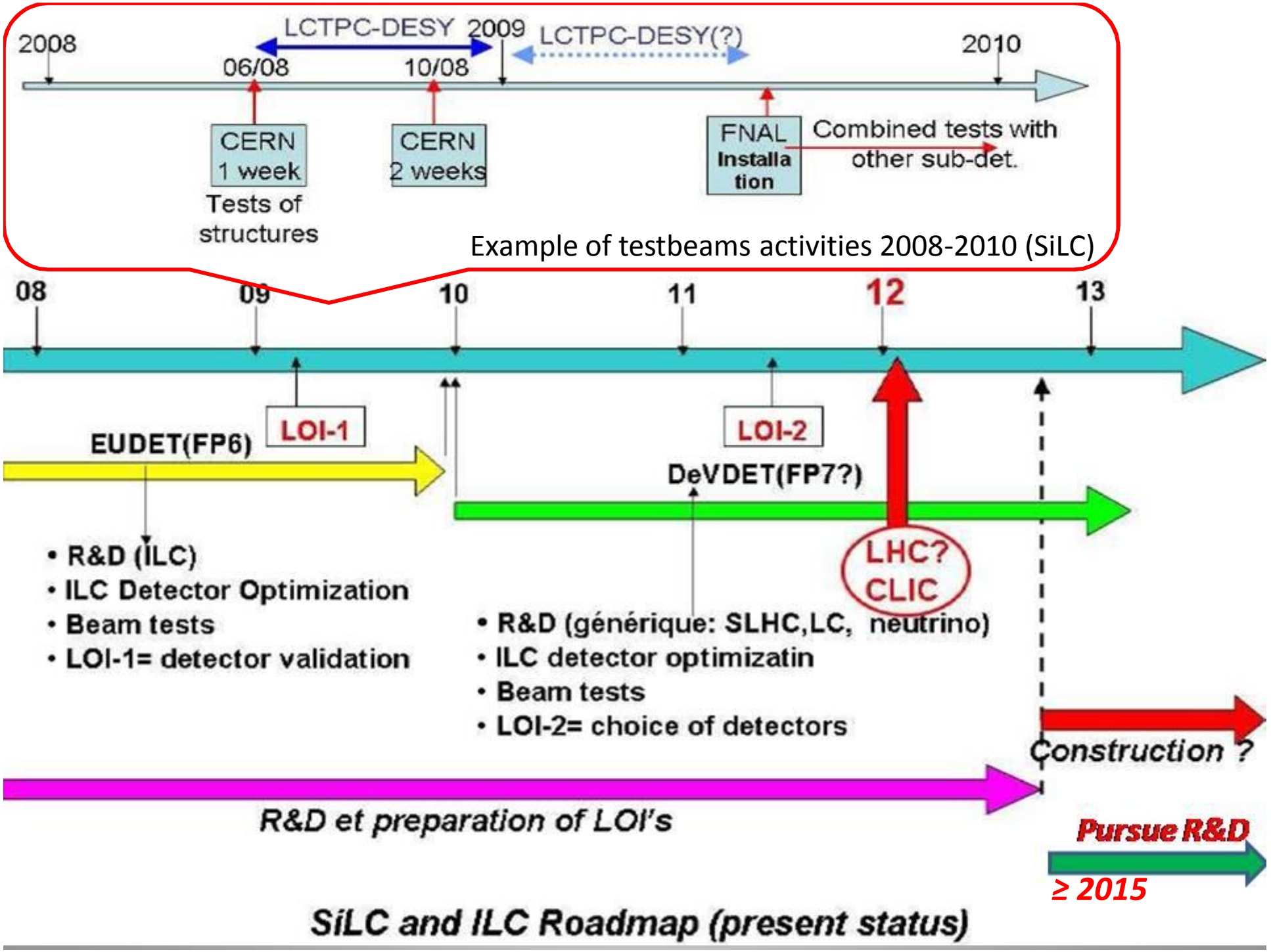


We are working on both Fronts: simulation studies and mechanical integration

PROPOSED WORKPLAN
Other crucial tool: Test beams

SiLC Test beams, ex: CERN Test Beam




2008
LCTPC-DESY
2009
LCTPC-DESY(?)
2010
06/08
10/08
CERN
1 week
Tests of
structures
CERN
2 weeks
FNAL
Installa
tion
Combined tests with
other sub-det.
Example of testbeams activities 2008-2010 (SiLC)
08
09
10
11
12
13
LOI-1
LOI-2
EUDET(FP6)
DeVDET(FP7?)
LHC?
CLIC
• R&D (ILC)
• ILC Detector Optimization
• Beam tests
• LOI-1= detector validation
• R&D (générique: SLHC,LC, neutrino)
• ILC detector optimizatin
• Beam tests
• LOI-2= choice of detectors
Construction ?
R&D et preparation of LOI's
Pursue R&D
≥ 2015
SiLC and ILC Roadmap (present status)