TPC in ILD

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NIKHEF

LC TPC Collaboration

Louisiana Tech

Americas Asia Carleton Univ. *Hiroshima Univ. *KEK **TRIUMF** *ISAS, JAXA Univ. de Montreal, *Kinki Univ. **Univ. of Victoria** & *Kogakuin Univ. **TRIUMF** *Minadanao State Univ. BNI *NIAS **Cornell Univ.** *Saga Univ **Indiana Univ. Tsinghua Univ. LBNL**

Contact persons for ILD: Keisuke Fujii, Ron Settles

Univ. of Tokyo (ICEPP)

*TUA

(*) CDC group

Europe

IIHE

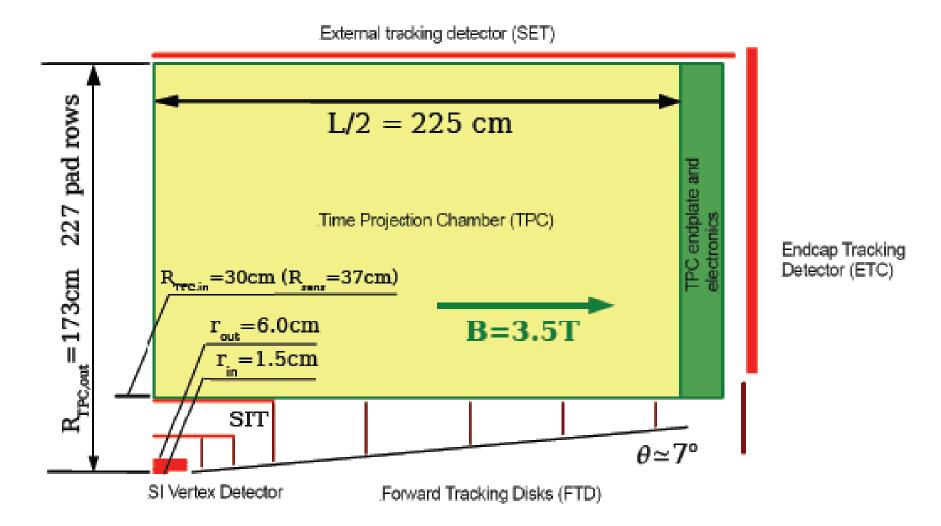
LAL, IN2P3 IPN, IN2P3 Univ. de Paris-Sud **CEA Saclay RWTH Aachen** Univ. Bonn **DESY & Univ. Hamburg Albert-Ludwigs Univ.** Univ. Karlsruhe **MPI-Munich Univ. Rostock Univ. Siegen NIKHEF BINP**, Novosibirsk PNPI, St. Petersburg **Lund Univ. CERN EUDET**

R&D Phase

- 1. <u>Demonstration Phase</u>: Provide a basic evaluation of the properties of an MPGD TPC and demonstrate that the requirements (at ILC) can be met using small prototypes.
- 2. <u>Consolidation Phase</u>: Design, build and operate a "Large Prototype" (of large number of measured points) at the EUDET facility in DESY.
- 3. <u>Design Phase</u>: Start working on an engineering design for aspects of the TPC at ILC.

We are mostly in the phase 2. However, there are still important studies of the phase 1 left, and the phase 3 is now starting together with the new ILD group.

ILD Tracking System Mokka Model LDCPrime 02Sc



From Alexei Raspereza 10/6/2008

Digitization Procedure & Spatial Point Resolutions

 Simple digitization : Gaussian smearing of SimTrackerHits positions ⇒ TrackerHits

TPC

Realistic parametrization of the TPC resolutions provided by LCTPC group (Ron Settles) [implemented by Steve]

$$\begin{split} &\sigma(r\text{-}\phi)^2 = \sigma_o^{\ 2} + D^2 \cdot L_{drift}/N_{eff} \\ &\sigma_o = (50 \mu m)^2 + (900 \mu m \cdot sin\phi_{local})^2 \\ &N_{eff} = 22/(sin\theta \cdot pad_height[mm]/6) \\ &D = 25 \mu m/cm^{1/2} \\ &\sigma(z)^2 = (400 \mu m)^2 + L_{drift}[cm] \cdot (80 \mu m)^2/cm \end{split}$$

- TPC: Aim for rφ resolution <100 μm

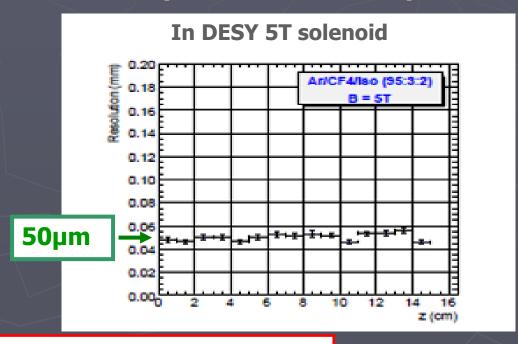
Spatial Resolution of MPGD TPC

The performance requirements for an ILC TPC greatly exceed the achievements of existing TPCs, in particular, in the momentum resolution; $\sigma(1/p_t) \sim 5 \times 10^{-5} \, \text{GeV}^{-1}$:

 \rightarrow > 200 position measurements with the point resolution $\sigma_{r\phi}$ < 100 μm . (From ILC RDR Vol. 4)

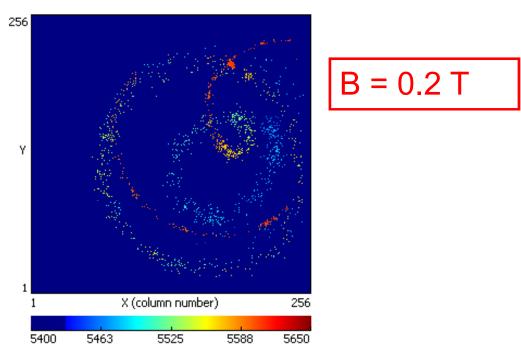
A demonstration by MicroMEGAS TPC with resistive anode In the DESY 5T magnet with Carleton TPC (M. Dixit et al., 2007)

- 2 mm x 6mm pads + resistive anode
- The small diffusion constant (20 μm/cm^{1/2}) of Ar-CF4-Isobutene (95:3:2).
- 50 μm (constant) resolution in the drift distance (max. 16 cm).
- Neff (at 0.5T) = 27-29.
- Still need to understand why 50 µm but not less.



DESY PRC presentation 1st April 2008 (Takeshi Matsuda)

- Similar results obtained for both 3-GEM and Micromegas amplification structures with pad (analog) readout
- Both these options keep being pursued
- In addition: working hard on (digital) pixel readout



Syst. error due to B-field distortions

- Allow max. 5% increase momentum error
 - \rightarrow hit measurement syst. error < 30 μ m
- "old" requirement: ∫B_r/B_z dz < 2 mm, but with anti-DID is already ~20 mm
- "abandon" old requirement; but B field must be mapped to sufficient accuracy to have syst. error $< \sigma_0$
- This implies $\delta B_{r (or \phi)} / B_z \approx 1x10^{-4}$

MDI/integration at/after Sendai

- with anti-DID: ∆Bz/Bz < 4.10-4 within 50 cm around central electrode
- The thickness of the TPC end plate is the responsibility of LCTPC, currently 10cm seems OK.
- The end cap tracker thickness depends on SilC. The distance between the two is taken as being 10cm.

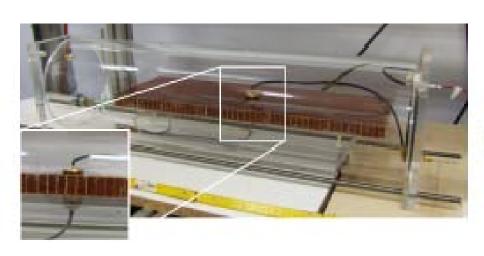
Current estimate endplate material

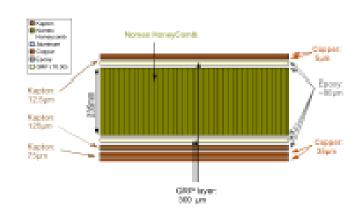
• 15% X₀

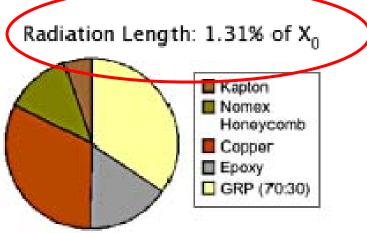
 More precise numbers, depending on different electronics options and cooling, to be worked on in next months

Sample pieces of the wall

- different possible cross sections of the investigated with sample pieces
 - \hookrightarrow high voltage tests up to $30\,\mathrm{kV}$
 - ightarrow no breakdown in $48\,\mathrm{h}$
 - - → 4-point bending tests
- \circ final layout has $1.3\,\%$ of an radiation length







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Consolidation Phase TPC Large Prototype Beam Test at DESY

Pixel beam telescope (EUDET)

Si strip detector (EUDET/SiLC)

Magnet: PCMAG (LC TPC)

Field cage & All Mechanics (EUDET)

Gas system (EUDET)

DAQ & Monitoring (EUDET)

Test beam (DESY)

Endplate (LC TPC)

MPGD Detector Modules (LC TPC)

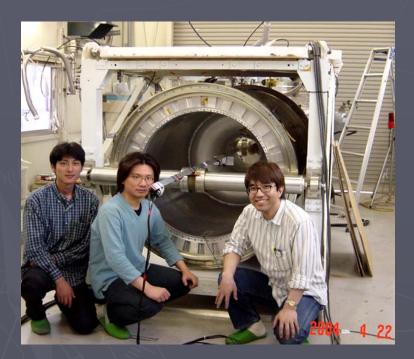
Cosmic trigger (LC TPC)

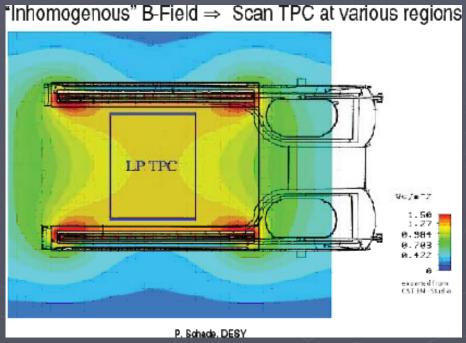
Readout electronics (EUDET & LC TPC)

Software development (EUDET & LC TPC)

Magnet (PCMAG)

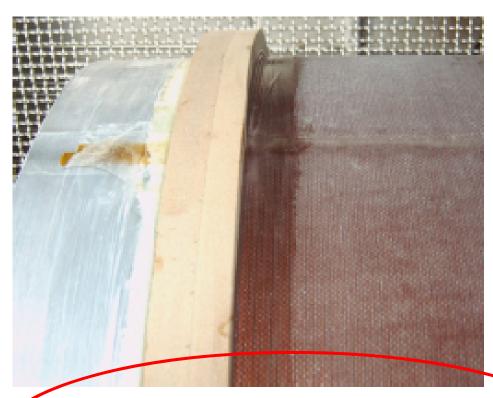
PCMAG is a Persistent Current, superconducting MAGnet with thin (0.2X0) coil and wall. It has no yoke. PCMAG was used in MP-TPC beam tests at KEK PS in 2004-200, and moved to DESY in Dec 2006 for LP1 beam test. The magnet has been tested and mapped at DESY in 2006-2007 under the cooperation of DESY, KEK and CERN groups. A new transfer tube is expected in April for safer operation, but PCMAG is essentially ready.





Coil diameter: 1.0 m, length: 1.3 m, weight: 460 kg, central magnetic filed: up to 1.2T, liq. He capacity and life time: 240L and max. 10 days, Operational current: 430A (1T), filed decay time: > 1 year, Transparency: 0.2X.

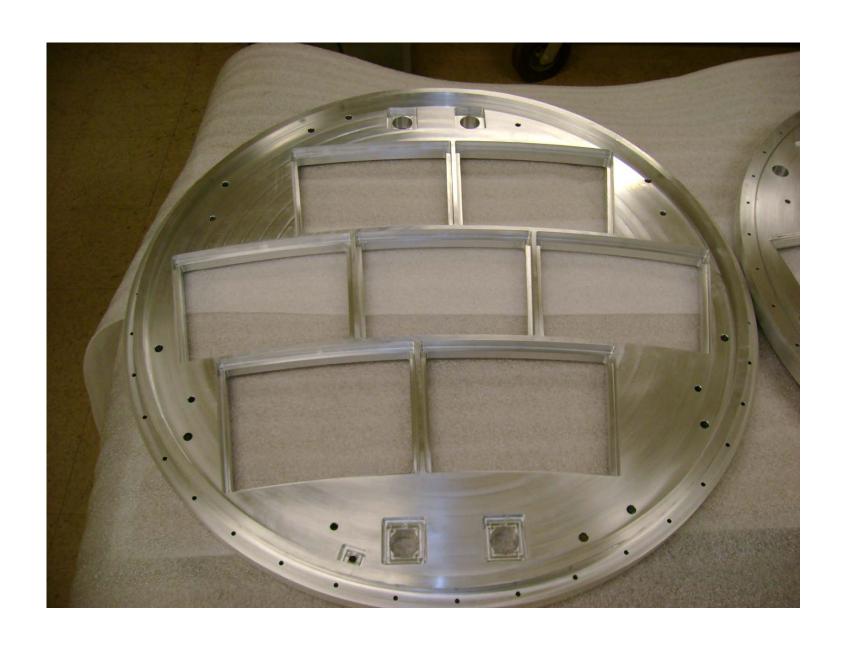
Status of the construction



- mandrel made of aluminium
 - \hookrightarrow diameter: $\Delta d \approx 0.5 \, \mathrm{mm}$
- field strip foil mounted
 - → remaining slot < 0.5 mm.
 </p>
 - → alignment worked well
- Kapton glued onto the foil
- first GRP layer attached
- epoxy is tempered at 60 °C
- flange machined and glued onto the GRP layer
- construction is expected to be finished this week.
 - field cage will be available at DESY end of June

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LP endplate ready



Single point resolution: three possible options for gasmultiplication + readout

- Need to reduce pad size relative to pad response function:
 - Resistive anode with Micromegas
 - Defocusing + narrow pads (1 mm) with GEMs
 - Digital pixel readout; avoids effects due to gain fluctuations

Detector Module: MicroMEGAS with Resistive Anode

(1) MicroMEGAS detector by the "bulk" technology (2004):

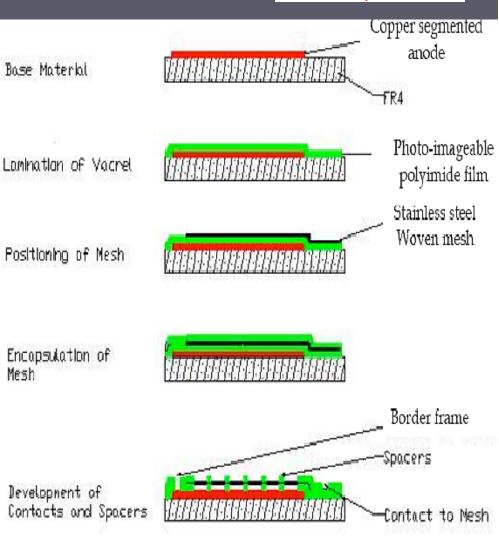
Mesh fixed by the pillars themselves : No frame needed :

fully efficient surface

Very robust : closed for $> 20~\mu$ dust

Used by the T2K TPC under construction





Detector Module: MicroMEGAS with Resistive Anode

(2) Resistive anode (RA) for the "bulk" detector:

3 techniques for the resistive coating:

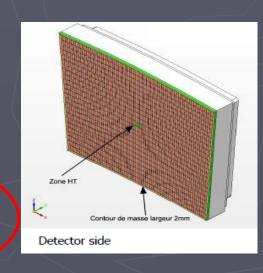
- The standard thick kapton foil laminated and covered with a resistive layer (Carleton)
- The application of amorphous silicon and doped a-Si by thin layer techniques (Neuchatel)
- Serigraphy of resistive pastes (CERN)

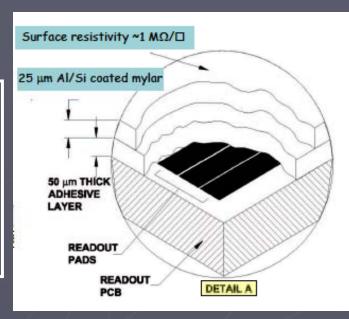
(3) LP1 detector module

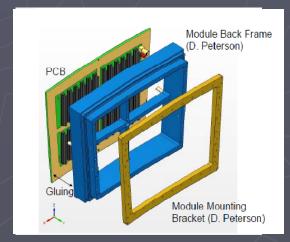
24 rows x 72 pads Av. Pad size: 3.2 x 7mm²

Layout of pad plane ready. To be submitted this week.

Depending on (2), deliver one without resistive anode at the beginning.

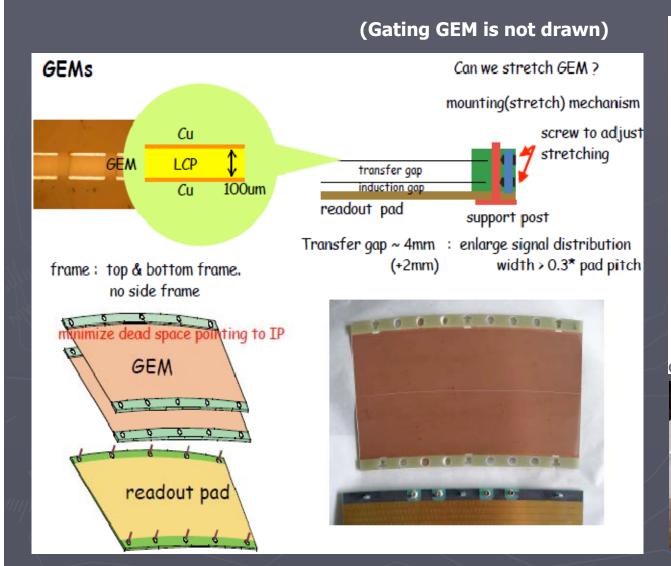


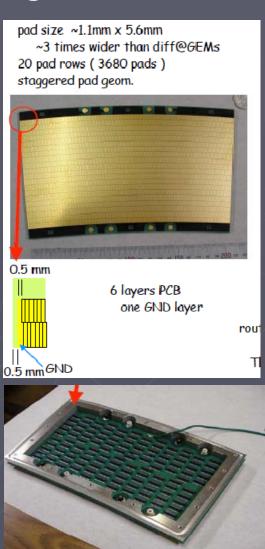




Detector Module: Double GEM with a gating GEM

(1) Double thick (100 μm) GEM with a (thin) gating GEM:





Detector Module: Double GEM with a gating GEM

(2) Pad PCB board: 8 layers

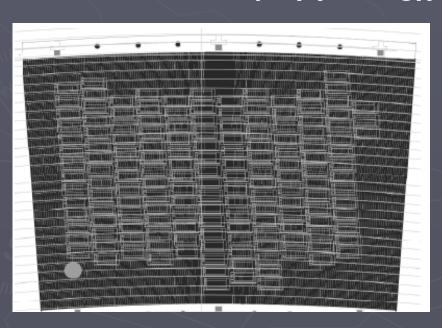
28 pad-rows x 176(192) pads for inner (outer) 14 rows Pad size: \sim 1.2 x 5.4 mm2 pads

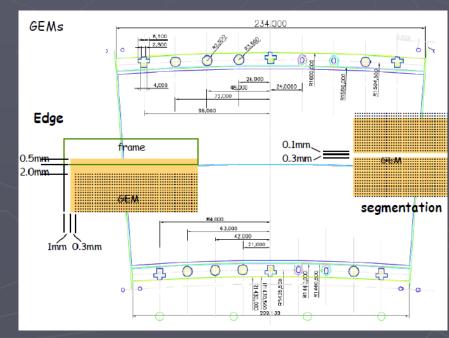
PCB layout being completed at Tsinghua Univ. Routing of GEM HV is a issue.

(3) **GEM**:

Thick GEMs are ready. The thin gating GEMs are still under work

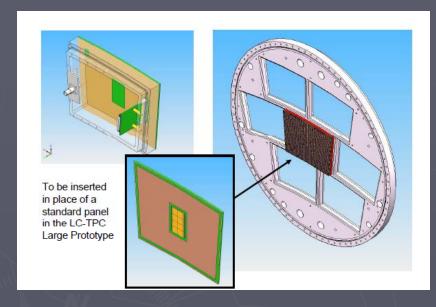
at the company (Si-energy).





Detector Modules with Timepix Chips

With MicroMEGAS (Saclay-NIKHEF)





8 chips (16 cm²)

With triple GEM (Bonn)

LP Module with 3GEM + TimePix

- ullet 3 standard GEMs 10 imes 10 cm 2
- 1 mm transfer gaps and induction
- Two quad-boards (NIKHEF) with 4 TimePix chips each



· Currently testing quad-board

anode plane

GEMs

readout plane

quad-boards reinforcement of anode plane

redframe







Design Phase: Advanced Endplate

To prove our crude estimations of 15% Xo for the TPC endplate thickness and about 170W/m² for an improved ALTRO-type electronics with power switching, we need to start a design study of the whole readout electronics chain including data transfer, and then a design study and R&D of the pad PCB plane with the flip-chip assembly. The R&D may includes simulations of power delivery, cooling and thermo mechanical features, and a test of pad PCB plane models mounted with dummy chips.

This also holds for the pixel readout option.