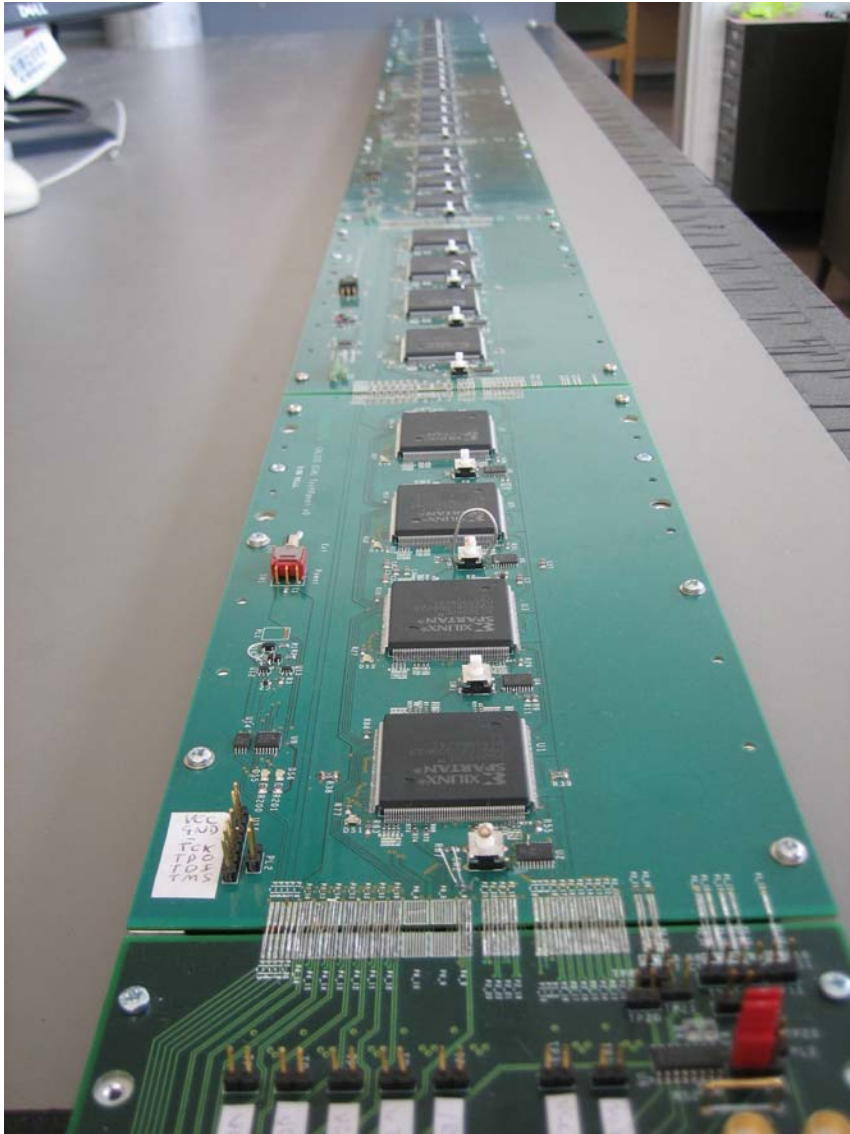


Update: CALICE test slab & DIF developments

- Slab signal distribution
- DIF status update

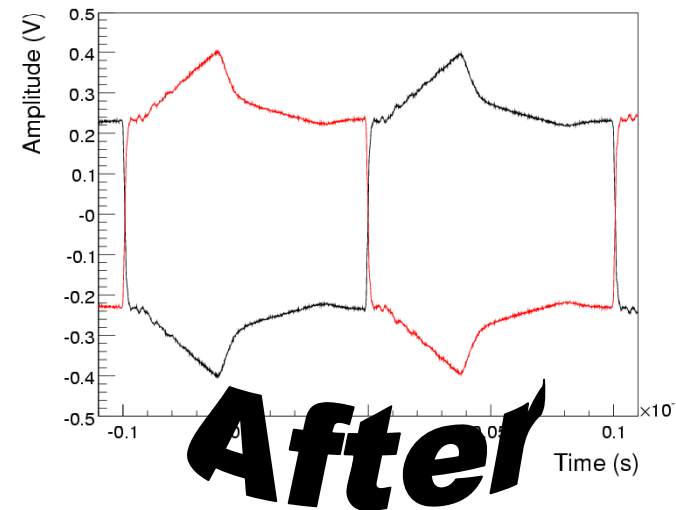
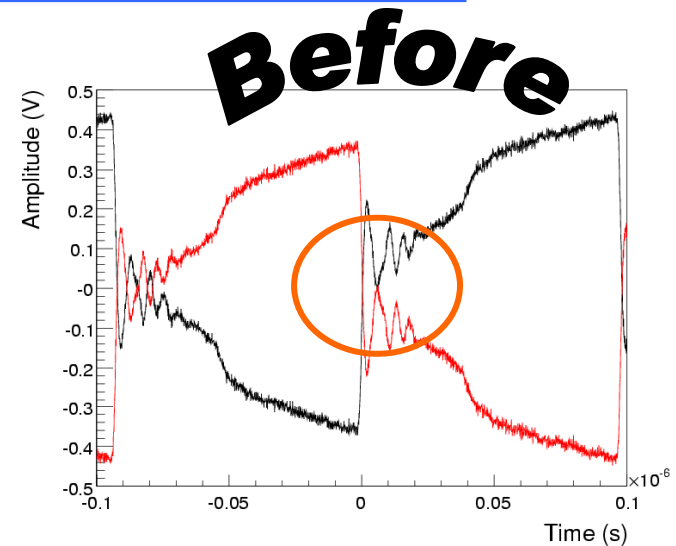
CALICE Test Slab Update



- Test slab extended to full length: 7 panels of 240mm = 1.68m
- 28 FPGAs emulating 56 HCAL VFE chips
- Clock distribution and data readout on global or panel level

Test Slab: clock glitches

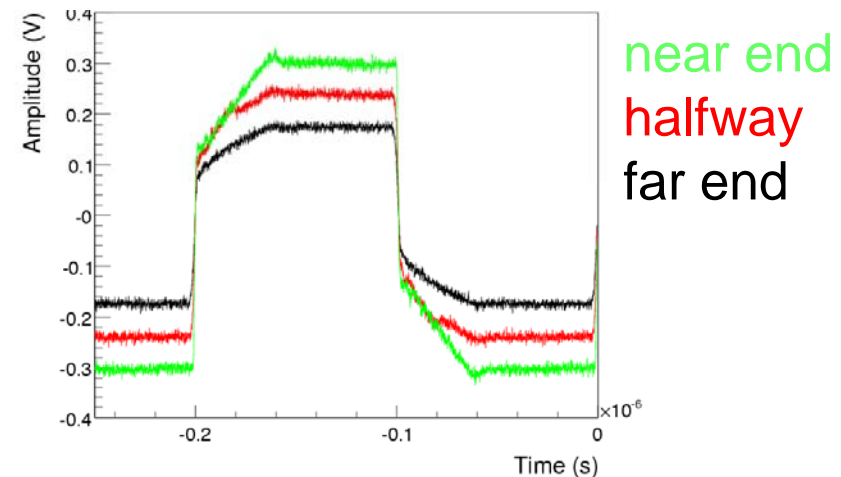
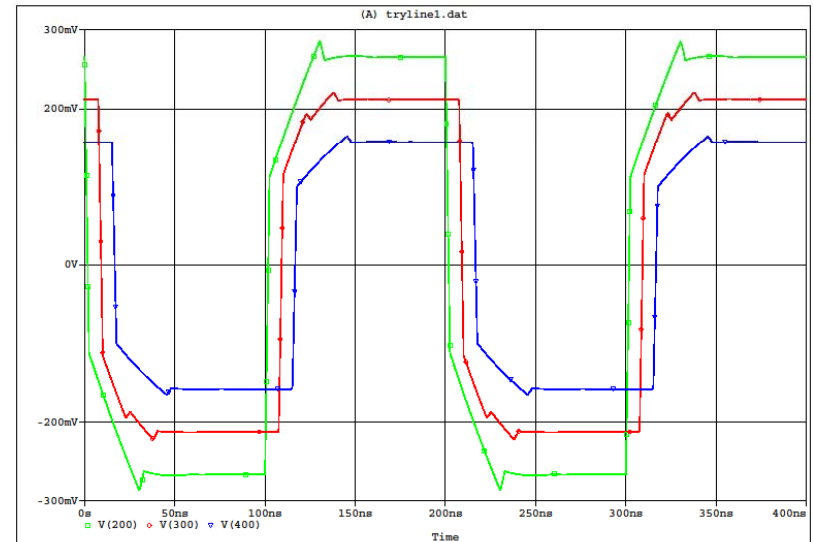
- When trying to transfer data from emulated chips: **trouble!**
- Glitches in logic caused by over/undershoots on clock lines
- Re-investigate clock propagation along slab length
- Optimal termination turned out to be way off the predicted value



Test Slab: Clock signal simulation

Slow clock: 1-5 MHz

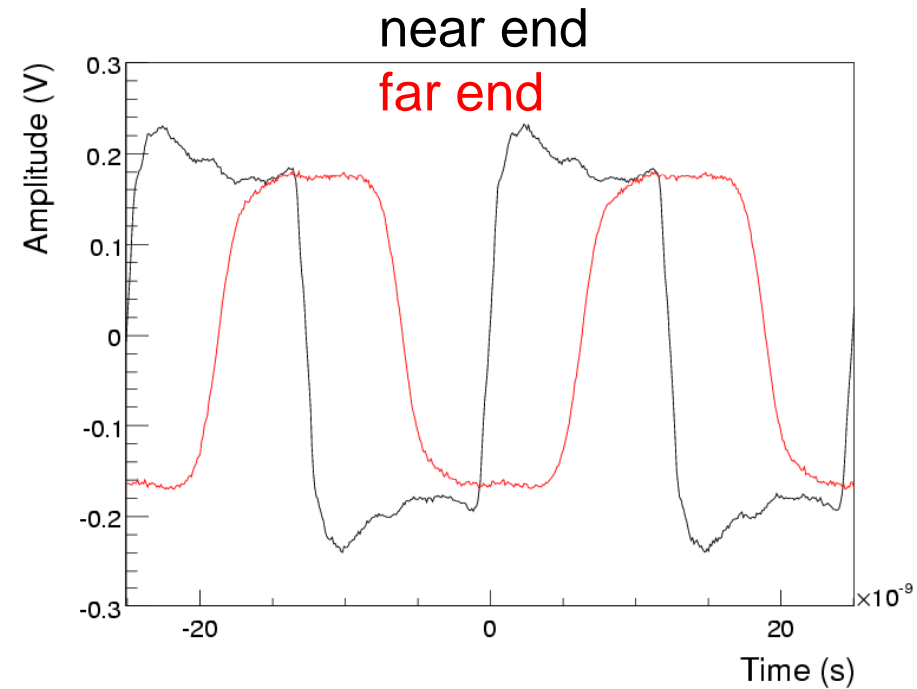
- Simulation of resistive, lossy T-line in agreement with measurements
- Optimised termination w.r.t. clock 'eye'
- Termination resistor = 30 Ohm
PCB trace resistance = 17Ohm,
LVDS driver series resistors = 10 Ohm
- Total: $10+17+30+17+10 = 84$ Ohm:
well within LVDS specs
- Recommend higher drive current:
LVDS: 3.5mA, bus-LVDS: 8mA or FPGA
output: 12mA (for Xilinx Spartan3)
hopefully sufficient for very long lines



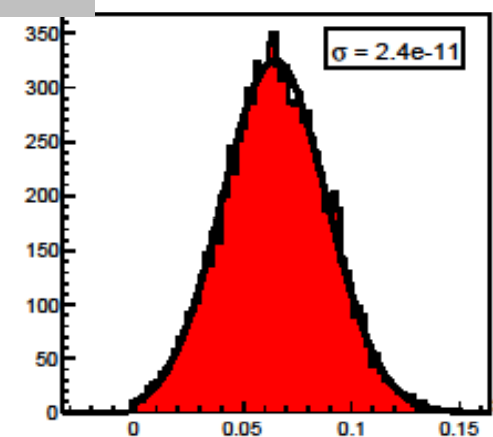
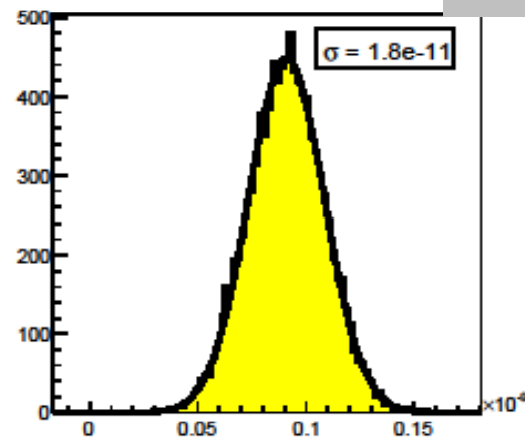
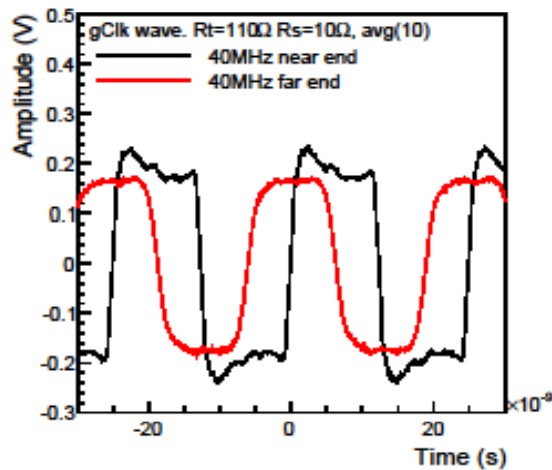
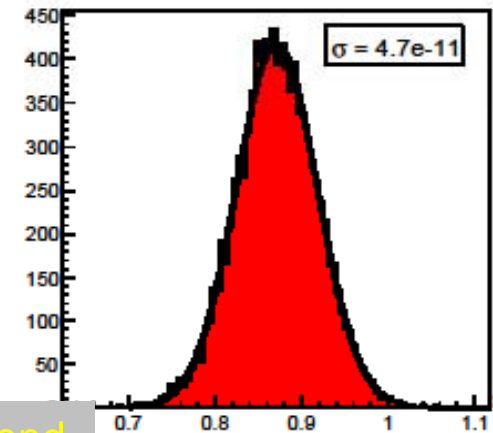
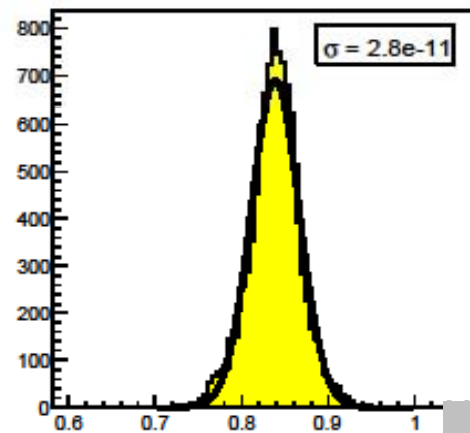
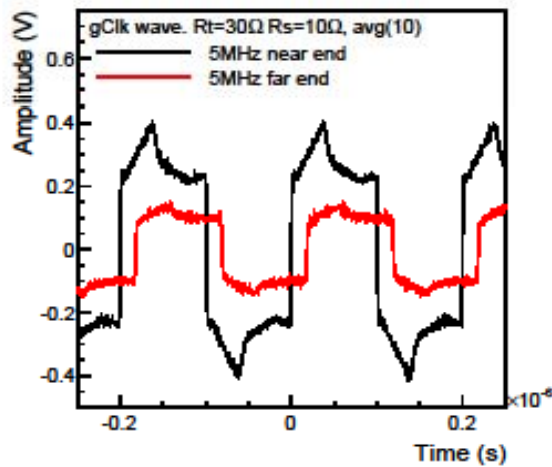
Test Slab: Fast Clock Distribution

Fast clock: 40 MHz

- Optimised termination w.r.t. clock 'eye', both on near and far end.
- Termination $R = 110 \text{ Ohm}$: undertermination, resulting in a reflected wave enhancing the far-end amplitude
- Lower amplitude than LVDS spec.
- This termination works for *this particular* frequency, and *this particular* line length.



Test Slab: Clock Jitter

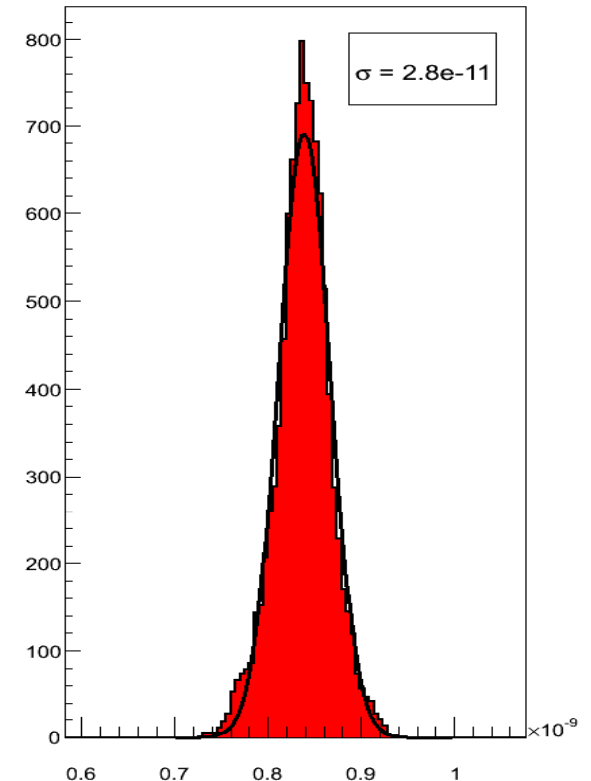
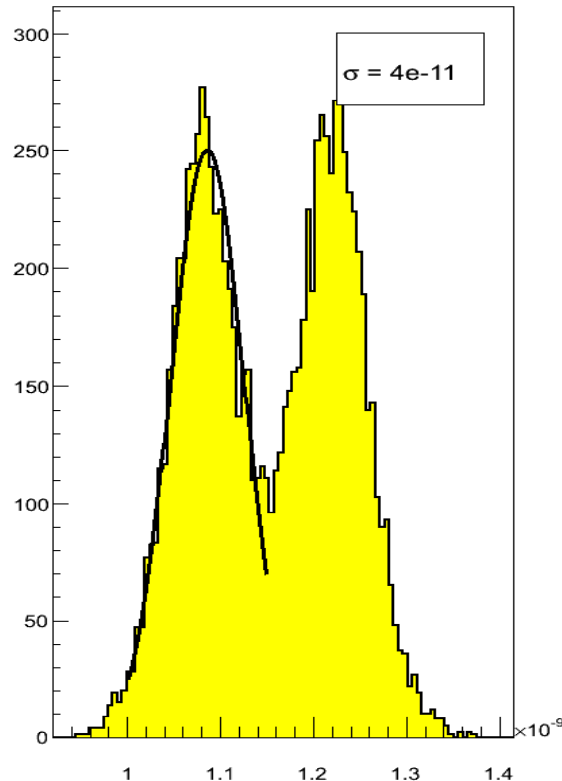
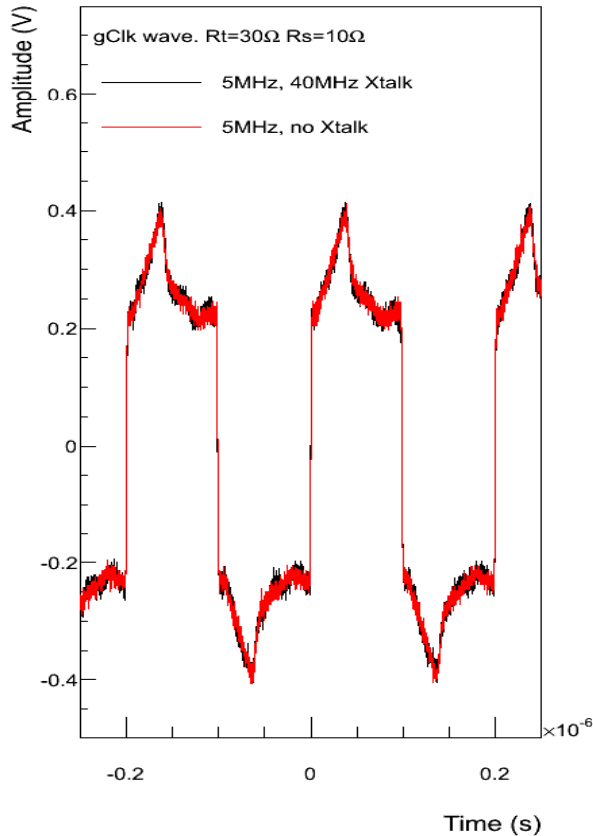


No Problems here! 😊

Test Slab: Clock Xtalk

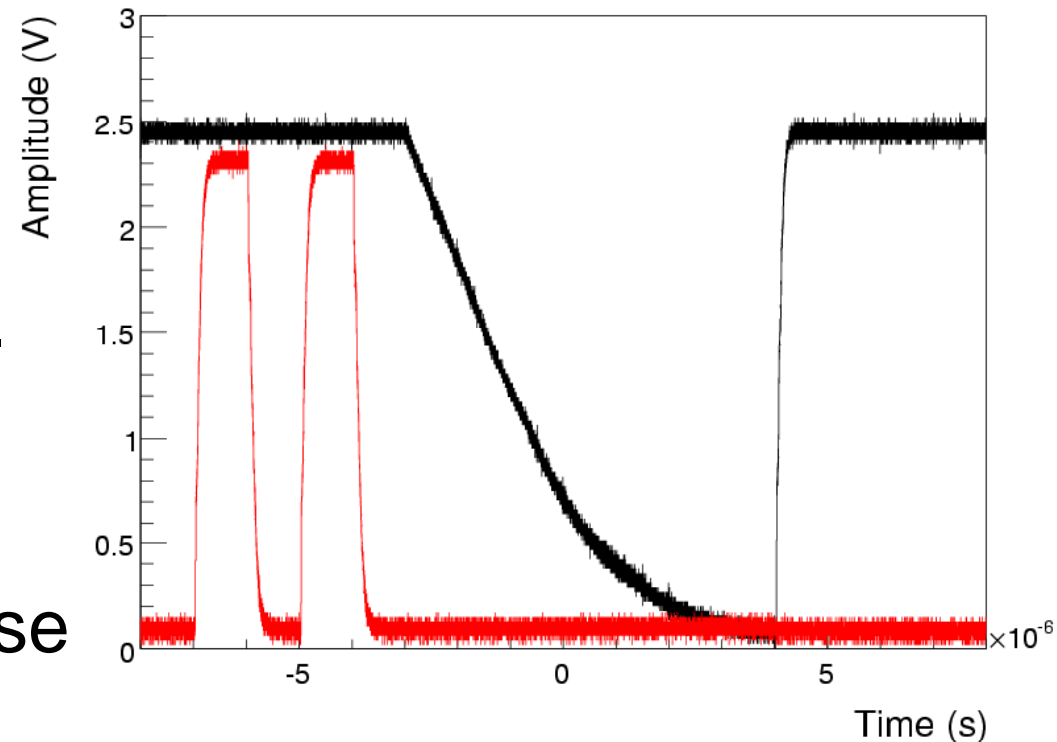
40M asynchronous clock on 5M neighbouring traces leads to increased jitter.

Still manageable, but try to avoid this by optimising layout of LVDS traces



Test Slab: TxOn and OutSerie on long slab

- TxOn: open-collector, OutSerie: tristate.
- No termination, non-optimised pulldown at DIF.
- Both 2mA drive current.
- OutSerie OK at 1MHz, but drive current has to increase for 2MHz or higher.



Test Slab : recommendations

- Jitter increases from near to far end, but is generally low.
- Xtalk should be reduced by improving layout of clock traces (see Maurice's talk)
- 2mA drive 3state is OK for TxOn, OutSerie @ 1MHz.
For higher readout speeds, drive current should increase.
- After optimisation of LVDS clock termination: no glitches 😊
- Clock propagation problems 'understood':
 - PCB trace resistance complicates T-line behaviour.
Adding another 17 μ m copper might be useful!
 - Tuning fast clock termination resistor compensates for attenuation.
- This line has a length of $t=13\text{ns}$. **What about lines with $t > T$?**

DIF status

- DIF progress suffered from slab work -sorry!
- Architecture based on collection of state machines, triggered by link commands
- ECAL DIF: Spartan3 instead of Spartan3E
- Marc Kelly made 8B/10B link available: runs fine on development boards. Compatibility with LDA assured!
- Hardware is ready: similar USB chip as other DIFs, external RAM for flexibility. Large FPGA device fitted for development, to be downscaled later.
- Firmware work is waiting... Sharing code could well save the (my) day!

DIF architecture

Same old picture of a DIF architecture proposal:

