SKIROC ADC measurements and cyclic ADC development @ LPC Clermont-Ferrand

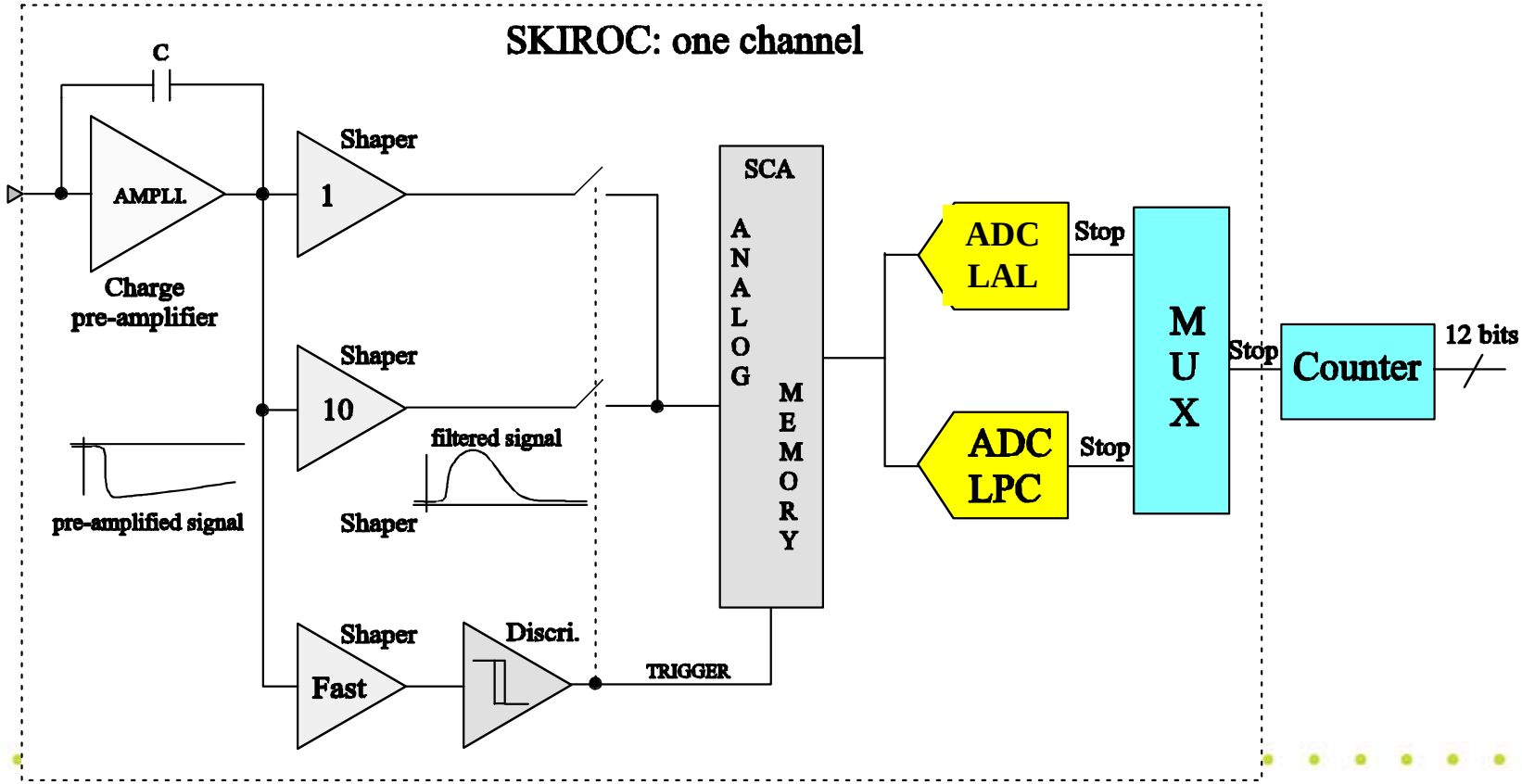
Laurent ROYER, Samuel MANEN

IN2P3
Institut National de Physique Nucléaire et de Physique des Particules

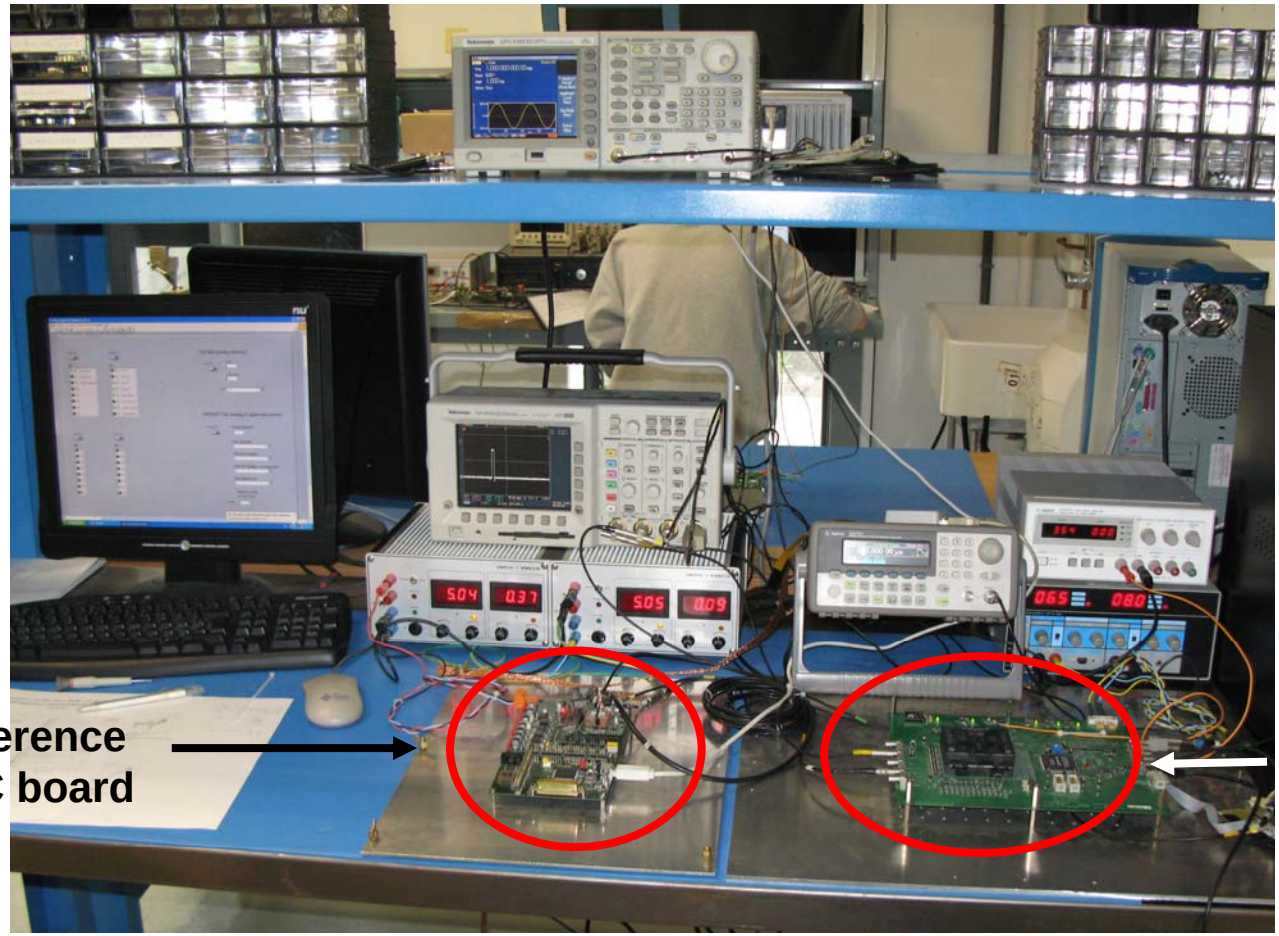
CALICE Calorimeter for ILC

Reminder: one channel of SKIROC

- Two ramp ADC: one from LAL, one from LPC
- Resolution of 12 bits, 80µs@50MHz
- Mux. to select data output with slow control
- Power pulsing implemented on ADC



Setup of test bench @ LPC



Reference ADC board

SKIROC test board

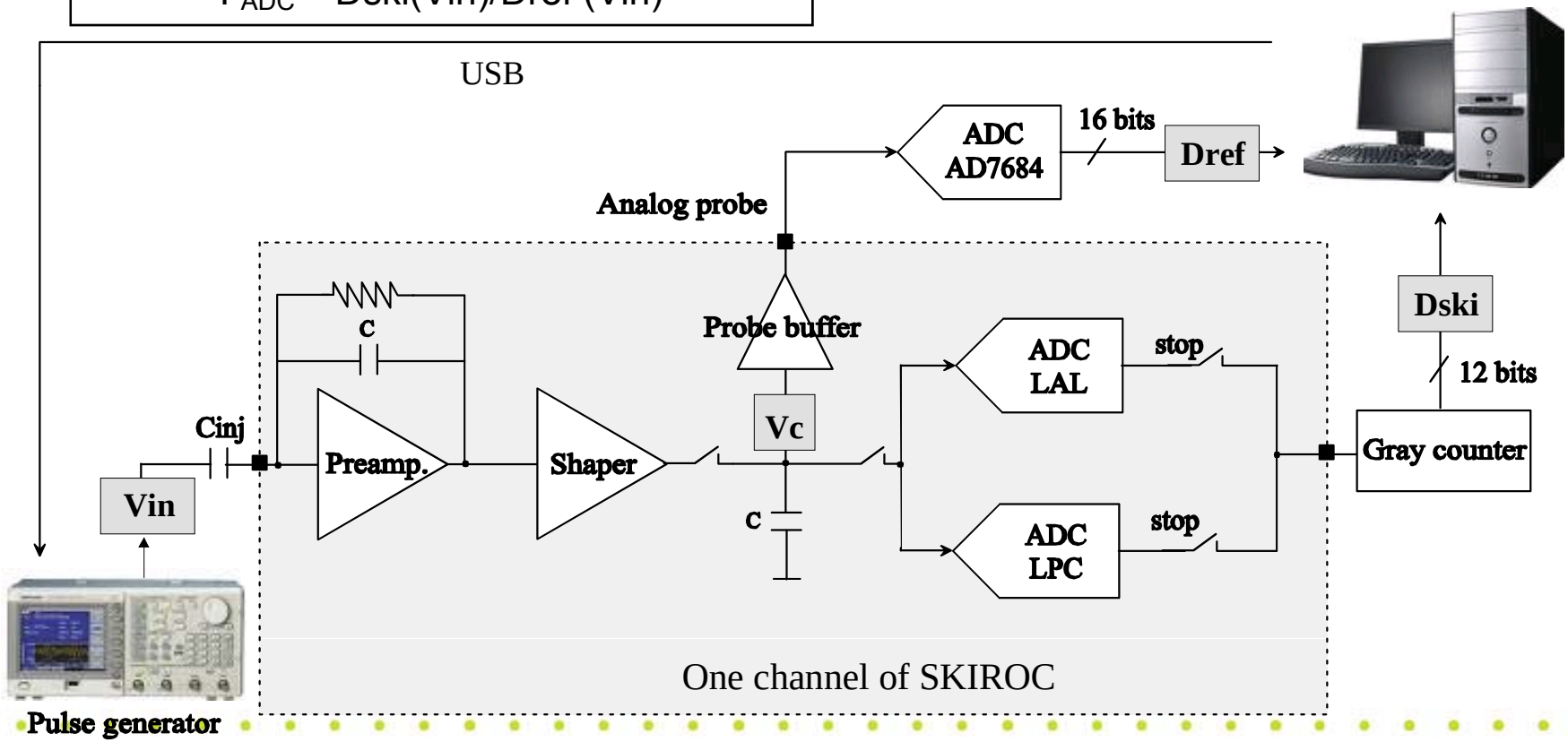
Main difference with LAL setup: external reference ADC to acquire the analog probe signal

Setup of test bench @ LPC

- Use of an external ADC to acquire the input of Skiroc ADC through the analog probe

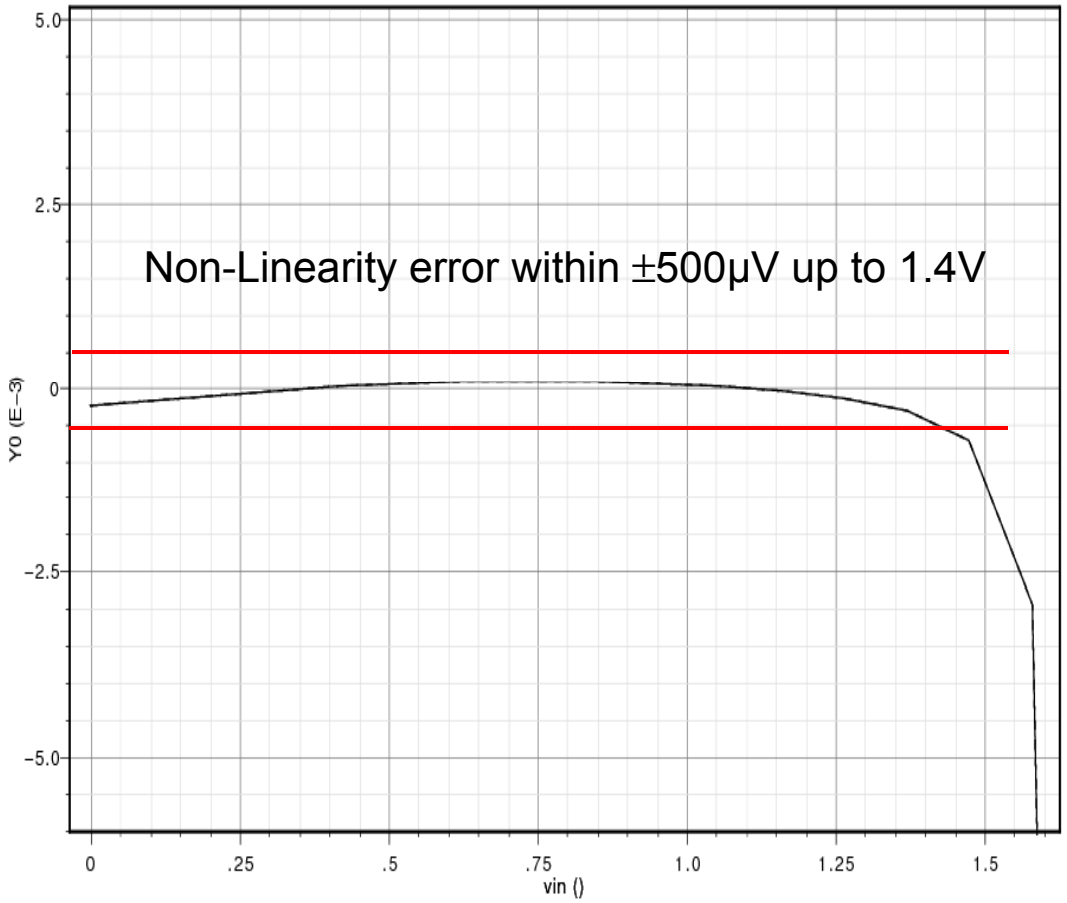
With a linear probe buffer & ADC AD7684
Function transfer of ADC under test:
F_{ADC} = Dski(Vin)/Dref (Vin)

- Automatic test with a single PC to control via 3 USB ports:
  - SKIROC
  - the pulse generator
  - The reference ADC



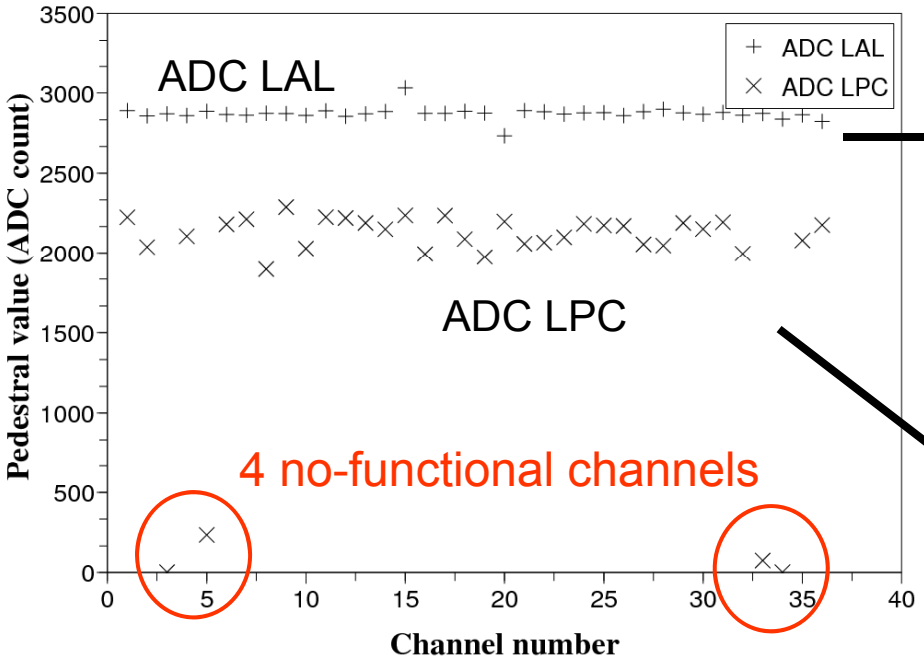
Simulated linearity of the probe buffer

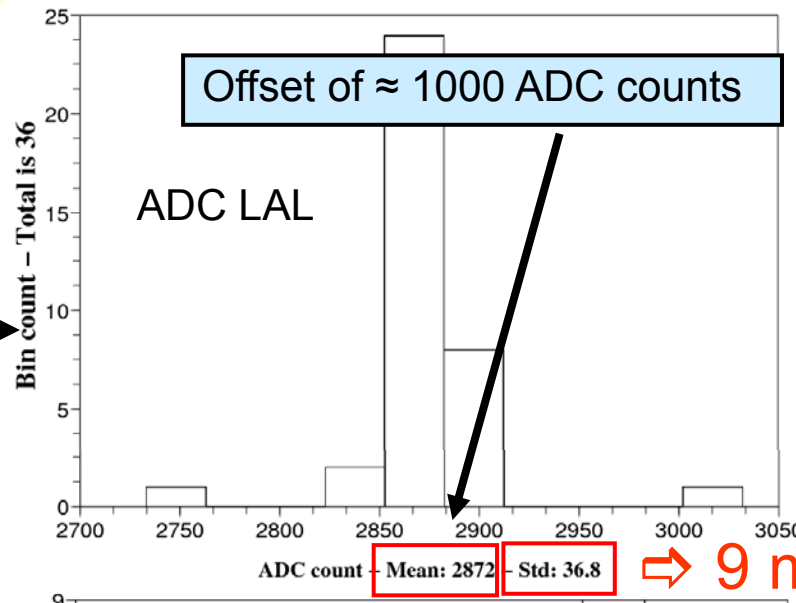
In simulation, no significant non-linearity introduced by the probe buffer



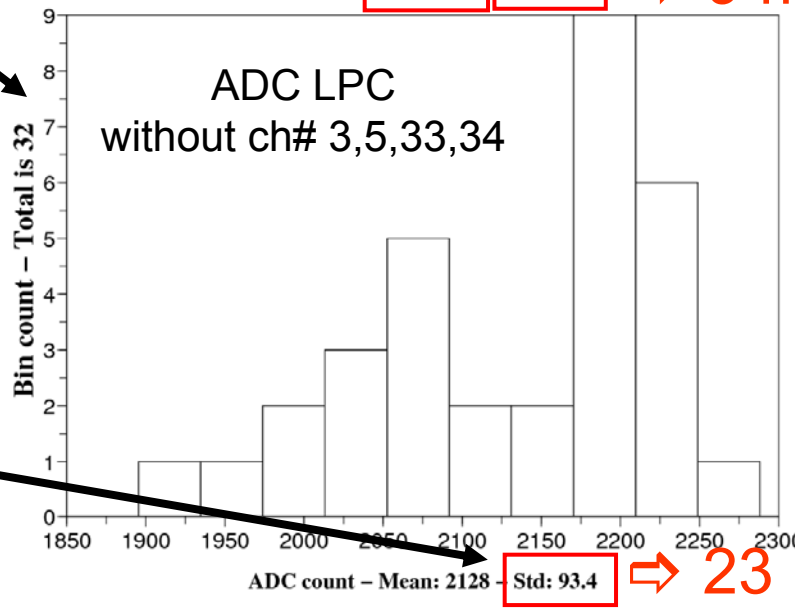
Pedestal measurements

Measurements @ ½ full dynamic range
(≈ 2000 ADC counts)





⇨ 9 mV

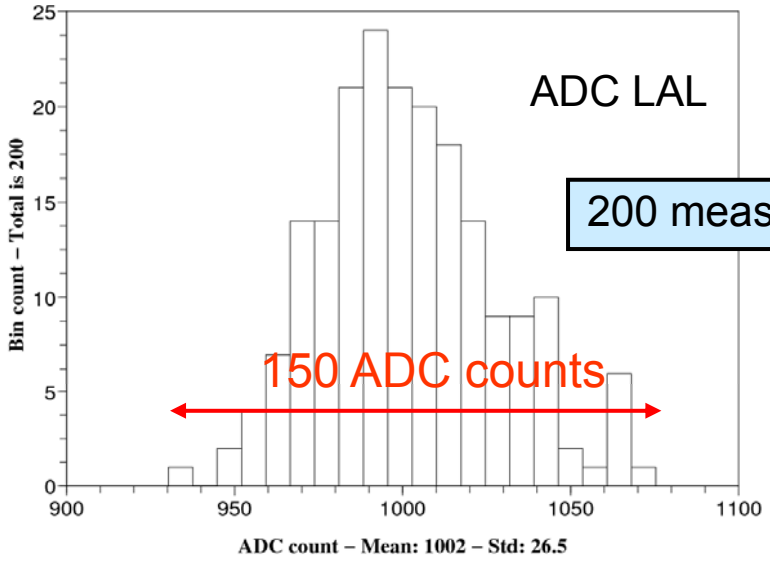


⇨ 23 mV

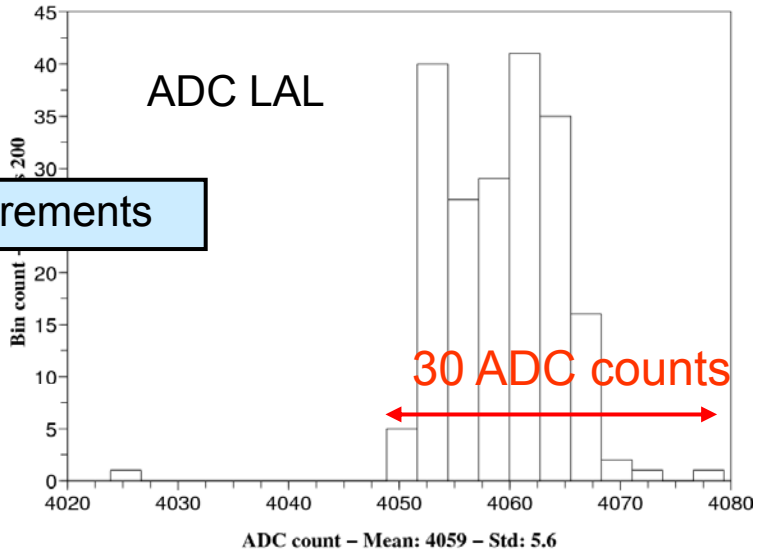
- Pedestal dispersion mainly due to comparator offsets
- Latest version comparator designed @ LPC has offset dispersion lower than 5mV (standard deviation)

Noise measurements

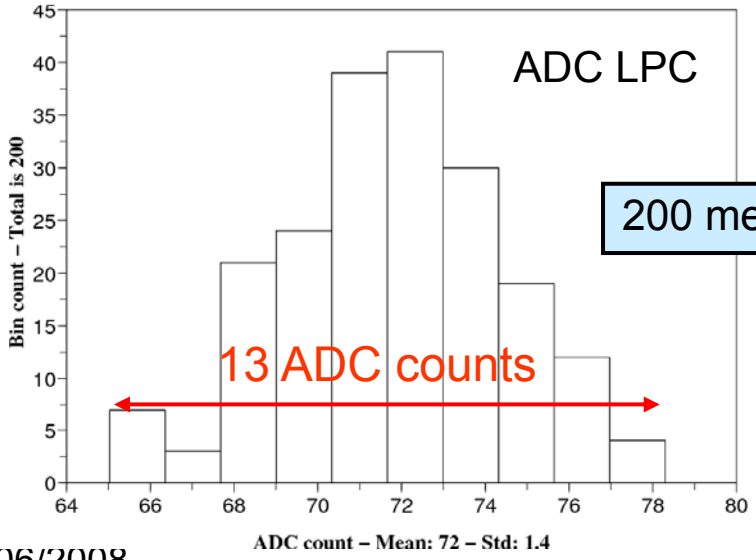
No input signal

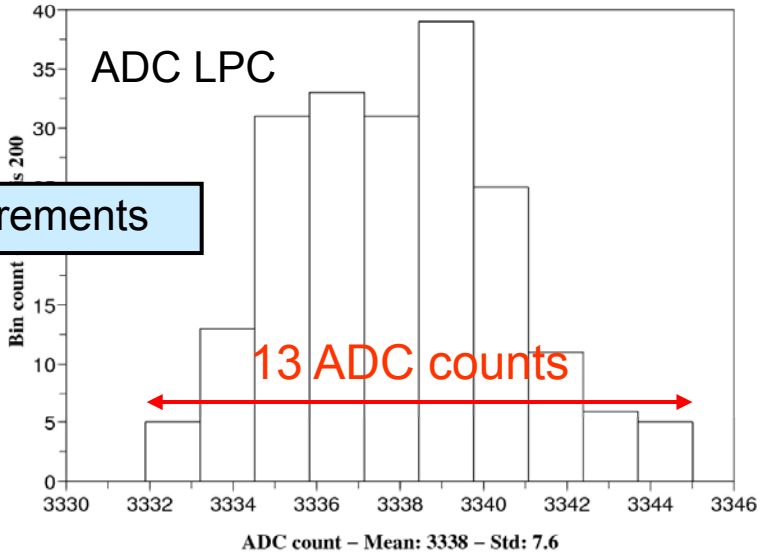


0.7V input pulse voltage



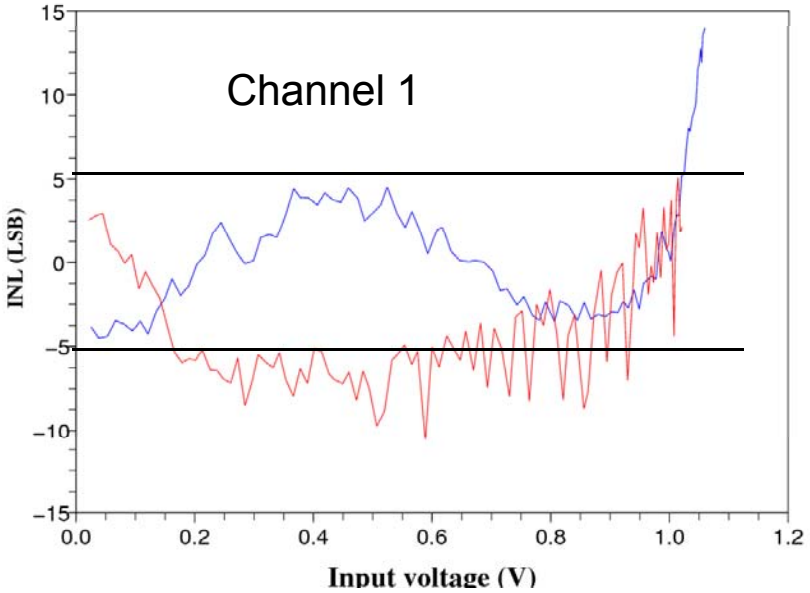
200 measurements

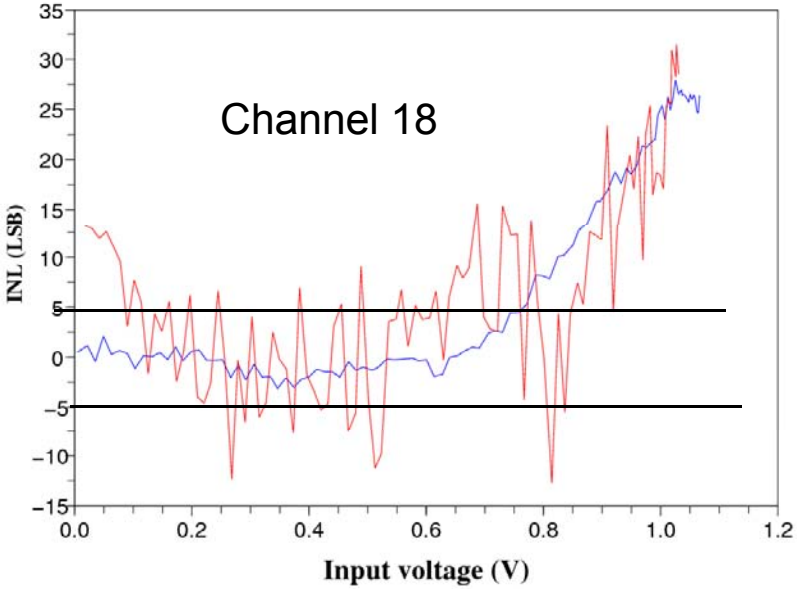




200 measurements

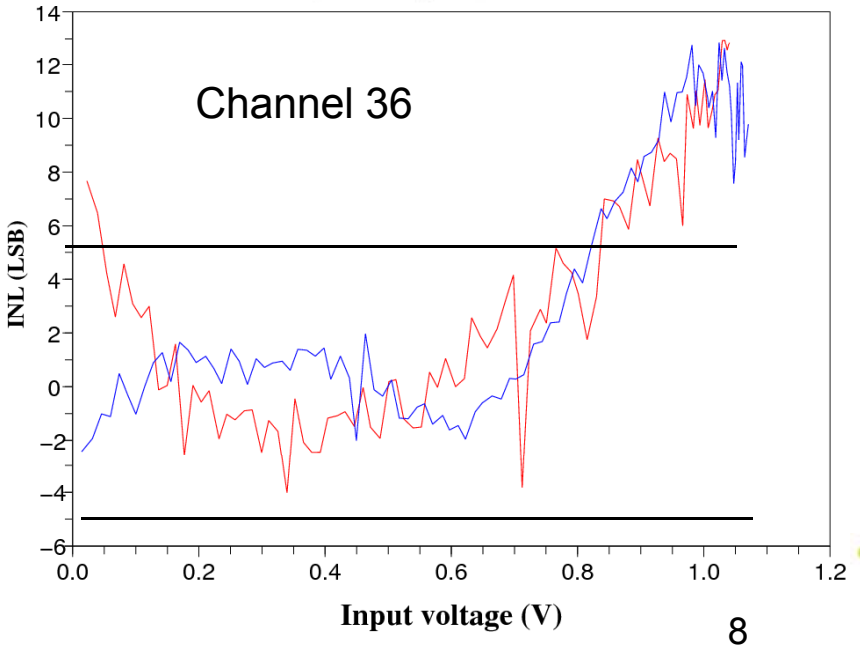
Linearity measurements





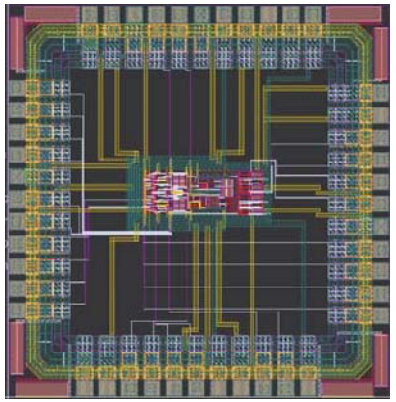
Red: ADC LAL
Blue: ADC LPC

- 200 steps from 0 to 1.1V, mean value of 10 meas./step
- Non-Linearity within ±5LSB up to ≈0.8V
- Nearly similar curves for the 2 ADCs
  - Linearity performance limited by the setup of the test ??

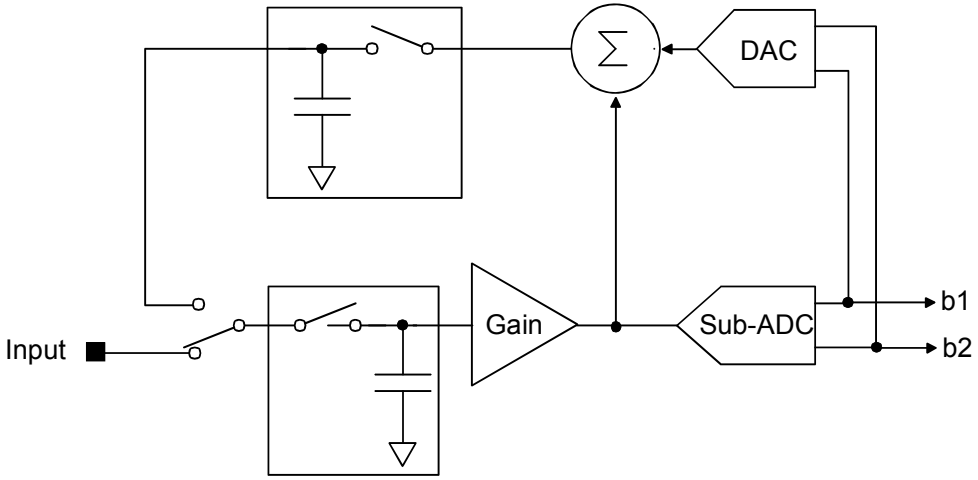


A 12-bit cyclic ADC (1)

- A 12-bit cyclic ADC sent to fabrication the 21th of March
- Delivery expected this week
- ADC designed with the validated building blocks (Amplifier & Comparator) of our 10-bit pipeline ADC (published in IEEE NS in June 08)

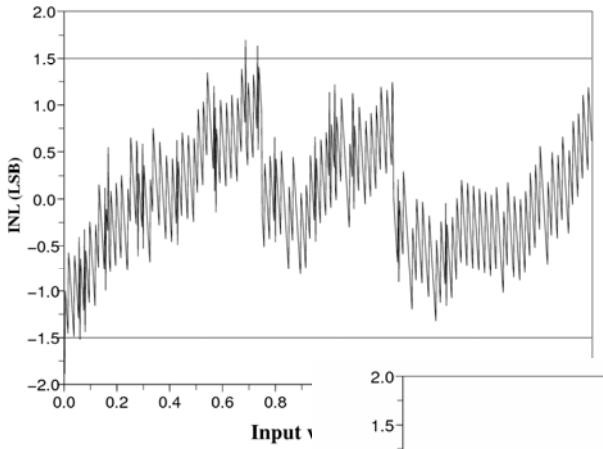


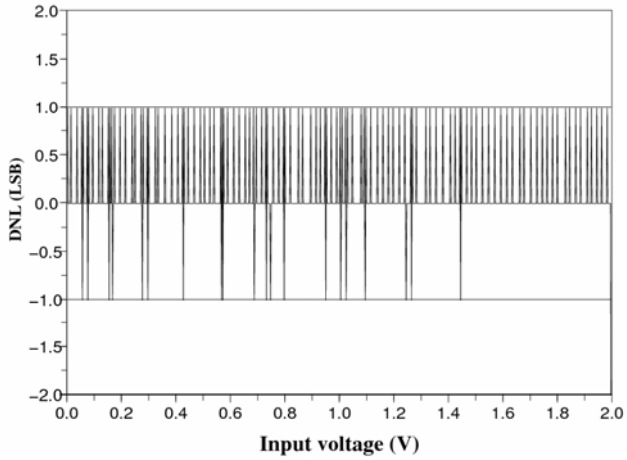
- Advantages of the cyclic architecture:
  - Small area: (700x250) μm^2
    - One ADC/channel for the final 64ch. chip
  - Intrinsic serial output data
  - Good tradeoff between speed, resolution & consumption



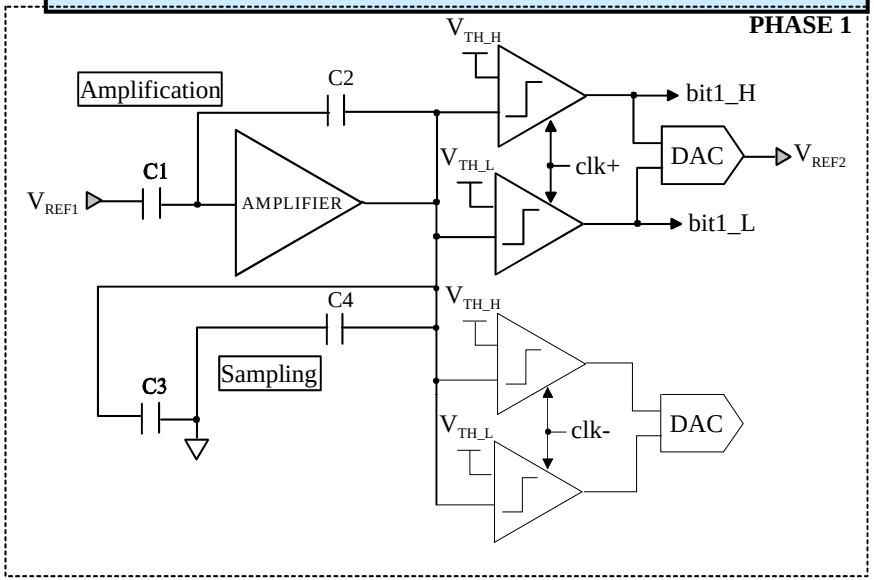
A 12-bit cyclic ADC (2)

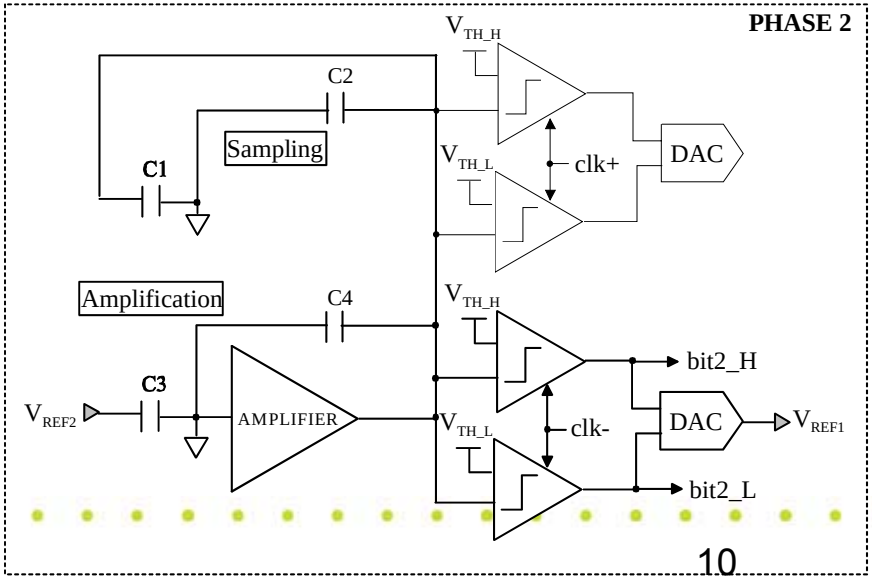
- Performance of the designed cyclic ADC:
  - Optimized architecture w/ 1 ampli. & 4 comp.
  - Time of conversion: 7µs w/ 1MHz clock freq.
  - Consumption: 4 mW
  - Integrated cons. with power pulsing: 0.12 µW
  - INL within ±1.5LSB, and DNL within ±1.0 LSB





2 conversion phases with a single ampli.





Conclusion

SKIROC measurements:

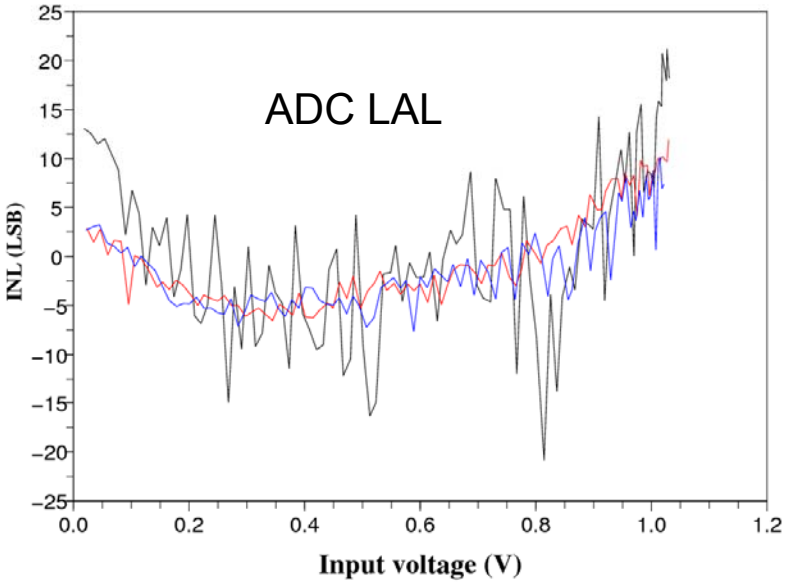
- Test bench in Clermont is now operational (thanks to Mowafak, Francois, Julien @ LAL)
- Preliminary results @ LPC show:
  - Lower pedestal dispersion for ADC LAL but offset
  - LAL ADC noisier than LPC one
  - Similar linearity for both ADC with resolution limited to ≈ 9 bits
- Discussion with LAL required :
  - To compare LAL/LPC results
  - To understand results (pedestal offset, noise vs amplitude, non-linearity…)
  - To program complementary meas.
    - Power pulsing
    - Improved linearity meas.
    - …

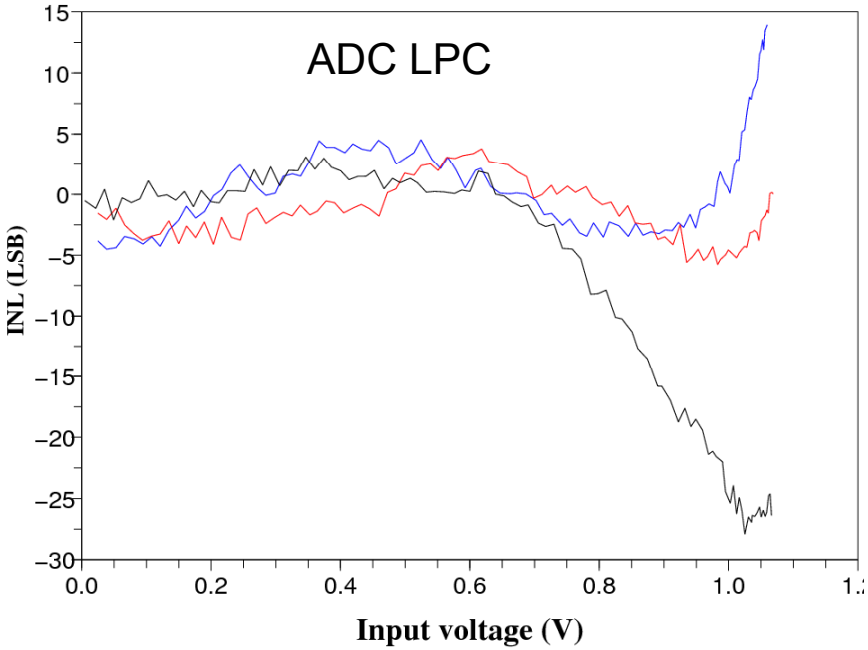
Cyclic ADC:

- Our best candidate for the final 64-channels VFE chip
- Performance of the 1st prototype evaluated in June/July

SPARE

Linearity measurements





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