

CALICE Electronics issues

2 June, 2008

Orsay Micro Electronic Group Associated

Electronics for technological modules



- Summary of Argonne meeting
- Some issues from London's meeting
- pressing issues :
 - Hardroc, Spiroc and SKIROC results and plans [Omega,LPCC]
 - ASIC Production issues
 - ECAL ASUs and signals distribution [Cambridge, Manchester, LAL, LLR]
 - AHCAL HBUs [DESY]
 - DHCAL ASUs and DIF [Lyon, LAPP, LLR]
 - Power supplies considerations
 - 3rd generation R&D [Omega,LPCC,LPSC]

HARDROC2

- HARDROC1 could go to production directly
 - No major bug
 - Measurements going on since > 1 year : still some imperfections found
 - Main drawback is package size and double row bonding yield
- HaRDROC2 could be prototyped in june 08
 - Keep HARDROC1 basic architecture and backward compatibility
 - Have 3 very different thresholds
 - Move bonding pads to single row
 - + many small changes

(gain accuracy, power pulsing...)

– Area : 25 mm2

nega

HV sparks (ESD)

- ASIC inputs:
 - protection PADs (AMS library): robustness up to 2kV HBM (100pF)
- From T2K large µmegas [E. Delagnes], AC coupling necessary for area > 10cm²:
 - Maximum decoupling capacitor that can be integrated: ≈30pF (50µm x 600 µm) and Cdet= nF loss of signal
 - EXTERNAL CAP=500 pF/ch to ensure protection
 - Drawbacks of a decoupling cap: Xtalk, space
- <u>HV sparks robustness for large GEM-like</u> detectors requires dedicated design effort

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HV

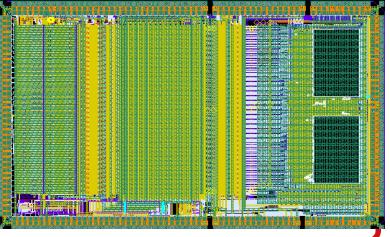
1 nF

500p

1M

SPIROC2

- SPIROC1 needs one more prototype before production
 - 2 major bugs : no probe, no ADC
 - Analog part so far OK, can be used to replace FLC_SiPM
 - Autotrigger at ~50-100 fC
 - Could be tested with existing detector and DAQ
 - Many more measurements to be done : complex chip
- SPIROC2 could be prototyped in june 08
 - If no major change
 - Possibly SKIROC compatible
 - TQFP208 package : 28x28x1.4 mm



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SKIROC2

- SKIROC1 cannot be used for detector
 - Digital part outside
 - needs one more prototype before production
 - Analog part so far OK, can be used to replace FLC_PHY3
 - Many more measurements to be done
- SKIROC2 could be SPIROC2
 - Bypass input capacitance
 - Possibly limited dynamic range
 - But ECAL PCB needs 64 channels

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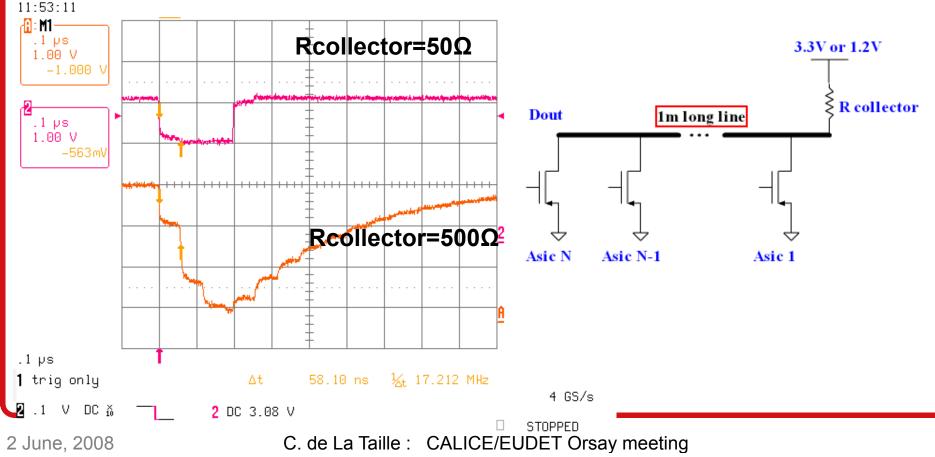
Digital part

- Digital part validated on hardroc
- VHDL code available
- Still many small changes coming up [see F. Dulucq]
 - Many improvements on Slow Control
 - Default mode
 - Last FF for daisy chain timing requirements
 - Reduce PAD number
 - Increase reliability:
 - Double some drivers
 - Possibility to disconnect bus drivers
 - Add bypass on critical signals
 - Remove "dummy frame" and improve digital operation
 - Management of PowerON for digital part
 - Start / Stop clocks
 - Start / Stop LVDS receivers...

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Open collector signals after 1m long line

- 5 m data line / slab -> 500 pF
- Multiple reflections when unterminated : 1 MHz max
- 50 ohm termination => clean, 10 MHz R/O possible, power dissipation 10 mW/slab in DIF
- Need to change driver transistor size in ASICs



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Tentative schedule

- June 08 : submission of HaRDROC2 and SPIROC2
- Sept 08 : chips in hand and for standalone tests
- March 09 : production run with HaRDROC2, SPIROC2 and (challenging) SKIROC2 (64ch)
- June 09 chips available for ASUs

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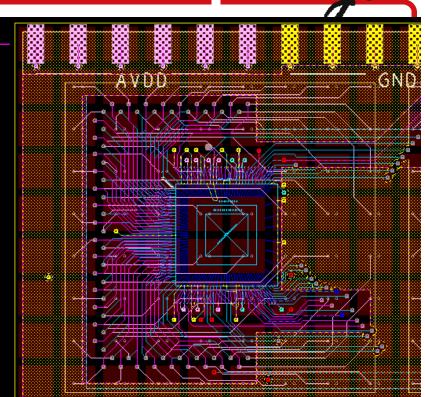
PCB developments

- ECAL : ASU prototype
 - FEV5 expected soon
 - Uses 4 HArdroc chips
 - Can test stitching
 - Connects to proto DIF

- AHCAL : HBU
 - First prototype with Spiroc

DHCAL : m2 prototype boards

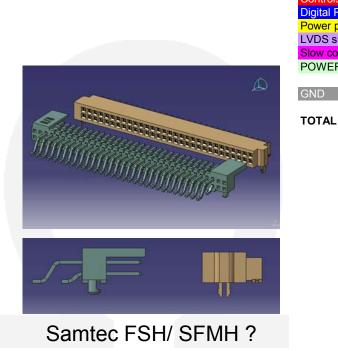
For RPCs and µMEGAS : different sizes and connections





DIF issues

- Common connector specification
- 90 pins
- Thanks to DIF task force



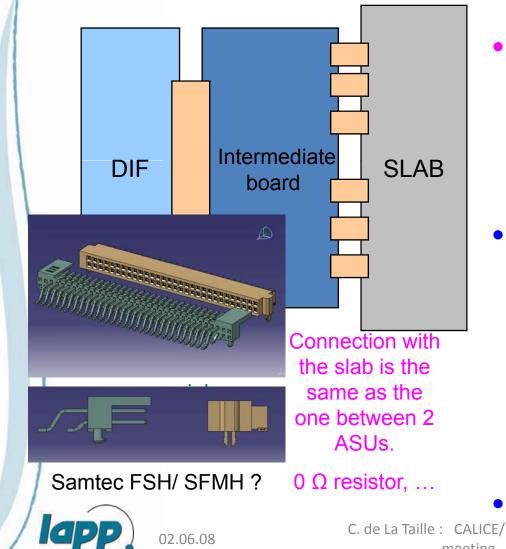
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nalog	3
Iser Single Ended	22
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igital Readout	12
ower pulsing controls	5
VDS signals	16
Slow controls signals	8
OWER pins	6
SND	13

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Clk_40MHz_1_P 81 82 Clk_40MHz_	1_N
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Raz_Chn_P 85 86 Raz_Chn_N	
/al_Evt_P 87 88 Val_Evt_N	
AVDD 89 90 AVDD	

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Interface with the SLAB



- Use of a small
 intermediate board,
 which is specific to the
 FE ASIC and ASU.
- The DIF can be used :
 - Whatever the FE ASIC.
 - Whatever the slab (RPC, uM)
 - Whatever the slab to slab connection.

• 1^{rst} ASU is the same as C. de La Taille : CALICE/EUDET Orsay meeting the others. 12



- A very critical issue !!!
- Power supplies won't be dimensionned for continuous operation, but for 1/100 of the load.
- Need local storage (capacitors, even a battery!) on power board and regulators to accomodate large voltage swing
- Simple calculation (ECAL)
 - Slab = 24 000 channels
 - 1 mA/channel unpulsed => 24 A/slab
 - With a <u>24 000µF</u> capacitor <u>dV/dt = 1V/ms => acceptable</u>

Done and to do list

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- DONE
 - Second generation ASICs prototypes
 - Auto-trigger
 - Daisy-chain readout

• TO BE DONE :

- PCB stitching (in progress)
- Tests of bonding chip on board for ECAL (in progress)
- DIF prototypes (in progress)
- Tests of power budget with existing chips and boards
- Tests of power pulsing with Imad's boards
- Integration issues (in progress)
- Design of Power distribution (no one' s looking)
- HV distribution and robustness
- Testbeam with 2nd generation detectors
- MEASUREMENTS, MEASUREMENTS, MEASUREMENTS