DIF development – Status and Common Approach

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for the CALICE DAQ and Front-End developers

AHCAL DIF Status

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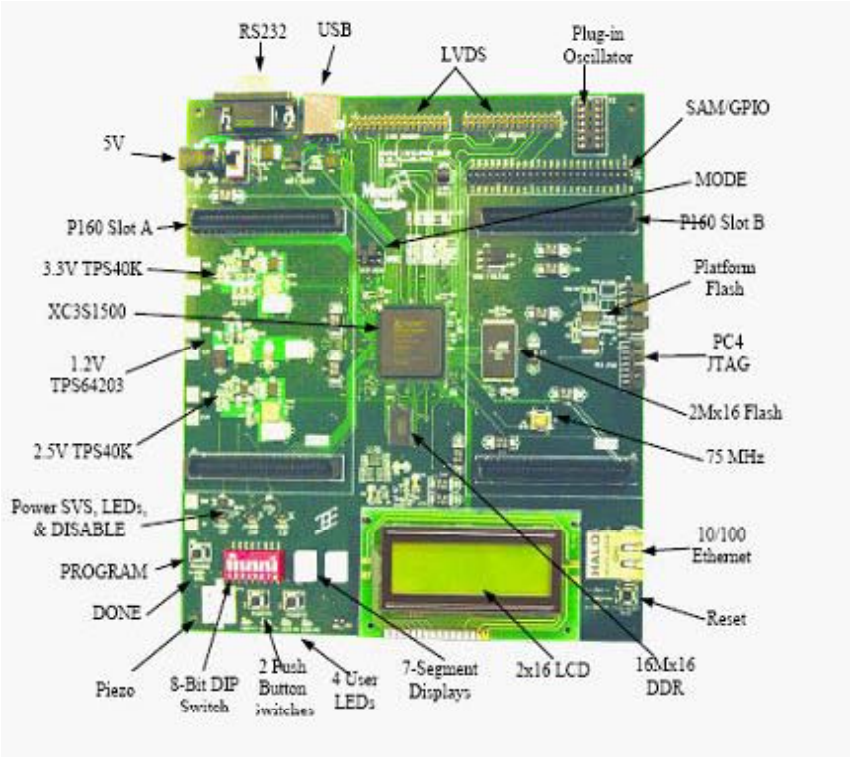

-Based on commercial FPGA (Spartan3-1500) board

-Command list and
DIF state diagram
in preparation

-VHDL code generation soon
(prototype firmware for
USB access in 2008):
Starting with SPIROC VHDL (testbench or FPGA firmware) and Altera firmware blocks from LAL SPIROC testboard (->USB).
AHCAL DIF firmware: Frantisek Krivan

Motivation I

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For the DIF firmware development, we should also take use of the similarities of the three detectors ECAL, DHCAL and AHCAL.

Possibly: Proceed as we did in the DIF working group with the hardware (e.g. DIF connectors).

Motivation II

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In the DIF group, we should clarify together:

Firmware status within DIF development groups (ECAL, DHCAL, AHCAL)?
„Are we developing firmware blocks that already exist?"

Reference documents (hardware, firmware architecture)?
„Where can I find the most-up-to-date specs.?"

How to share tasks and later firmware blocks?
„Ensure that e.g. the address decoder works in the same way for ECAL, DHCAL and AHCAL"

How to fix specifications?
„Reject changes of already fixed firmware blocks"

In order to start the collection of design parameters :

Architecture @DIF

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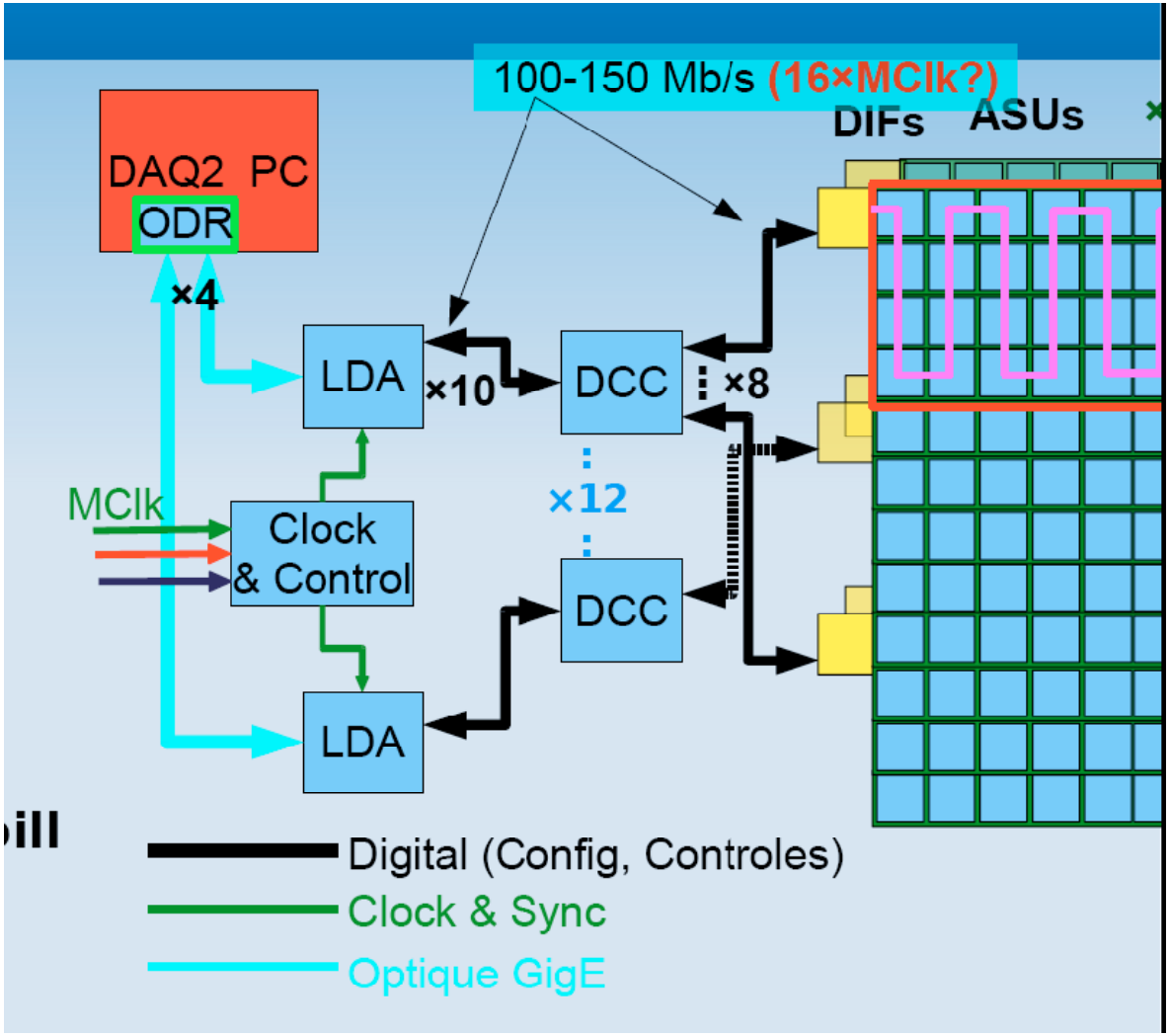

Clock: 50..100MHz (DCC to DIF)

Only one HDMI line From DCC to DIF

DCC = CCC

C&C is only connected to LDA

Vincent Boudry,
Electronics meeting July 29th, 2008

Connectors

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DIF- interm. board (to slab)

	N pins
Analog	3
User Single Ended	22
Controls Single Ended	5
Digital Readout	12
Power pulsing controls	5
LVDS signals	16
Slow controls signals	8
POWER pins	6
GND	13
TOTAL	90

GND	1	2	GND
User Single Ended 0	3	4	Analog_0
User Single Ended 1	5	6	GND
User Single Ended 2	7	8	Analog_1
User Single Ended 3	9	10	GND
User Single Ended 4	11	12	C_test
User Single Ended 5	13	14	GND
User Single Ended 6	15	16	User Single Ended 16
User Single Ended 7	17	18	User Single Ended 17
GND	19	20	User Single Ended 18
User Single Ended 8	21	22	User Single Ended 19
User Single Ended 9	23	24	User Single Ended 20
User Single Ended 10	25	26	User Single Ended 21
User Single Ended 11	27	28	Reset_BCID
User Single Ended 12	29	30	GND
User Single Ended 13	31	32	Resetn
User Single Ended 14	33	34	Start_Conv_daqb
User Single Ended 15	35	36	End_Readout
GND	37	38	Start_acq
TransmitOn_3	39	40	RamFull
Pwr_analog	41	42	Dout_3
TransmitOn_2	43	44	GND
Pwr_dac	45	46	Dout_2
Pwr_ss/Pwr_sca	47	48	Start_Readout
GND	49	50	Trig_ext
TransmitOn_1	51	52	Start_Readout_Bypass
Pwr_digital	53	54	Dout_1
TransmitOn_0	55	56	GND
Pwr_adc	57	58	Dout_0
SC_SROUT	59	60	SC_SRIN_BYPASS
SC_SROUT_BYPASS	61	62	SC_SRIN
SC_select	63	64	SC_reset
SC_clk	65	66	SC_load
User_LVDS_P	67	68	User_LVDS_N
Trig_Ext_P	69	70	Trig_Ext_N
DIF Power 3	71	72	DIF Power 2
Clk_5MHz_0_P	73	74	Clk_5MHz_0_N
Clk_5MHz_1_P	75	76	Clk_5MHz_1_N
GND	77	78	GND
Clk_40MHz_0_P	79	80	Clk_40MHz_0_N
Clk_40MHz_1_P	81	82	Clk_40MHz_1_N
DVDD	83	84	DIF Power 1
Raz_Chn_P	85	86	Raz_Chn_N
Val_Evt_P	87	88	Val_Evt_N
AVDD_0	89	90	AVDD_1

DIF working Group,
Feb.2008

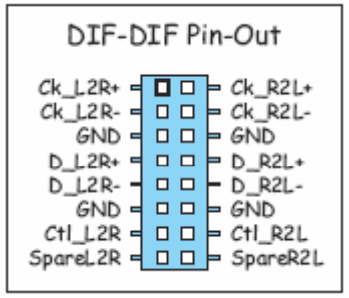
LDA-DIF

	Gnd	2	1	Clk+
	DL2D+	4	3	Clk-
Pair2 (STP)	DL2D-	6	5	Gnd
	Gnd	8	7	DD2L+
	SpD2L+	10	9	DD2L-
Pair4 (STP)	SpD2L-	12	11	Gnd
	Pow2	14	13	Pow1
	SpL2D-	16	15	SpL2D+
	Pow3	18	17	Gnd
			19	Pow4

Pair1 (STP)
Pair3 (STP)
Pair5 (UTP)

Possible Pinout for HDMI
(Based on SAMTEC HPDPI cable signal designation)

DIF-DIF



Bart Hommels,
EUDET annual meeting 2007

State Diagram DIF

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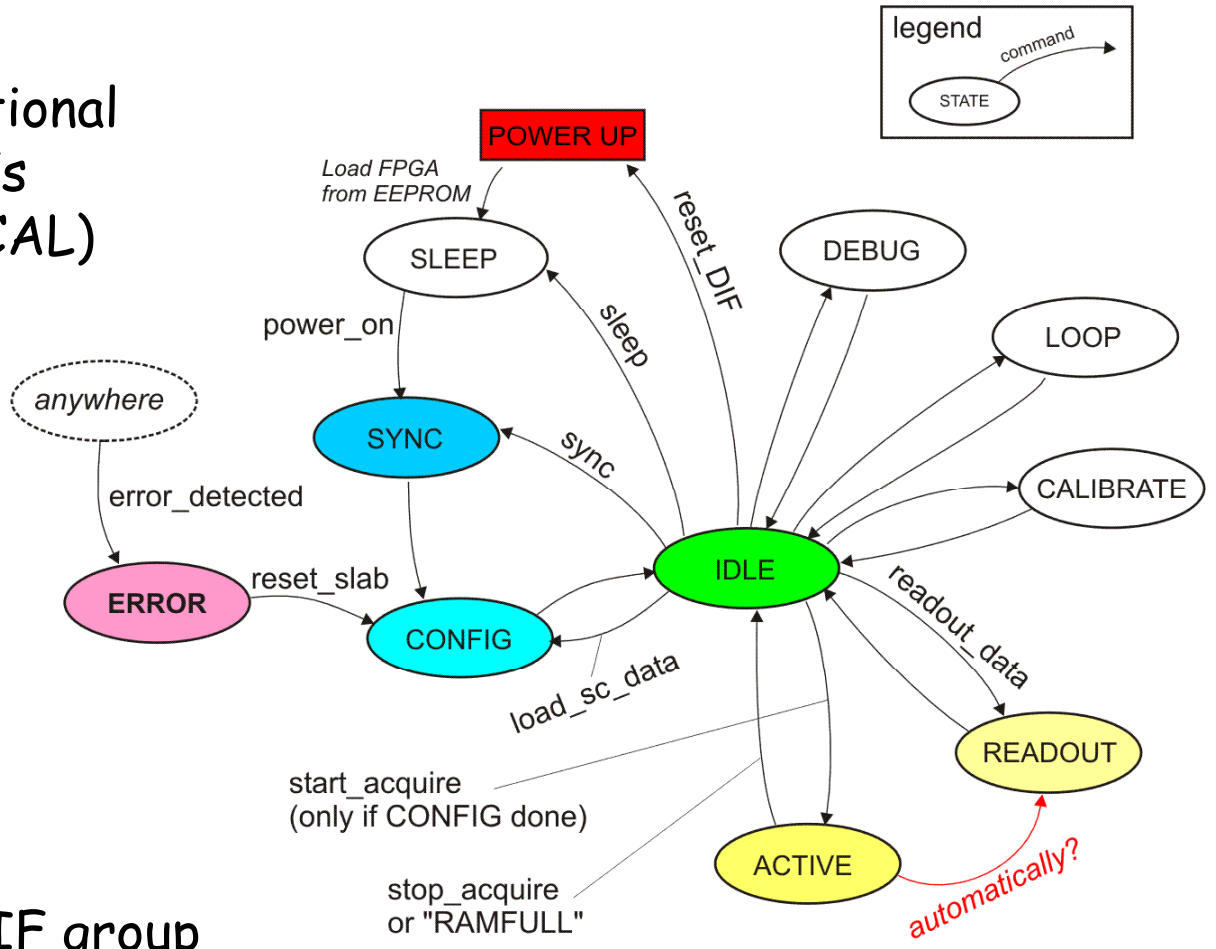
Aim: Common operational behaviour of all DIFs (ECAL, DHCAL, AHCAL)



Very first idea,
incomplete,
to be discussed in DIF group
(Aug. 2008)

Command List LDA ⇔ DIF

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Aim: Common command names in DIF firmware code (ECAL, DHCAL, AHCAL)

Very first idea,
incomplete,
to be discussed in DIF group
(Aug. 2008)

Command	Function and Parameters	Change DIF State?
power_on	turn slab power on / off (maybe partly?)	no
reset_DIF	reset of DIF electronics (not: slab)	yes
reset_slab	reset of slab (ASICs). Not: DIF	yes
reset_BCID	synchronize data taking by resetting bunch counter	no
sleep	puts DIF and slab into SLEEP state (powered down)	yes
sync	synchronization LDA all DIFs	yes
idle	puts DIF into idle state (DIF power on, slab power on minimum)	yes
load_sc_data	Load slab with slow-control data	yes
readout_sc_data	readout of actual slow control data to DAQ (in case that sc-data is stored close to DIF)	no
start_acquire	switch slab on and take data parameters: with external or internal trigger	yes
stop_acquire	stop data taking without RAMFULL (DHCAL: "ramfullext")	yes
readout_data	readout the results from slab	yes
readout_status	readout of the DIF status register	no
readout_control	readout of the DIF control register	no
readout_ID_info	several registers: Board-ID, firmware version, production date, FPGA speed grade, …	no
loopback_mode	LDA-DIF debugging: DIF into loopback mode	yes
dif_dif_link	take commands from the DIF-DIF connector	no
load_FPGA_firmware	load new firmware to FPGA via LDA	no
read_temperature	Readout the temperature sensors parameter: which sensor: DIF, slab, all	no
read_power	readout supply voltages and –currents on DIF	no
calibrate	do a calibration run parameters: with light- or charge injection	yes
calibrate_exttrig	do a calibration run with external trigger parameter: with light- or charge injection	yes
load_calib_analog	AHCAL: define analogue levels for calibration system (D/A converter setting)	no
load_calib_timing	AHCAL: define delay settings (e.g. trigger to clock)	no
readout_probe_regs	AHCAL: readout of the SPIROCs probe registers (debugging)	yes
load_uC_software	load new microcontroller software via LDA (AHCAL: on CALIB module)	no

AHCAL specific

DIF Command Sequences

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Example: What does the DIF do after a received „start_acquire"?
(sequence of ouputs to be set, timing definitions)

-check: configuration of slab (slow control) done?
-check: error registers (temperature, power failure, …)
-switch slab power(-cycling) on: „pwr_analog", „pwr_digital"
-reset Bunch Counter?: „reset_BCID"
-start data taking: „start_acqt"
-look for vetos/validations: „no_trig/Raz_Chn", „Val_Evt"
-stop data taking on „RamFull", „SCASat", or external „stop_acquire"
-start data readout automatically?

Timing Critical: All DIFs should start on the same clock cycle.

=> Common command sequencing as far as possible (e.g. ADC not in all detectors) => DIF working group

Data format DIF ⇔ LDA

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Only one HDMI connector between LDA and DIF.
Data/Commands are 8b/10b coded (firmware already available).

There are two types of frames:
1. Command Frames:
-16bit length: 8bit ‚comma char.' + 8bit command
-command[0]: DIF uses LDA or DIF-DIF input source,
command[1..7] - free for commands

2. Block Transfer (Result data and operation parameters?):
-16bit length + 16bit start-address + n*16bit data + 16bit CRC

Developed by the DAQ people: **Matt Warren, Marc Kelly, Maurice Goodrick, Bart Hommels, et al.:**
Electronics meeting July 29th, 2008

Data format DIF ⇔ LDA (CCC)

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Additionally, on the same HDMI Link (connector):

-Fast Trigger (asynchronous LDA=>DIF), pins 15 and 16, not coded
-Trainsync (synchronization of DIFs to one clock edge), pins 4 and 6, 8b/10b coded, LDA=>DIF
-GEN_IN (general purpose DIF => LDA), pins 10 and 12, not coded

Val_Evt and no_trig/RazChn on the Fast Trigger line during data taking?
RamFull/SCASat on GEN_IN line?

Can the DAQ group offer a LDA/CCC-board (or a full test environment) in order to have the same DIF test setup in all groups?

See also:
Marc Kelly's description of LDA-DIF interface: http://www.hep.manchester.ac.uk/u/mpkelly/calice/lda/Calice_LDA_Overview.html

Conclusions

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we have to decide

- if we want/need more detailed reference documents (more work at first, but maybe less effort later)

- how to coordinate the firmware development (subdivision into blocks), code repository, command list? At which level should each group proceed on its own?