Status of DCC

CALICE WEEK
University of Manchester
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Goal of DCC

- Main specification:
  - Reduce the number of LDA and ODR for the DHCAL

Remember :

3 Difs/layer (40 Layers)

10 Difs/LDA => 12 LDA and 3 ODR

- With DCC, we have need of:

  9 DIFs/DCC => 14 DCC => 2 LDA and 1 ODR

<u>Team DCC at LLR</u> :

Vincent Boudry, Antoine Mathieu, Franck Gastaldi

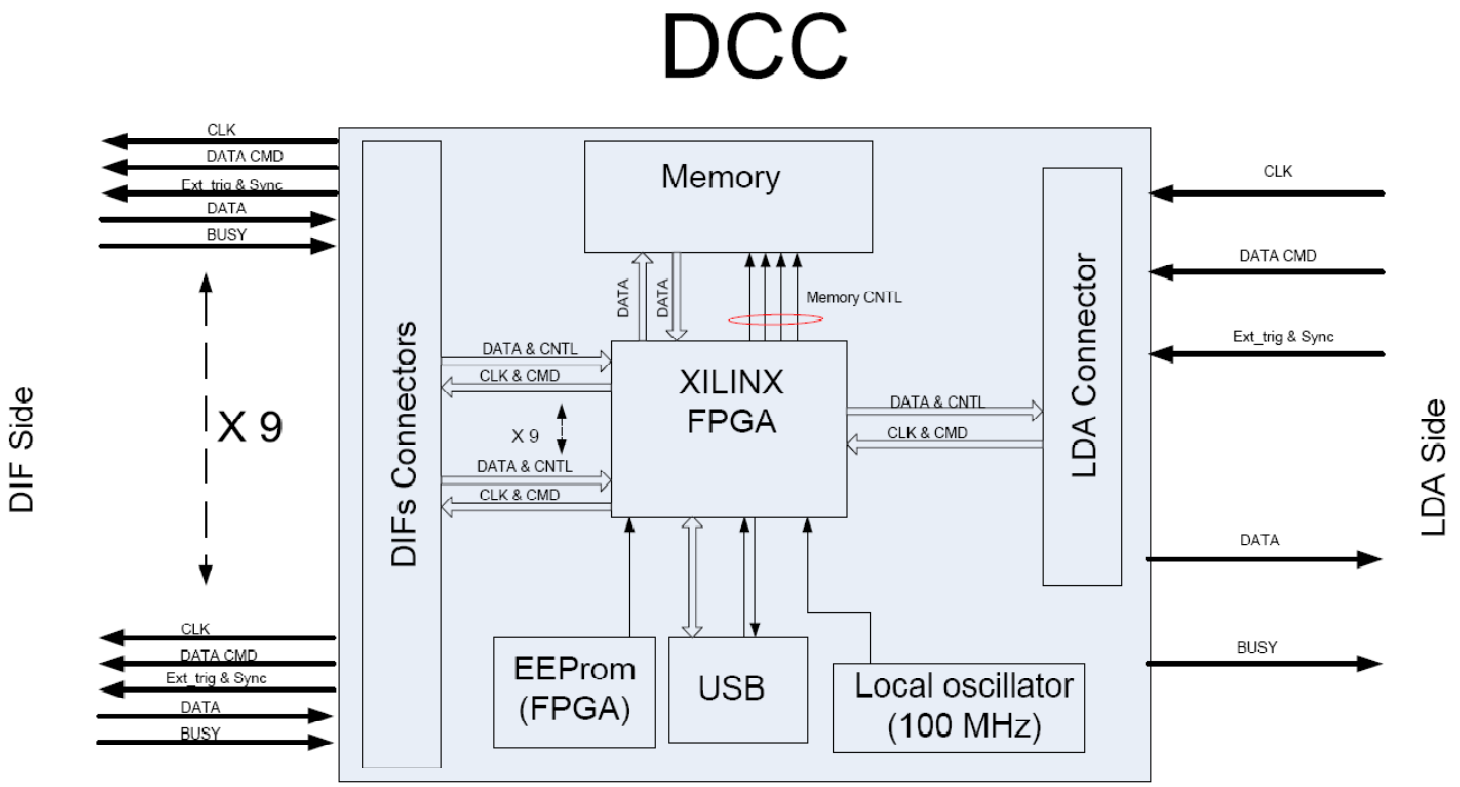
Fluxes

	N DIF/LDA	N DIF/DCC	ASIC Dclk [MHz]	ASIC FLUX [MB/s]	LDA-DIF Dclk [MHz]	LDA-DIF FLUX [MB/s]	LDA Dclk [MHz]	LDA FLUX [MB/s]
	10	9	10	1.25	80	10	1000	125
Detector	**DHCAL**		Evt Size	Mem Size				
			20 B	128			***B = Byte***	
Mode	Calib/Noise Single	Calib/noise Burst	TB Single	TB Burst	Demo			
N ASIC/DIF	48	48	18	18	18			
ASIC	20 B	2 560 B	20 B	2 560 B	2 560 B			
R/O time 1	*16 µs*	*2 048 µs*	*16 µs*	*2 048 µs*	*2 048 µs*			
R/O time ALL	*768 µs*	*98 304 µs*	*288 µs*	*36 864 µs*	*36 864 µs*			
DIF	960 B	122 880 B	360 B	46 080 B	46 080 B			
R/O time	***96 µs***	***12 288 µs***	***36 µs***	***4 608 µs***	***4 608 µs***			
LDA w/o DCC	9 600 B	1228 800 B	3 600 B	460 800 B	460 800 B			
R/O time	***77 µs***	***9 830 µs***	***29 µs***	***3 686 µs***	***3 686 µs***			
DCC	8 640 B	1105 920 B	3 240 B	414 720 B	414 720 B			
R/O time	***864 µs***	***110 592 µs***	***324 µs***	***41 472 µs***	***41 472 µs***			
LDA w/ DCC	86 400 B	11059 200 B	32 400 B	4147 200 B	4147 200 B			
R/O time	***691 µs***	***88 474 µs***	***259 µs***	***33 178 µs***	***33 178 µs***			
Max R/O time	***864 µs***	***110 592 µs***	***324 µs***	***41 472 µs***	***41 472 µs***			
Max Freq	1.16 kHz	0.01 kHz	3.09 kHz	0.02 kHz	0.02 kHz			
Max evts Freq		1.16 kHz		3.09 kHz	3.09 kHz			

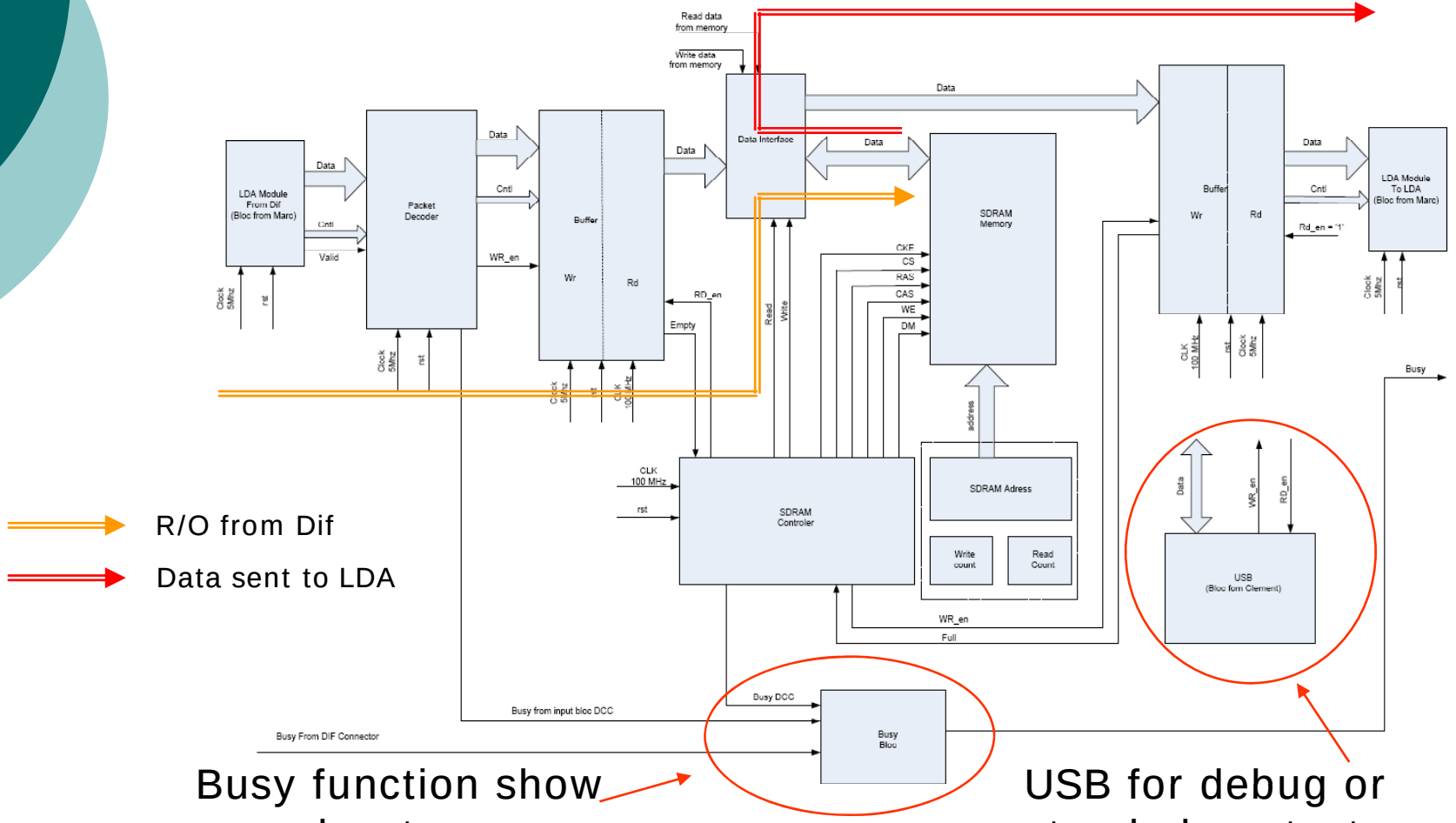
w/o DCC, the LDA r/o time is close to DIF r/o time

Remark : With a DCC, the flux between DIF and LDA is optimized and the cost will be moderate

Overview of DCC

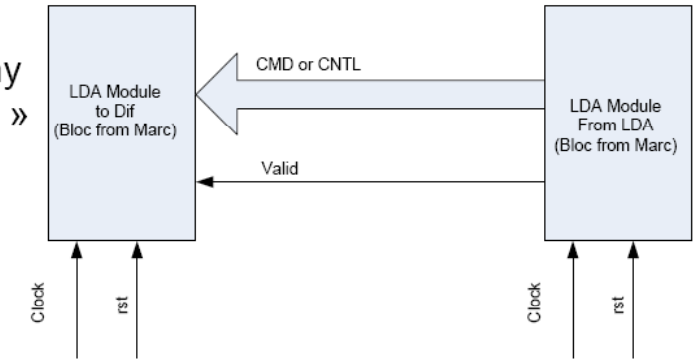


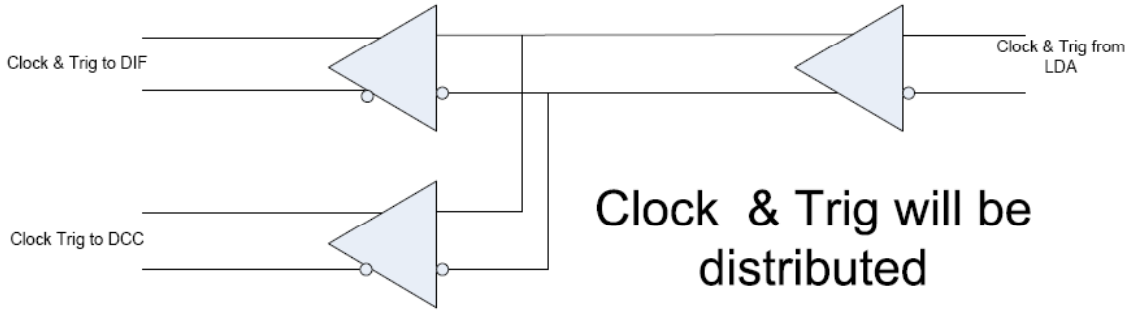
Overview of DCC blocs (Data side)



Overview of DCC blocs (CMD, CLK, Trig)

There will be as many « LDA Module to DIF » than DIF



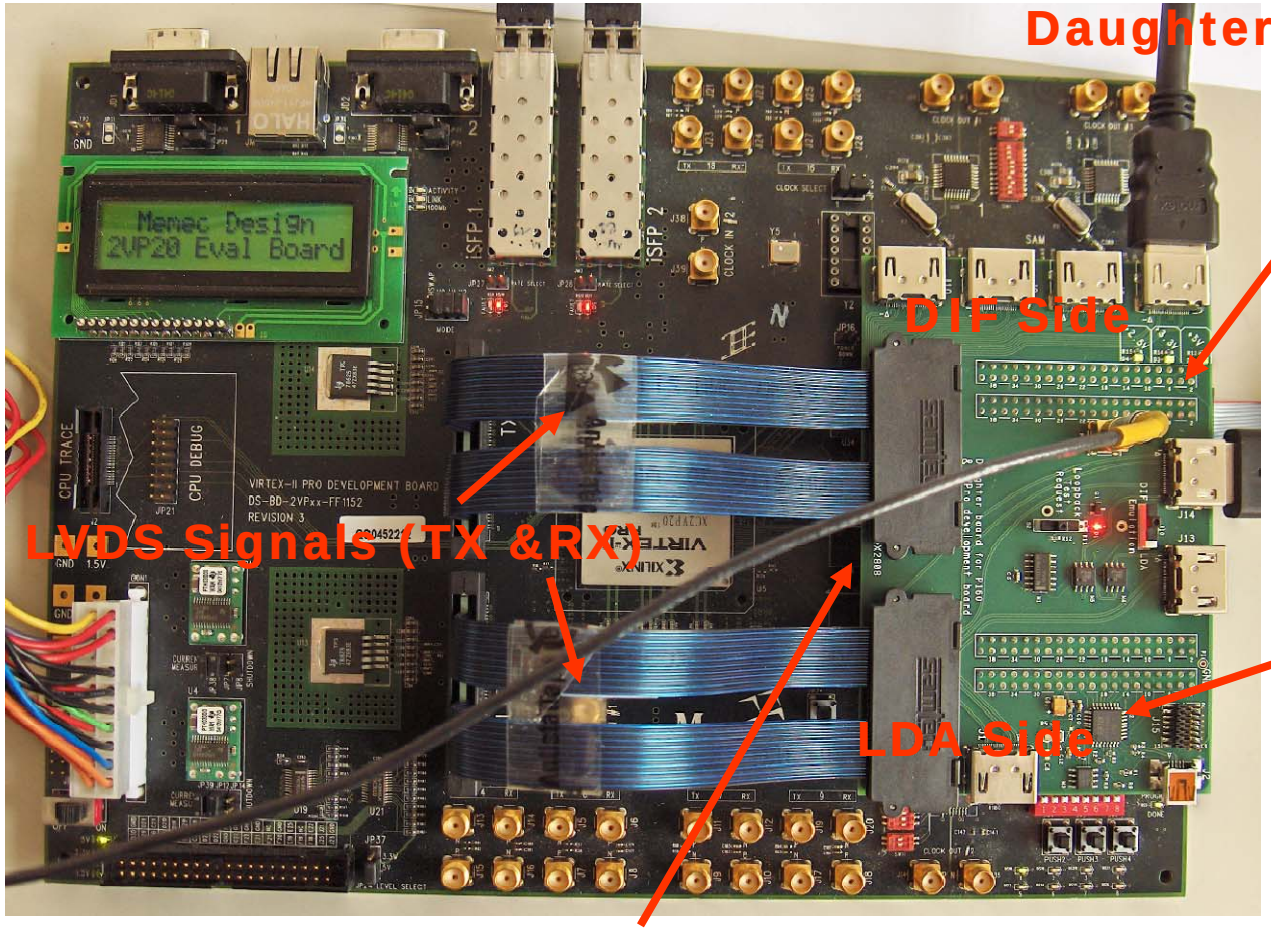


Clock & Trig will be distributed

Status

- Prototype 0 before the DCC board
  - Read 4 DIFs
  - Implementation and tests of the VHDL code
  - Designed from a XILINX evaluation board with a 128 Mbits SRAM and daughter board to the HDMI, USB connection
- Where are we ?
  - The daughter board is fabricated
  - We work on each VHDL code blocs (Memory controller, buffer, and others…..)
  - We re-use all LDA modules (Marc) and USB module (Clement)

Picture on XILINX evb and daughter board



Planning (estimation)

- Until end of 2008
  - Start of DCC schematic and first layout
  - Define the optimum memory component
  - FPGA will be a Spartan-3
- January – April 2009
  - Fabrication of DCC prototype
  - Setting up tests bench
  - Tests and validation of VHDL code
- June – July 2009
  - If all work, start of production

  Remark: the time of production will depend on availability of some components