<u>IN2P3</u>







SKIROC2 issues

Orsay Micro Electronics Group Associated



- SKIROC 1 performances and limits
- SPIROC in SKIROC mode
- Expectations for EUDET
- SKIROC 2 proposal
- Bonus : ROC chips in test beam



SKIROC 1 design limits

- Most critical issue : Too much dynamic range in the charge preamplifier
 - Max input signal : 2000 MIP
 - Noise floor : 0.15 MIP
- Preamplifier gain too small
- Huge gain in the trigger path to be able to trig on 1/2 MIP SKIROC linearity results



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SPIROC used in **SKIROC** mode



SKIROC2 issues, CALICE meeting, 9/9/08 - Omega



- Dynamic range : -500 MIP/cell → same as physics prototype
- Number of channels :
 - 36 instead of 64

Expectations for EUDET



- 64 channels to read out new 256 pads wafers with 4 chips
 - This is a critical PCB requirement
 - This will make SKIROC2 the biggest chip of the ROC family
 - 50-60 mm²
- Capability to operate in ILC mode and in test beam
 - This is a physics requirement to take data with EUDET module
 - Calculation of data rates to be validated
- High dynamic range from 0.1 to 2500 MIP
- (Eventually) time measurement to tag events in test beam (not useful in ILC mode)

SKIROC 2 block scheme proposal



Schedule

- Skiroc 2 expected to be sent in fab in March'09
 - Sharing of the HARDROC2 and SPIROC2 production
 - If SKIROC 2 is validated → production in hand for EUDET module
 - Cheaper than an engineering run for prototyping due to big silicon area (60mm² ie ~60k€)
- Next PCB prototype will use SPIROC2 with Hamamatsu wafers
 - Validation of all electronics and assembling process
 - missing : dynamic range (500MIP/2500MIP), granularity
 - PCB in hand before the end of the year?

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Test beam and ILC timescale trade off

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ILC beam structure





Acquisition : Trigger in ILC mode



Acquisition : Trigger in test beam mode Omega

