Electronics Integration - Status

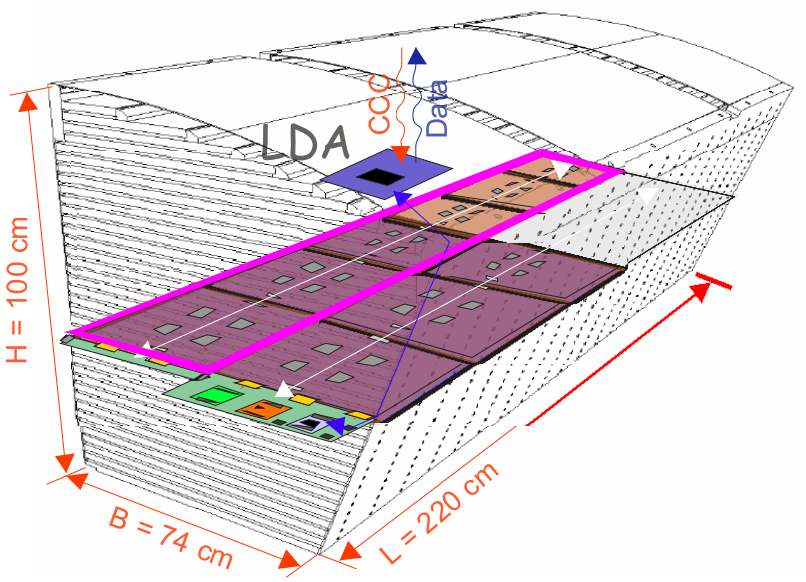
Mathias Reinecke

for the AHCAL developers

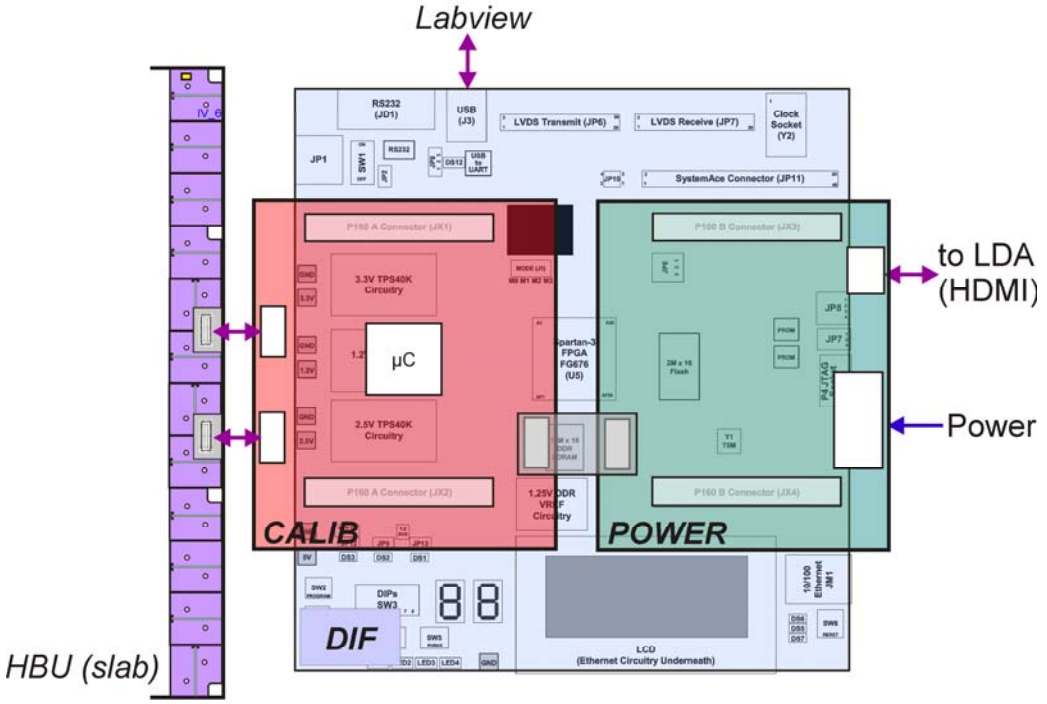
Next prototype: Architecture

FE

the future …



1st EUDET Prototype (**1st step**)



Commercial DIF, new mezzan.
(CALIB, POWER), 1HBU (later: 6)

Prototype Tiles

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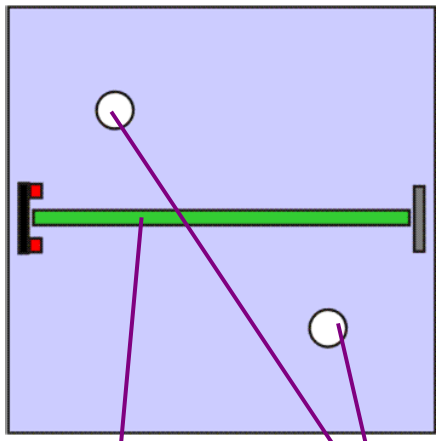
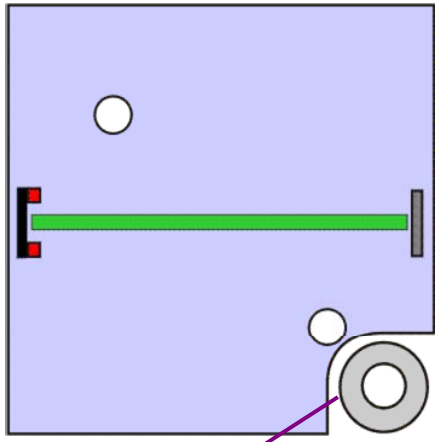
Prototype Tile for HBU0

dimensions in (mm;mm)



Mechanics Tile for HBU0



100-150 prototype tiles (structures machined, not moulded):
Problems with SiPM assembly, impact on time schedule for HBU0!!

Tiles for EUDET module

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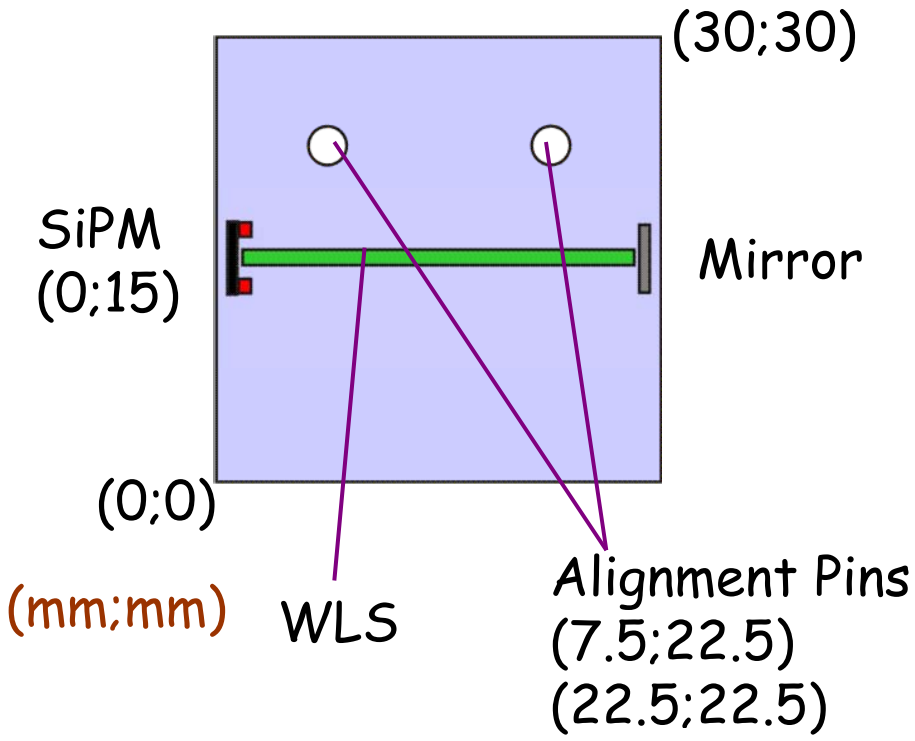
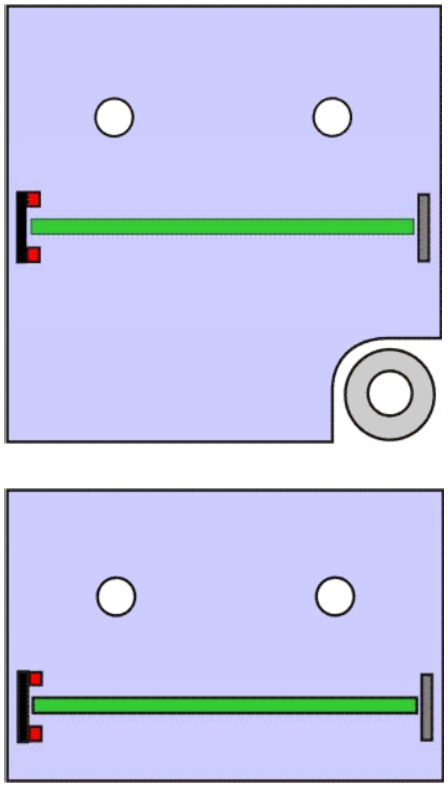
Standard Tile (moulded)





Shorted (by 1cm) tile for inter-layer sizes

No time schedule up to now.

HCAL Base Unit (HBU0)

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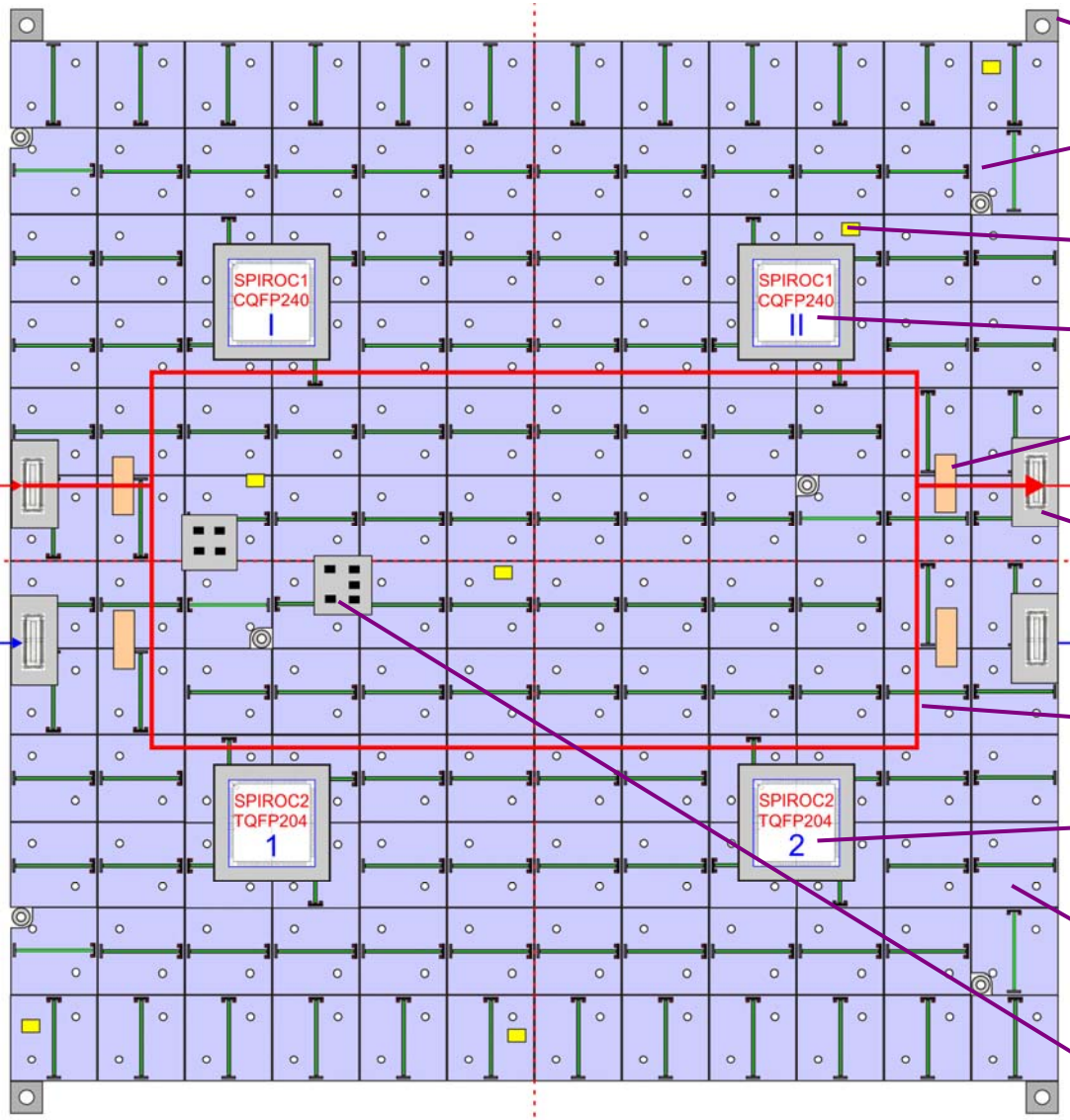


Signal IN

Power IN

Cassette fixation

Mechanics Tile

Temp. Sensor

SPIROC1

Debug Conn.

Flexlead Conn.

Two signal paths

SPIROC2

Prototype Tile

Calibration Electr.
(LED + Charge Inj)

HBU0 Status

FE

-Integration concept fixed
-Schematic (Mentor Graphics CAD) finished
-Layout is waiting for tile geometry information
-Critical parts (connectors) ordered.

-Layout is complex (1-2months), PCB manufacturing and assembly: 1-2months => realization in 2008 already critical!

Design progress is interrupted due to missing tile information.
Shall we proceed without tile information?
=> Large gaps between tiles, large holes (1mm) in PCB for SiPM pins. Not a real integration test …

HBU Interconnection (Flexleads)

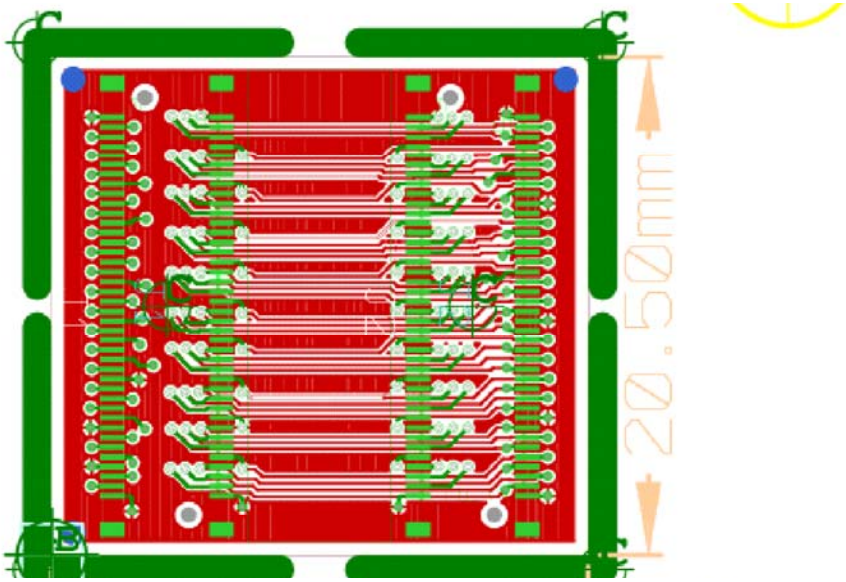
FE

-Two types of Flexleads (for Signals, Power) have been designed (CAD)

-Flexleads allow +/-100µm displacement of connecting modules

-Magnet-field tests up to a few Tesla done: no problems seen.

-Flexleads can be ordered now!



Flexlead CAD Layout

DIF Status

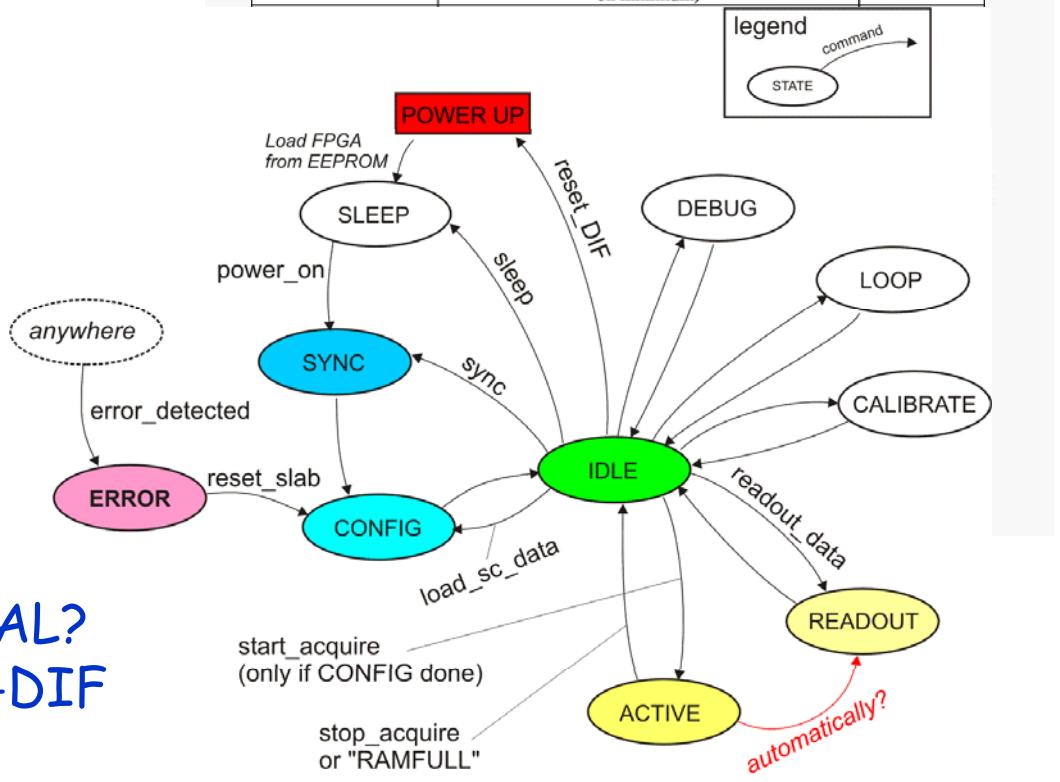
FE

-Based on commercial FPGA (Spartan3-1500) board

-Command list and DIF state diagram in preparation

-VHDL code generation soon (prototype firmware for USB access in 2008)

Command	Function and Parameters	Change DIF State?
power_on	turn slab power on / off (maybe partly?)	no
reset_DIF	reset of DIF electronics (not: slab)	yes
reset_slab	reset of slab (ASICs). Not: DIF	yes
reset_BCID	synchronize data taking by resetting bunch counter	no
sleep	puts DIF and slab into SLEEP state (powered down)	yes
sync	synchronization LDA all DIFs	yes
idle	puts DIF into idle state (DIF power on, slab power on minimum)	yes



DIF state diagram

Firmware status of ECAL/DHCAL?
Reference documents for LDA-DIF interface (also: DAQ group)?
Firmware development needs closer coordination.

CALIB Status

FE

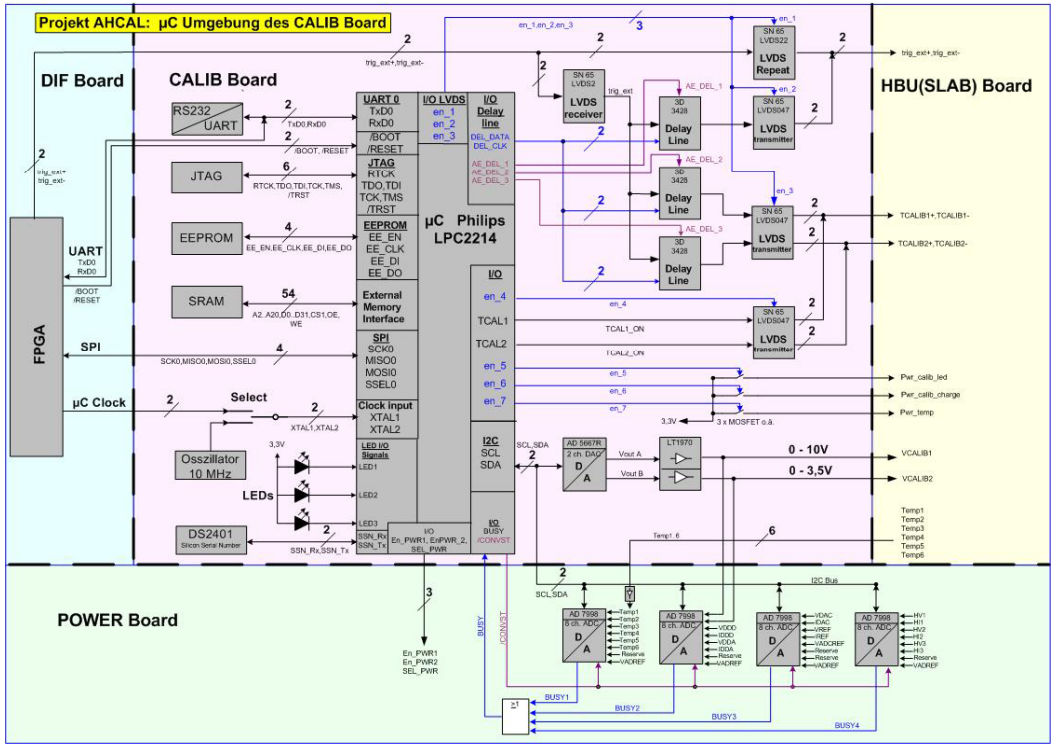
„AHCAL Calibration System“
(UV-LED and Charge Injection)

-Concept fixed, schematic finished

-µController software dev. ongoing (good progress)

-Layout (CAD) starts now, expected to be finished: End of September.

-Module should be available: November/December 08



By
M. Zeribi

POWER Status

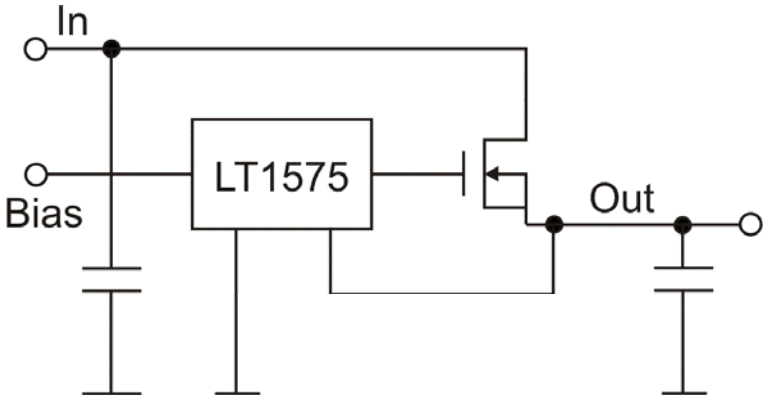
FE

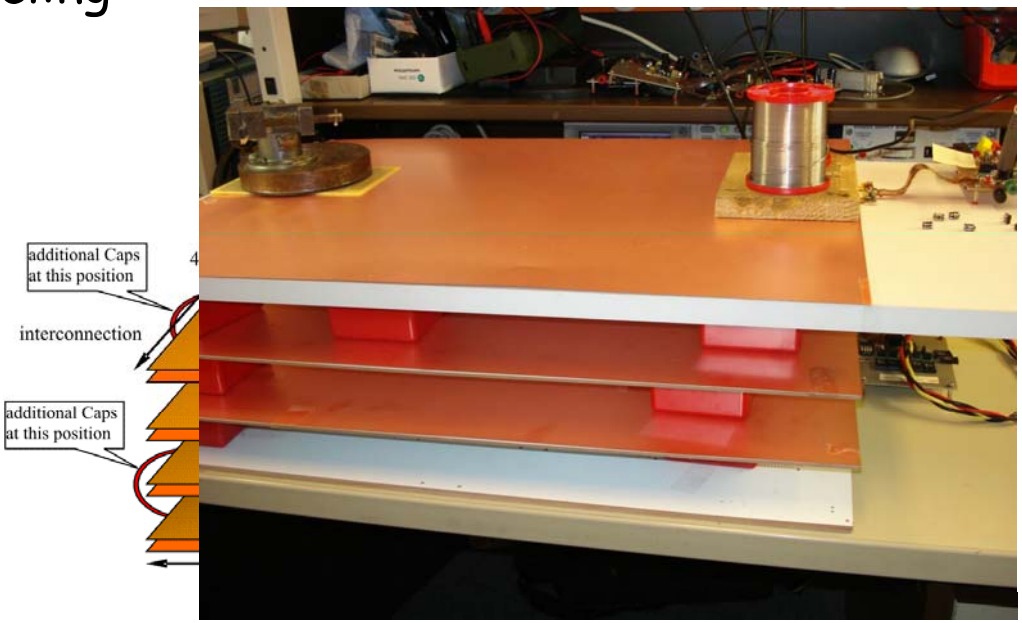
„AHCAL Slab Power Regulators"

-Regulator setup fixed, schematic finished

-Suitable for ILC-like power cycling

-Layout and Production probably in 2009 (module can be replaced initially by bench-top power supplies)

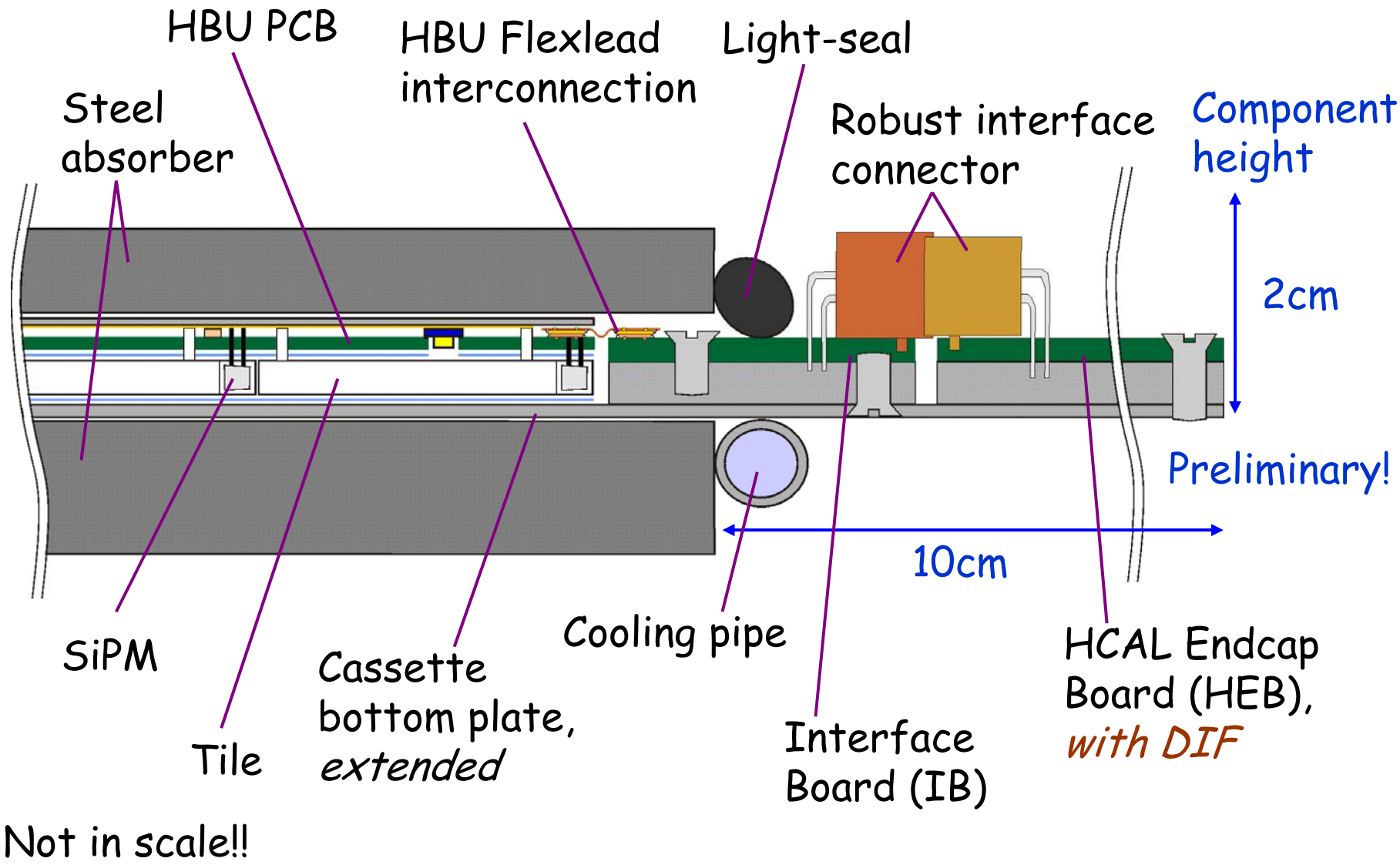




By
H. Wentzlaff

AHCAL Slab Interface (Mech.)

FE



Mechanics Status

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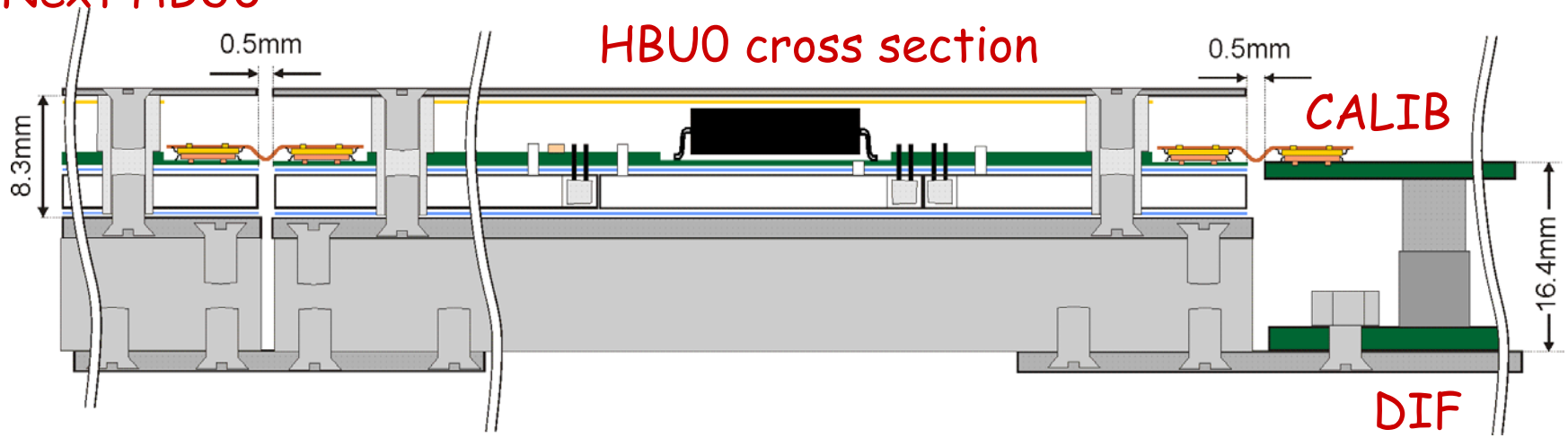
Next HBU0



- Mechanical proposal (cassette, interface to DIF) has been set up for the AHCAL prototype (HBU0, DIF as commercial board).

-The necessary mechanical parts are currently designed within CAD tool => production within 2008

Conclusions

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-AHCAL technical prototype (TP) does not cover a full slab, but ~150 channels (2 HBU0s, tile-prototypes).

-Eudet module (detector layer) requires HBU redesign. A full slab (and detector layer) is expected for summer/autumn 2009.

-timeline for TP is defined by HBU0 (tile geometry missing).

-development of the modules CALIB and DIF (firmware) in 2008 possible. But for HBU0 we need the tile information to proceed.