Si-W ECAL
Silicon wafers status

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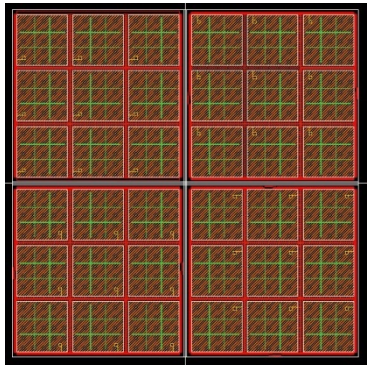
LLR

Si overview

- Cz and Rus used on the prototype (low cost, standard design)
  - Ok : Depletion, current leakage, signal
  - 500 nm, 6x6 cm², 26 pads : change to 300 nm, 9x9 cm², 256 pads
  - Square events : understood to come from guard rings
- Search for new design techniques
  - Segmented guard rings to avoid square events
  - Dead space (at the border) reduction
- Hamamatsu : new (secret) design
  - New size (324 pads)
  - Sold as having no guard rings (thus no square events)
  - Have guard rings ! External charge injection shows square events…
  - Large dead space
  - Test bench issue

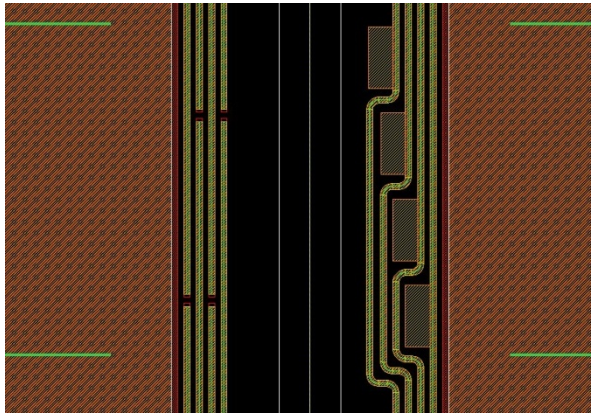
Segmented guard rings

- Should avoid the signal propagation along the border of the wafer



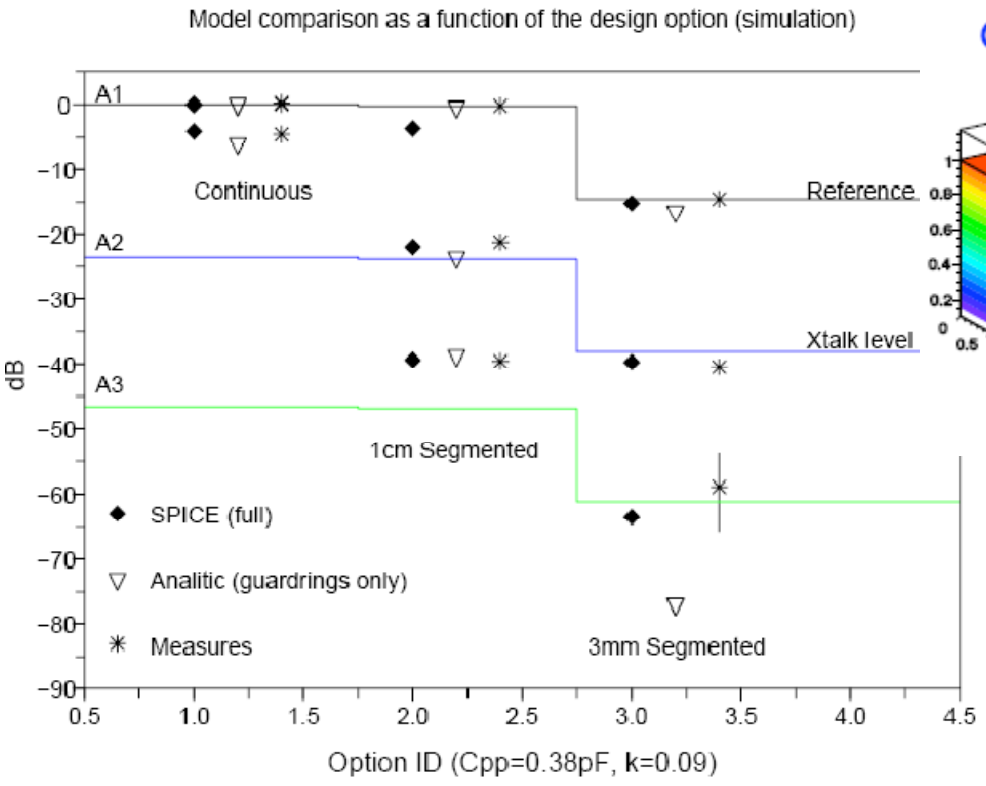
- Idea tested thanks to PCBs and test bench at LPC (CALOR'08 talk)
  - Segmented topology helps to prevent SqEvt (factor 50 on signal intensity)

- Prototype wafers are being manufactured (LLR made layout)
  - OnSemi/Institute of Physics (Prague), Cz
  - BhaBha Atomic Research Centre, India

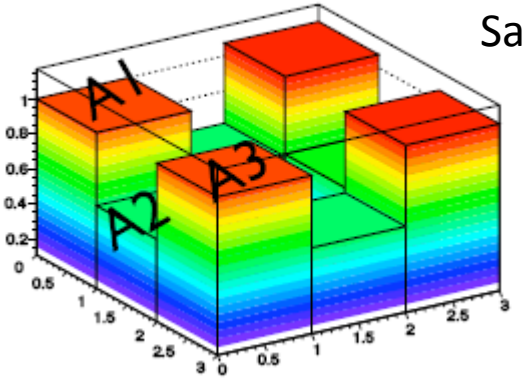


- Will be measured at LPC

Measurements of printed circuit models



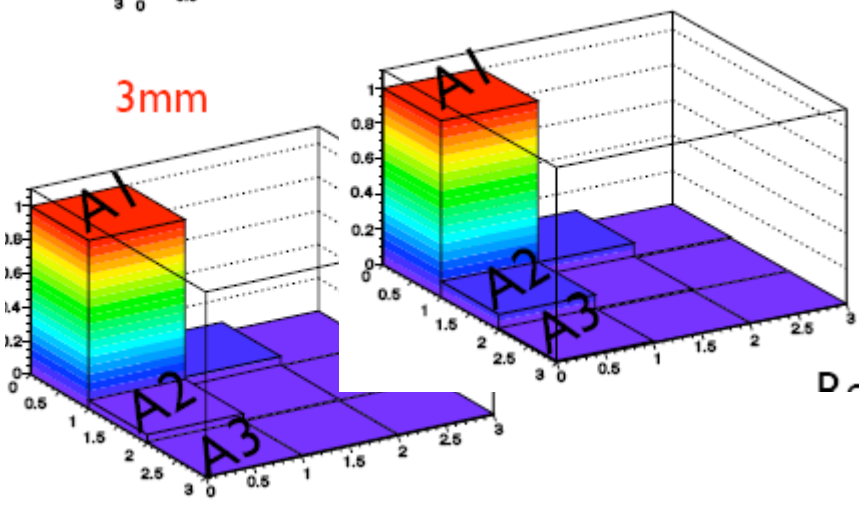
Continuous

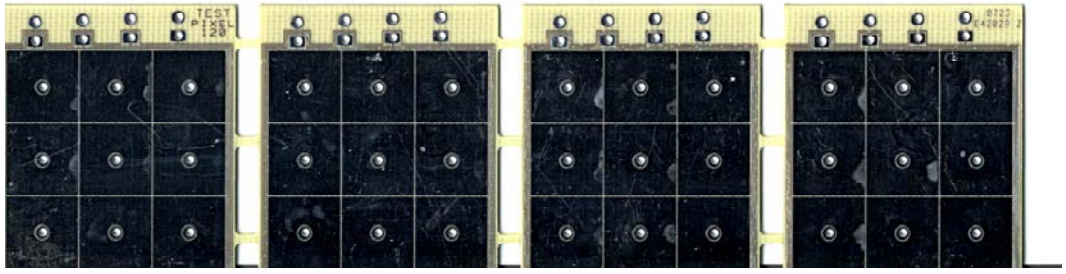


Same as in TB data

1cm

3mm

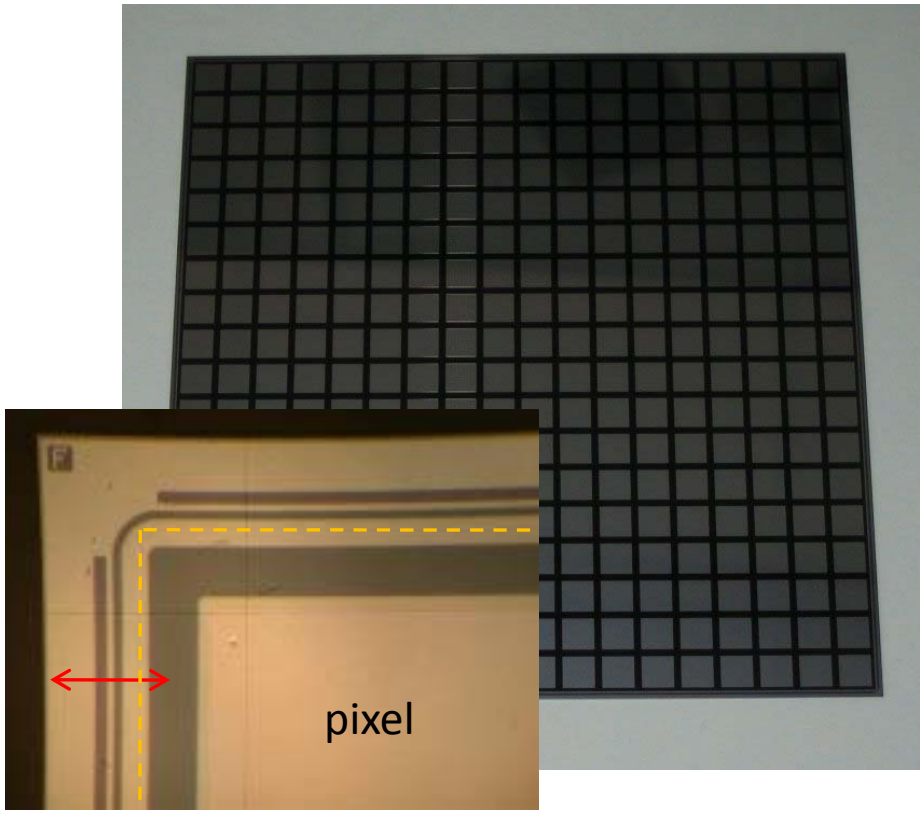




Hamamatsu wafers

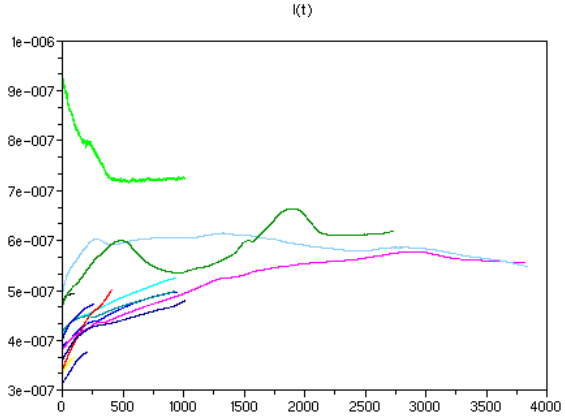
- Alternate design without (?) guard rings
- First samples with the new geometry
  - Gluing tests
  - Slab integration tests

- BUT
  - Dead Space : ~1.1 mm
  - unexpected metallization similar to a Guard ring

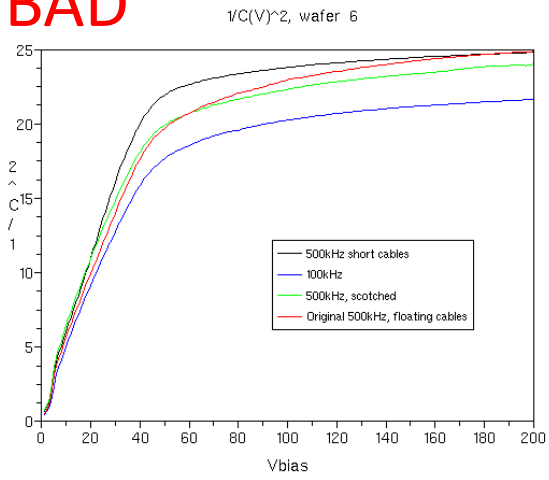


Tests of Hamamatsu wafers : status

- Leakage, I(V) curves : OK, breakdown > 500V
- Time, I(t) curves : OK (few samples tested)

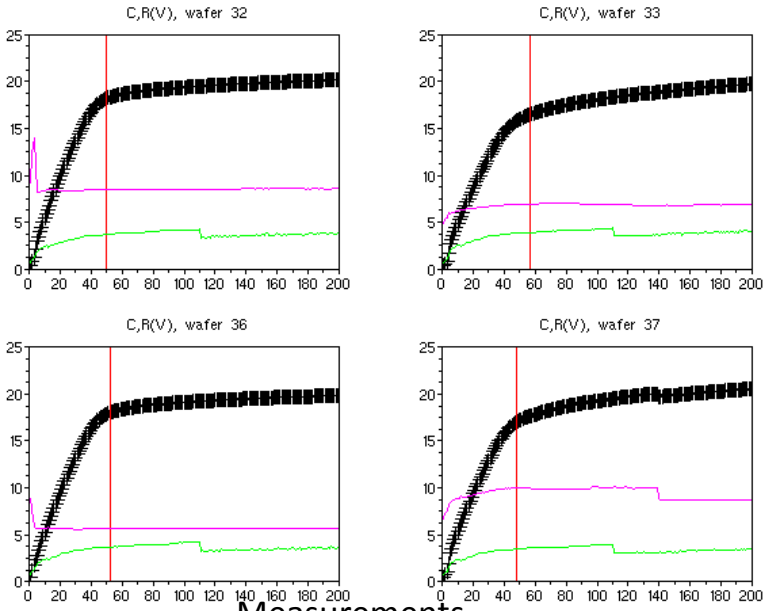


- Depletion, $1/C^2(V)$ curves : 50% BAD
  - Non reproducibility of the measurements
  - Time dependency
  - Need a new setup

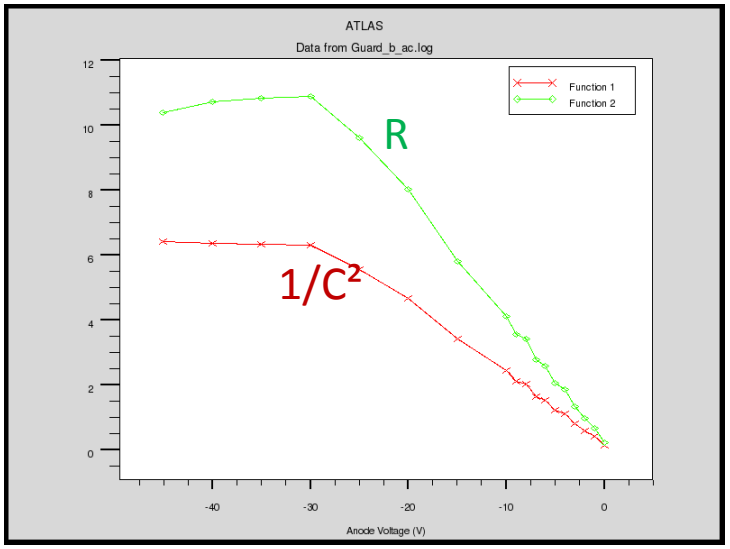


C(V) or $1/C^2(V)$ must be flat for bias voltage higher than the depletion voltage. If not, noise is generated from the capacitance modulation :
dQ = CdV + VdC = 300-3000 MIPs (measured values)

Tests of Hamamatsu wafers : comparison to simulation (serial R, C model)



Measurements



Simulation

Inflexion point around 40 V : OK

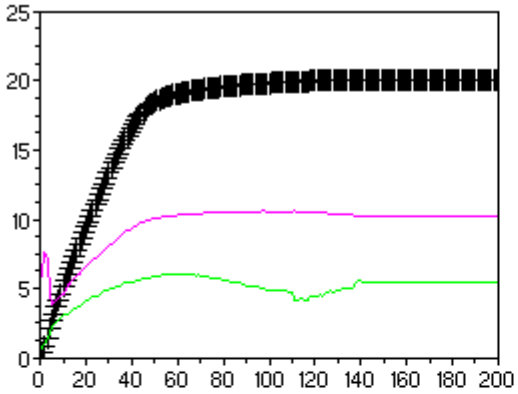
Behavior is not uniform according to the wafer ID

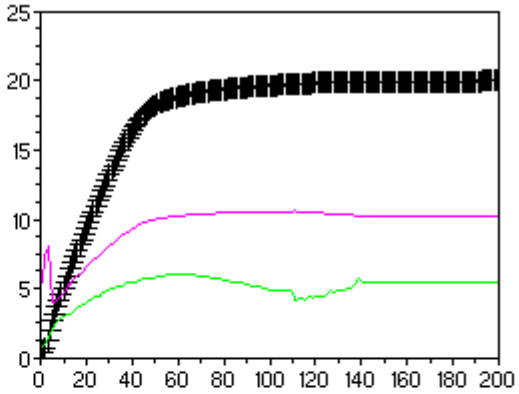
According to simulation R and $1/C^2$ should have the same shape : not the case

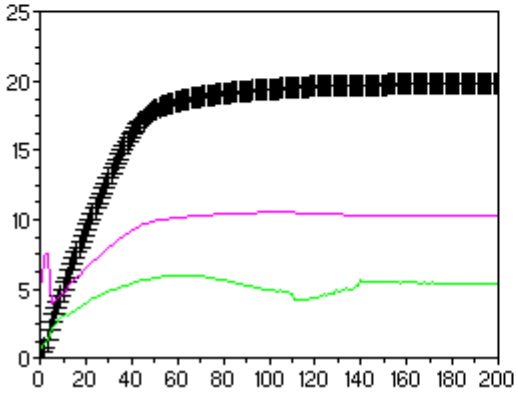
We may not measure the true R and C

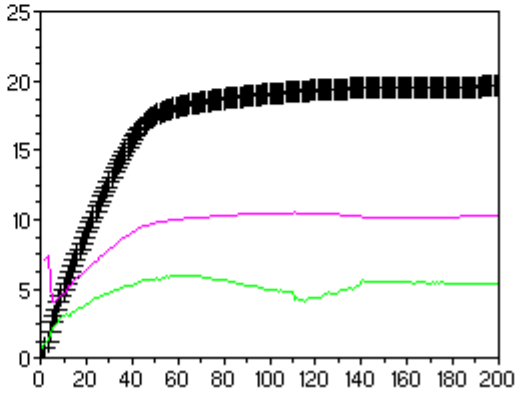
New test setup : short cables, ground loop suppressed, ceramic (instead of electrolytic) decoupling capacitance,…

Tests of Hamamatsu wafers : new test setup









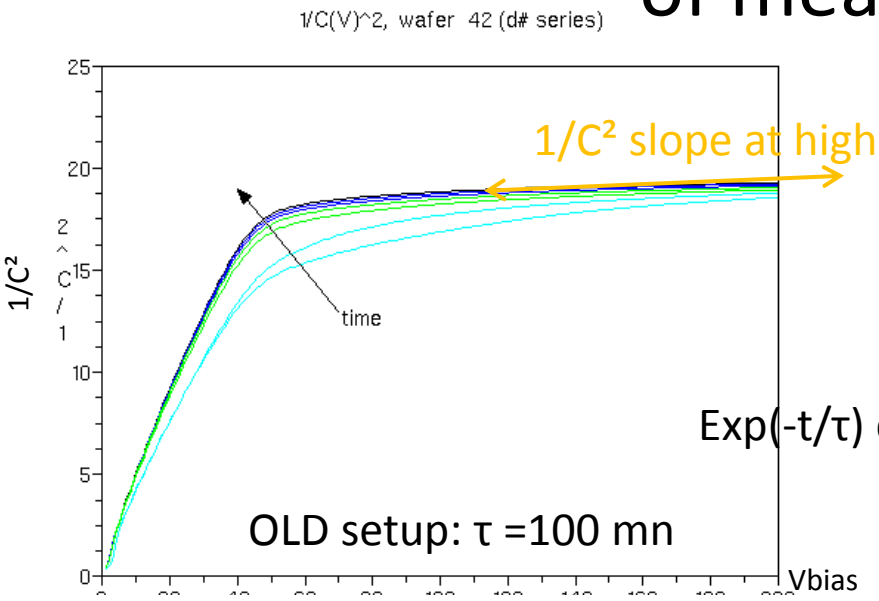
Uniform behavior

R and $1/C^2$ have the same shape : confidence in measurements is increased

$1/C^2$ flatness : better

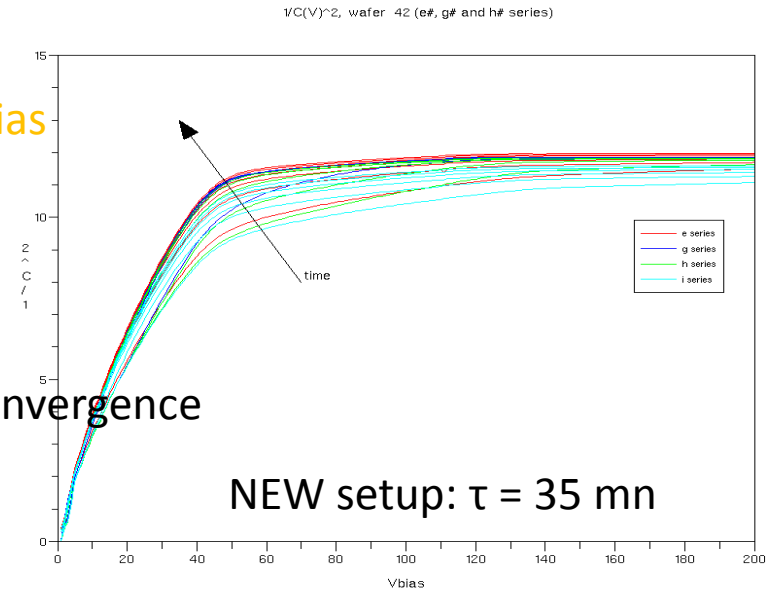
Yield ~ 100 % (instead of 50%)

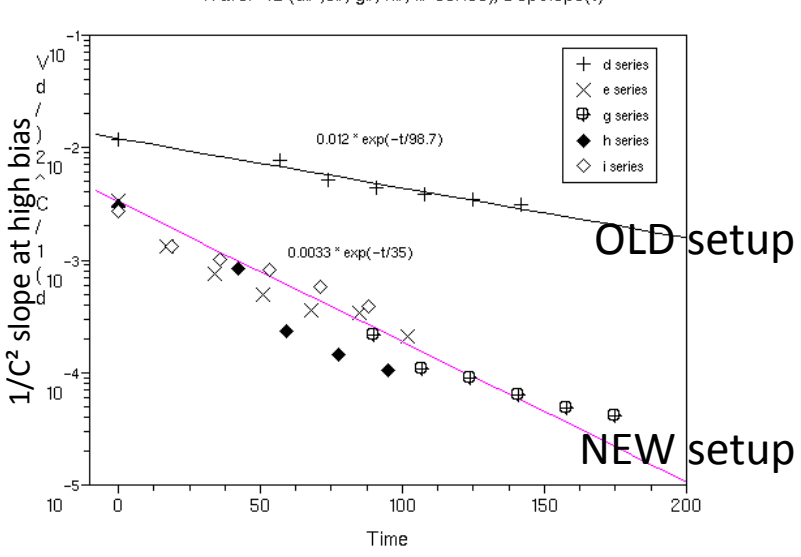
Tests of Hamamatsu wafers : time dependency of measurements



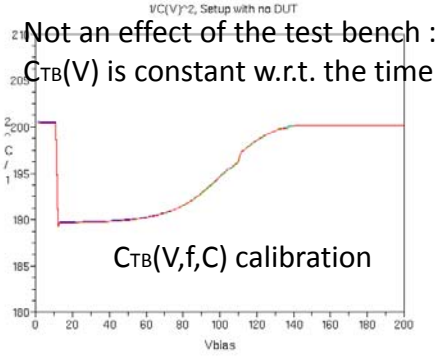
1/C² slope at high bias

Exp(-t/τ) convergence





Effect not seen with Czech wafers



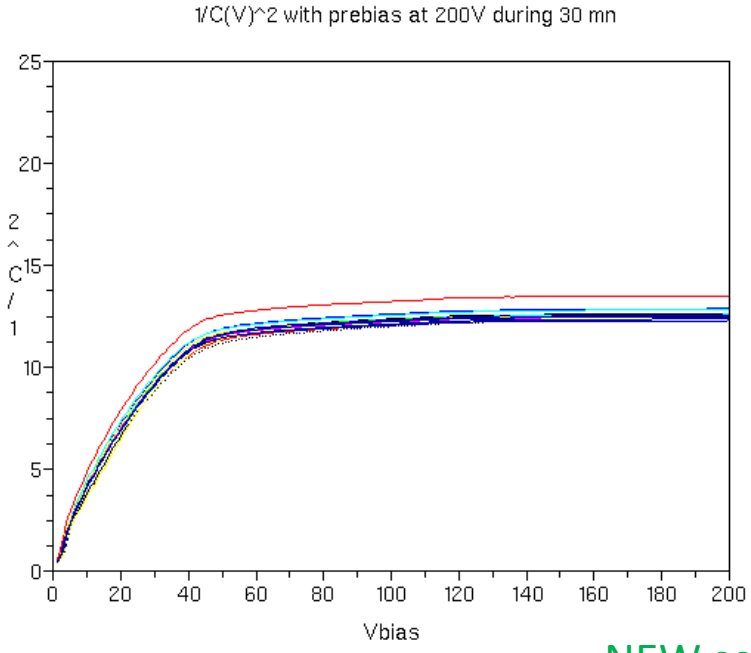
Not an effect of the test bench : $C_{TB}(V)$ is constant w.r.t. the time

With the new setup :

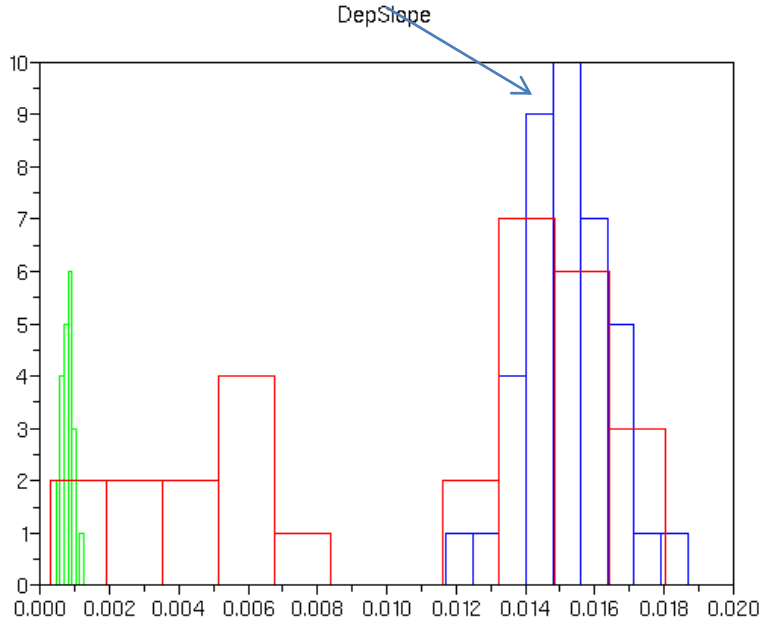
- Measured slope improved by a factor 10 to 80
- Time constant decreased by a factor 3
- "Recovery" τr > 1 day

Tests of Hamamatsu wafers : new procedure

- Wafers are biased at 200 V during 30 mn before measurements



OLD setup, Czech wafers (2007 meas.)

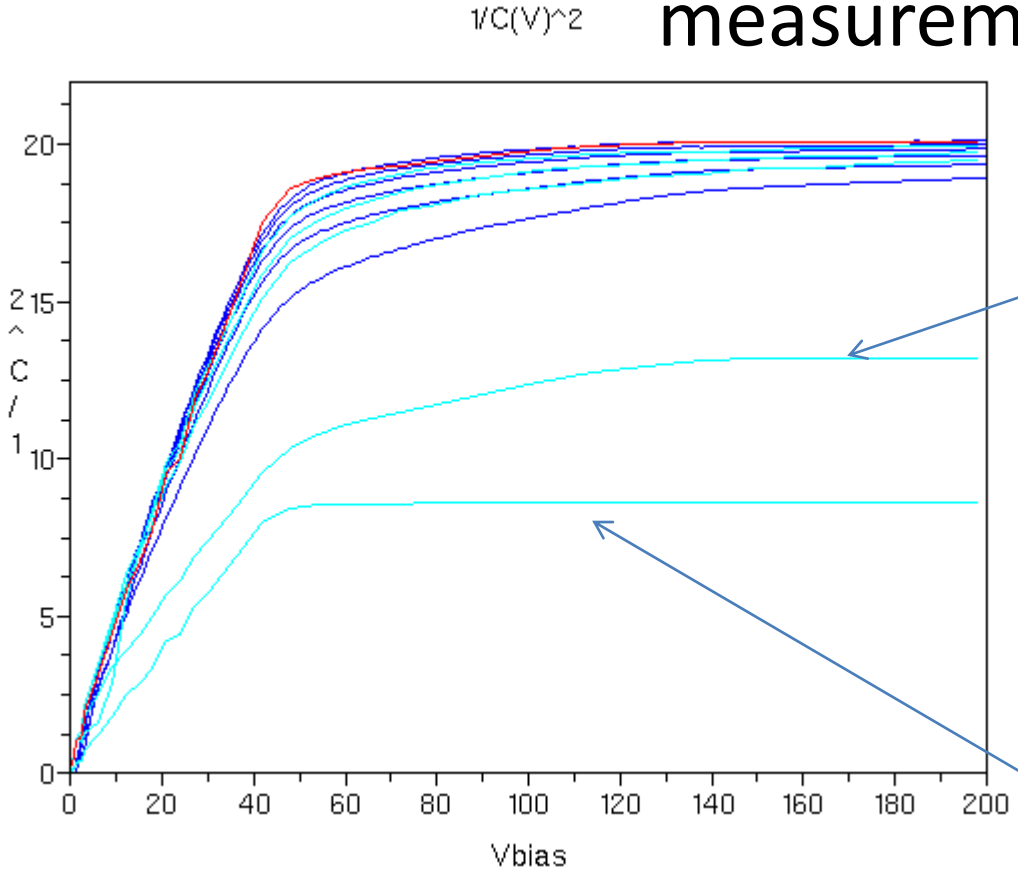


NEW setup, Hamamatsu
+ NEW procedure

OLD setup, Hamamatsu

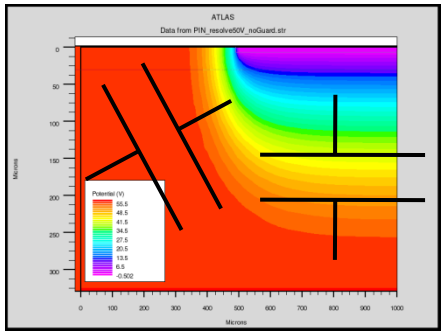
Measurements are reproducible
Measured flatness gain a factor 10 ($1/C^2$) and 80 (C)

Hamamatsu wafers : simulation vs measurements



17.5*4 x

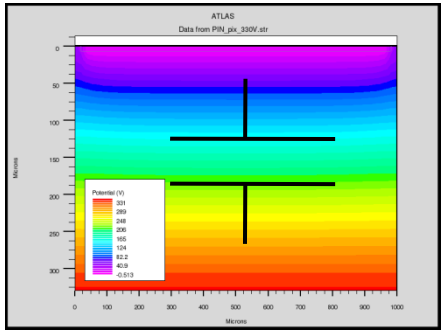
Side cap



+

17.5² x

Pixel cap



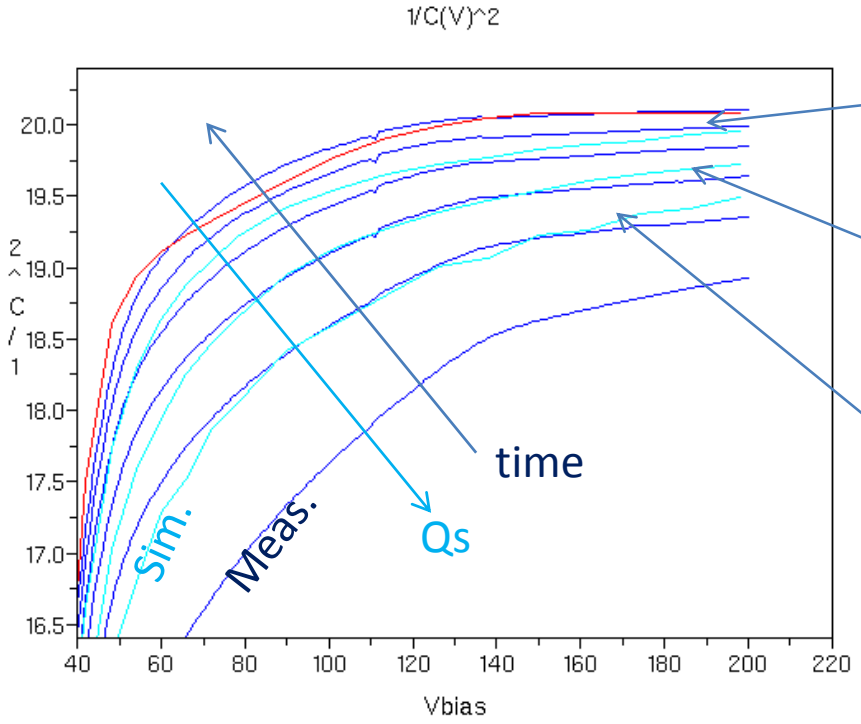
=

Red curve (scaled)

The Shape of the measurements is explained by the addition of two contributions to the overall capacitance of the wafer.
2 inflexion points : 40 V and 130 V in simulation AND measurements.
Full (side+pixel) depletion reached for Vbias>150 V and almost full depletion at 40 V but with a higher C(V) slope (noise).

Hamamatsu wafers : simulation

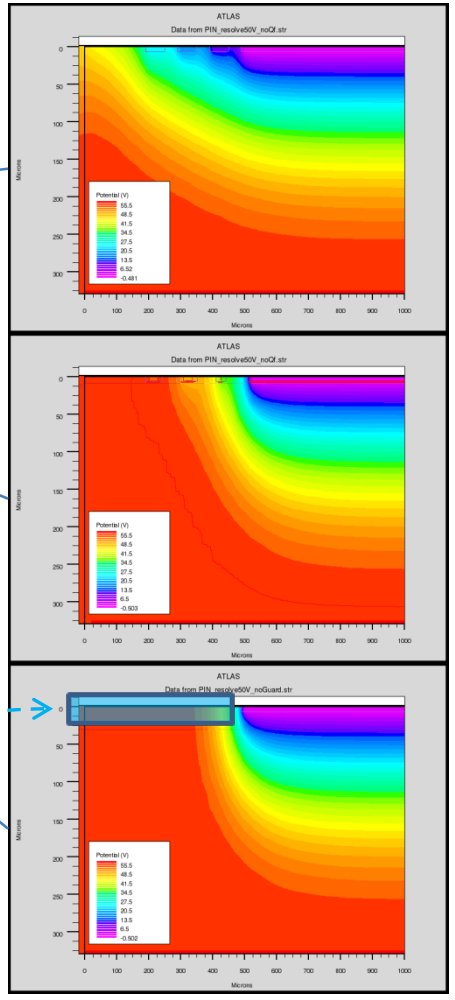
C(V,t) ⇔ C(V,Q) and Q(t) ?



Qs = - Qref

Qs = 0

Qs = + Qref



The variation of a surface charge density Qs lead to a similar behavior as for the time evolving measurements : the effective C(V) could depend on Qs.

Typically, interstitial defects create trap states filled according to the time (diffusion process : exp law). Trapped charge then compensate a initial charge due to the deposition process of the materials.

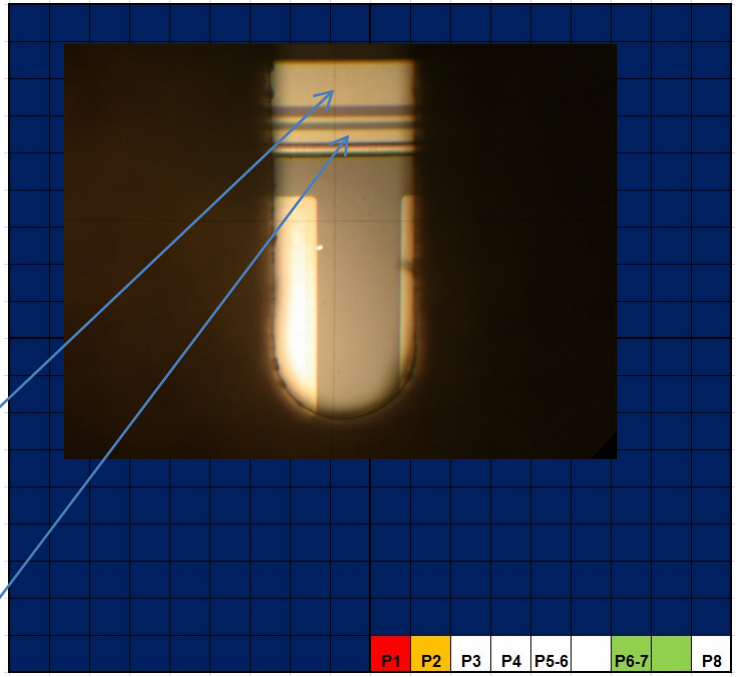
Qs=Qi+Qt(1-e(-t/tau))

Hamamatsu wafers : crosstalk measurements

Charge is injected on the metal rings: a similar behavior as for square events is measured. Compared to PCB models with continuous guard rings :

- Factor 4 less for the outer guard ring
- Factor 50 less for the inner guard ring

Square events are expected !



Pixel ID	Amplitude (mV)
P1	1030
P2	1060
P6-7	2080

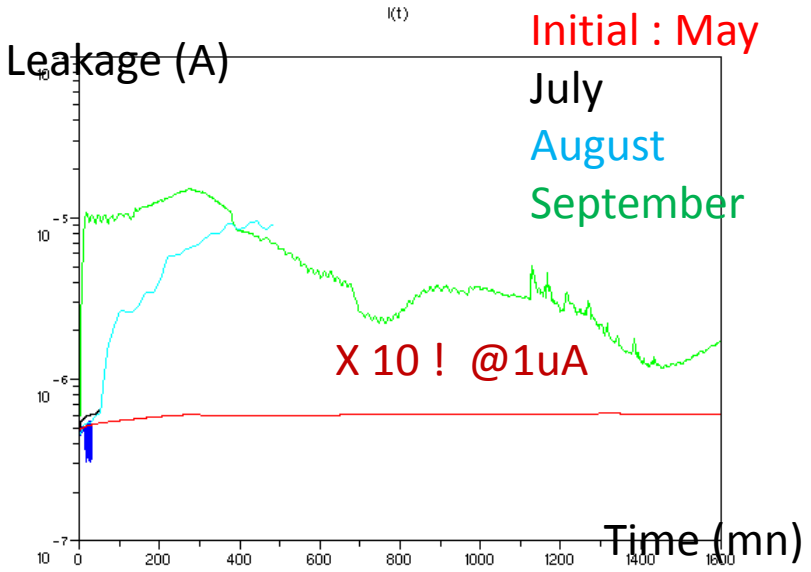
Pixel ID	Amplitude (mV)
P1	80
P2	63
P6-7	111

But signal (charge) is injected at the surface. What if charge is generated in the volume below the rings ?

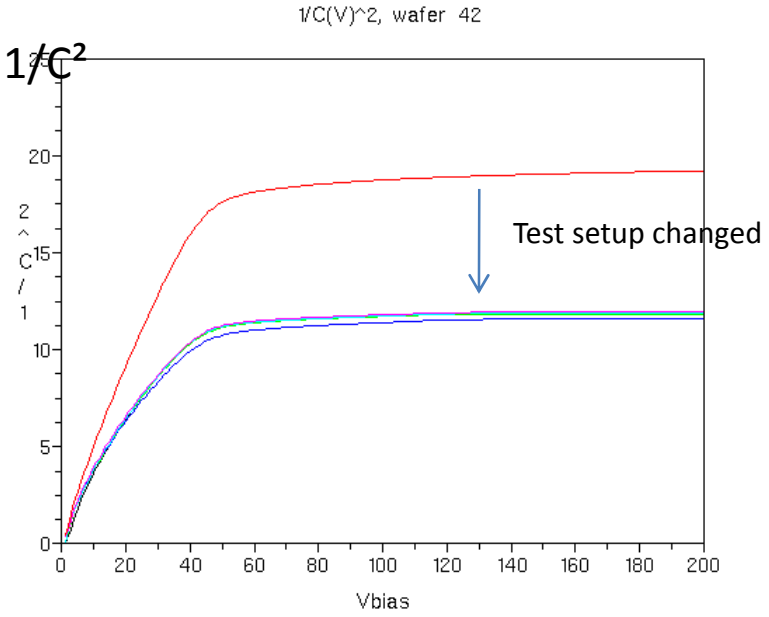
It needs further investigations with particles or laser beam

Hamamatsu wafers : glue and time

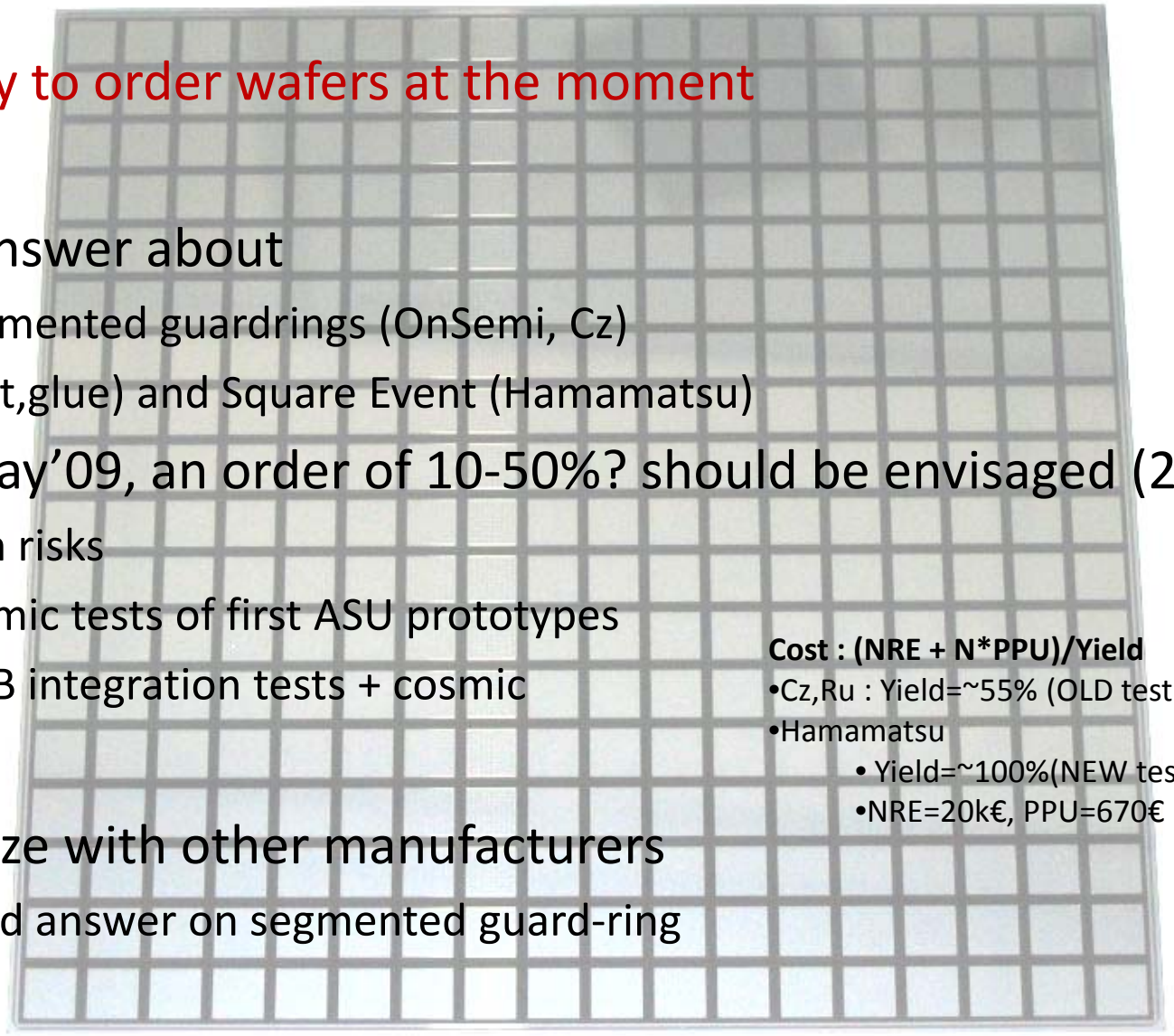
- One wafer was glued on July then regularly measured
  - Leakage in increased by a factor 10
  - Stable C(V)
- No clear correlation seen with temperature and humidity



- Still a lot a work to do about variations in time
  - Dedicated PCBs are being designed @LLR then few wafers will be glued at Manchester
  - behavior checks at long term (few months)



ECAL Silicon wafers : EUDET



- No way to order wafers at the moment

- If no answer about
  - segmented guardrings (OnSemi, Cz)
  - or I(t,glue) and Square Event (Hamamatsu)

before May'09, an order of 10-50%? should be envisaged (256 pixels)

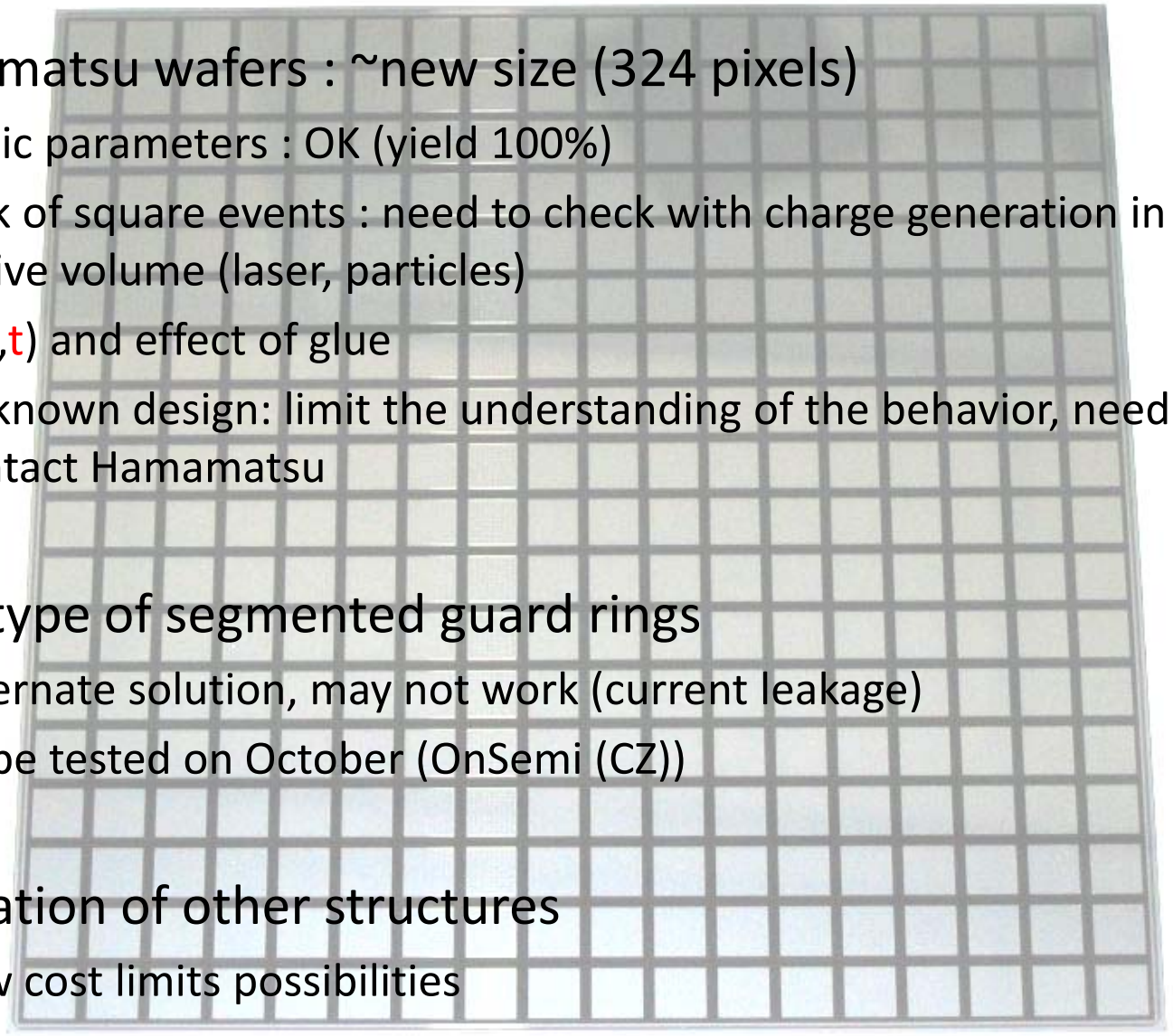
  - with risks
  - Cosmic tests of first ASU prototypes
  - SLAB integration tests + cosmic

Cost : (NRE + N*PPU)/Yield

- Cz,Ru : Yield=~55% (OLD test bench)
- Hamamatsu
  - Yield=~100%(NEW test bench)
  - NRE=20k€, PPU=670€ : 40k€/30 wafers

- New size with other manufacturers
  - Need answer on segmented guard-ring

ECAL Silicon wafers : Conclusion



- Hamamatsu wafers : ~new size (324 pixels)
  - Basic parameters : OK (yield 100%)
  - Risk of square events : need to check with charge generation in the active volume (laser, particles)
  - C(V,t) and effect of glue
  - Unknown design: limit the understanding of the behavior, need to contact Hamamatsu
- Prototype of segmented guard rings
  - Alternate solution, may not work (current leakage)
  - To be tested on October (OnSemi (CZ))
- Simulation of other structures
  - Low cost limits possibilities