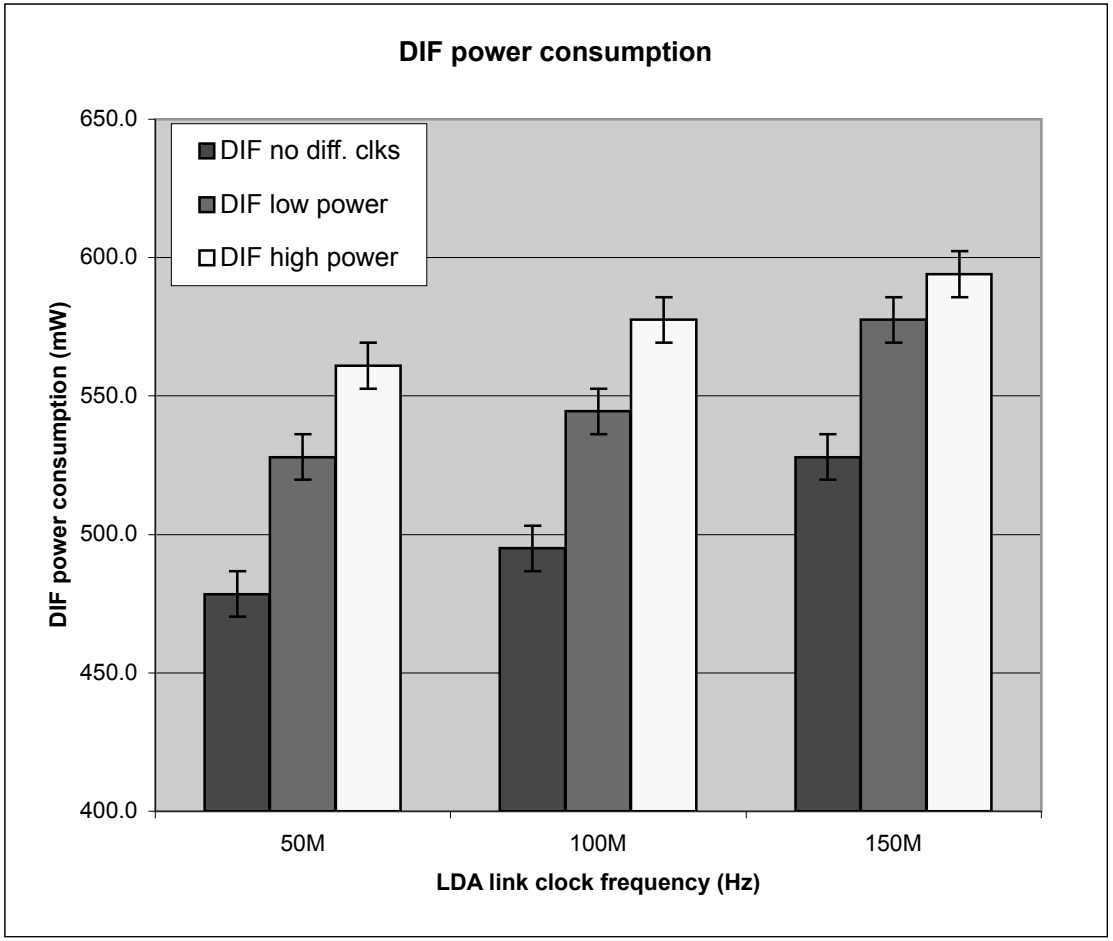

LDA link clock frequency	50M	100M	150M
DIF low power	528.0	544.5	577.5
DIF high power	561.0	577.5	594.0
DIF no diff. clks	478.5	495.0	528.0

two LVDS pairs low power:	49.5	49.5	49.5	
single LVDS pair low power	24.75	24.75	24.75	
four LVDS pairs low-high power	33.0	33.0	16.5	
single LVDS pair low-high power	8.25	8.25	4.125	
single LVDS pair high power:	33	33	28.875	
total DIF:				
4xCLK + 2xCTRL hi power	198	198	173.25	mW
in addition to 'no diff clks DIF'	676.5	693.0	701.2	

plus additional logic

POWER REGULATOR HARDWARE FOR SLAB IS NOT INCLUDED