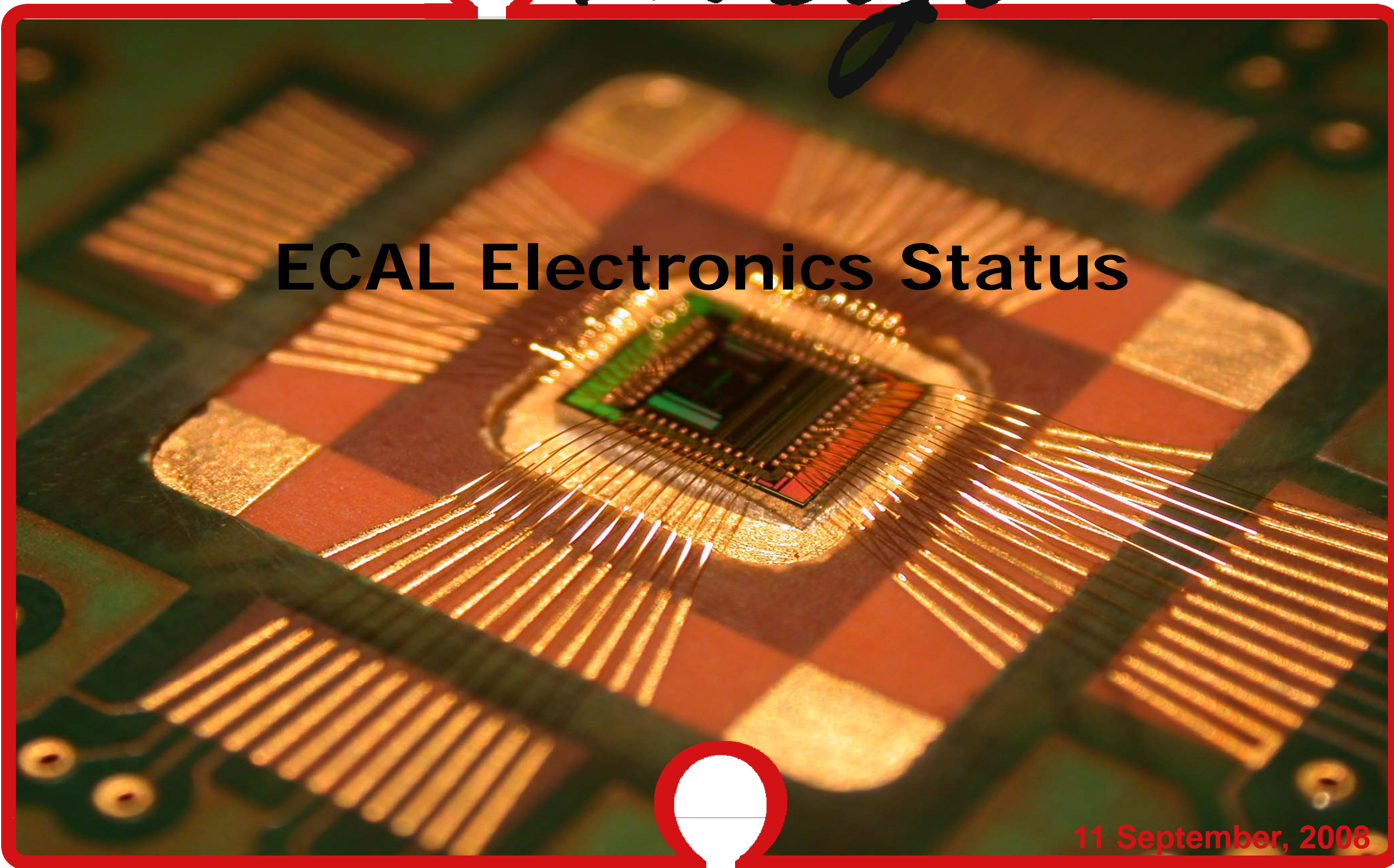
IN2P3

CSNSM LAL LUR IPN Orsay

Omega



ECAL Electronics Status

11 September, 2008

Orsay MicroElectronics Group Associated

ASIC design
SKIROC 2

SKIROC1 One channel block scheme

Slow shaper
Gain 10
T_p=180ns

Analog Memory
Depth = 5

Gain selection

12-bit ADC
(Wilkinson)

Charge Meas.

Slow shaper
Gain 1
T_p=180ns

Analog Memory
Depth = 5

20MΩ
1MΩ
0 →6pF

Input

Preamp.

3pF

Calib. Input

fast shaper
Gain 100
T_p=100ns

Amplifier
Gain 5

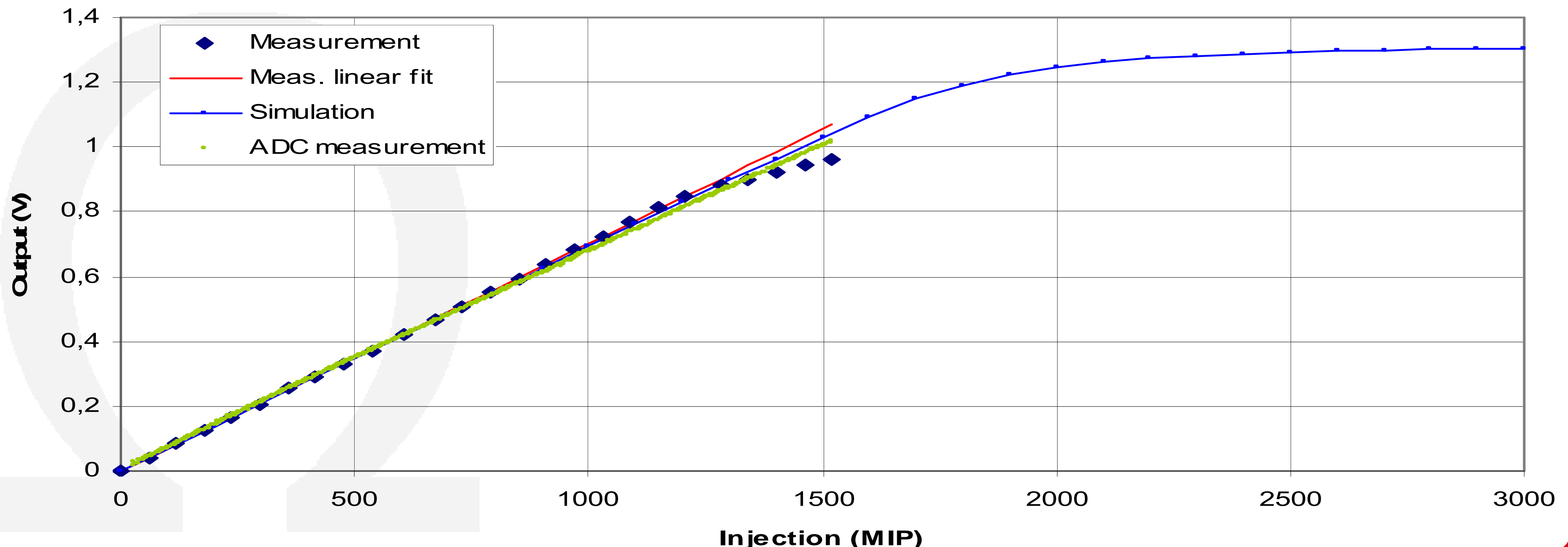
3-bit DAC adjustment

Trigger out

10-bit dual DAC – common to 36 channels

SKIROC 1 design limits

- Most critical issue : Too much dynamic range in the charge preamplifier
  - Max input signal : 2000 MIP
  - Noise floor : 0.15 MIP
- Preamplifier gain too small
- Huge gain in the trigger path to be able to trig on ½ MIP



SPIROC used in SKIROC mode

SPIROC limits in ECAL

- Dynamic range :
  - 500 MIP/cell → same as physics prototype
- Number of channels :
  - 36 instead of 64

Expectations for EUDET

Omega

- 64 channels to read out new 256 pads wafers with 4 chips
  - This is a critical PCB requirement
  - This will make SKIROC2 the biggest chip of the ROC family
    - 50-60 mm^2
- Capability to operate in ILC mode and in test beam
  - This is a physics requirement to take data with EUDET module
  - Calculation of data rates to be validated
- High dynamic range from 0.1 to 2500 MIP
- (Eventually) time measurement to tag events in test beam (not useful in ILC mode)

SKIROC 2 block scheme proposal

We already have that kind of structure on the shelf

20MΩ
1MΩ
Gain selection
8 pF
2 pF
Preamp.
Input
3pF
Calib. Input

Slow shaper
Gain 1
T_p=180ns
Analog Memory
Depth = 16
12-bit ADC (Wilkinson)
Charge Meas.
Peak sensing

fast shaper
Gain 100
T_p=100ns
3-bit DAC adjustment
Trigger out

High gain : 0.5 → 500 MIP
Low gain : 500 →2500 MIP

10-bit dual DAC – common to 64 channels

Time Measurement ? Everything in hand (from spiroc)

Schedule

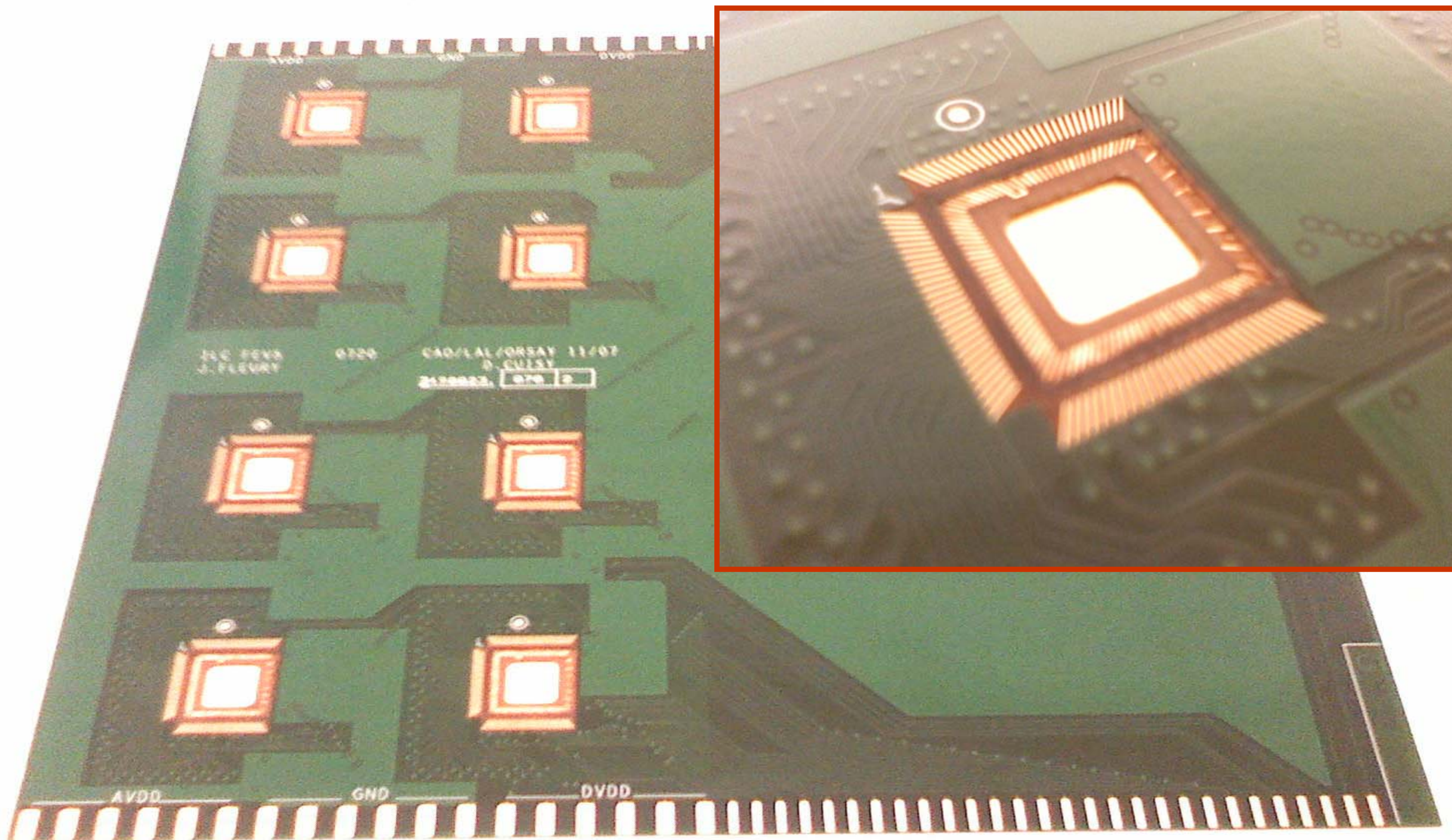
- Skiroc 2 expected to be sent in fab in March'09
  - Sharing of the HARDROC2 and SPIROC2 production
  - If SKIROC 2 is validated → production in hand for EUDET module
  - Cheaper than an engineering run for prototyping due to big silicon area ($60mm^2$ ie ~60k€)
- Next PCB prototype will use SPIROC2 with Hamamatsu wafers
  - Validation of all electronics and assembling process
  - missing : dynamic range (500MIP/2500MIP), granularity
  - PCB in hand before the end of the year ?

PCB design
FEV 5 presentation

Characteristics of FEV5

- Designed for :
  - 6-inch wafers (4 wafers of 9*9cm)
  - 0.5*0.5cm² pads → 324 pads/wafer → 1296 channels/PCB
  - Only 512 equipped with 8 Hardroc Chips
- stitching :
  - No step, solder pins on top layer
  - Exact solder procedure to be defined (Patrick, Maurice, etc.)
- Expected end of January, delivered in June

FEV5 : design

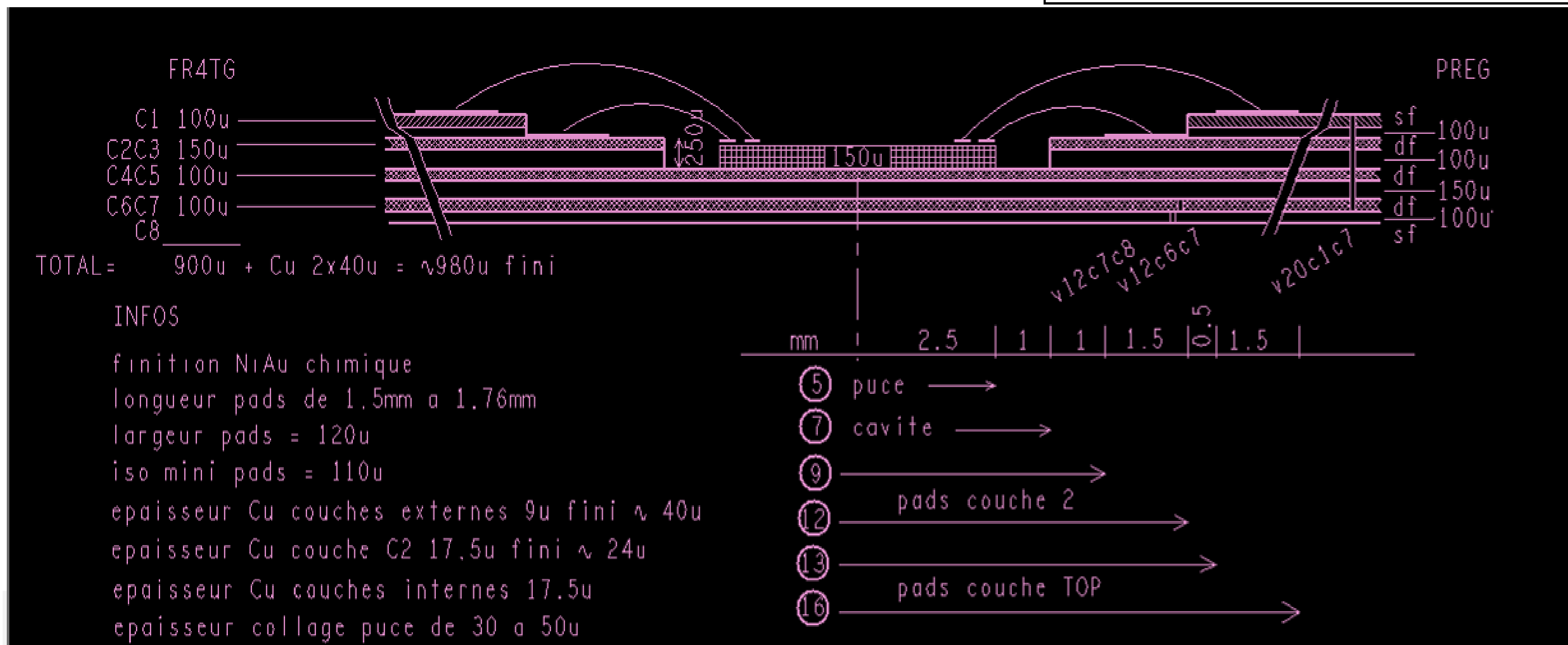


Chip Embedding + PCB Pile-up

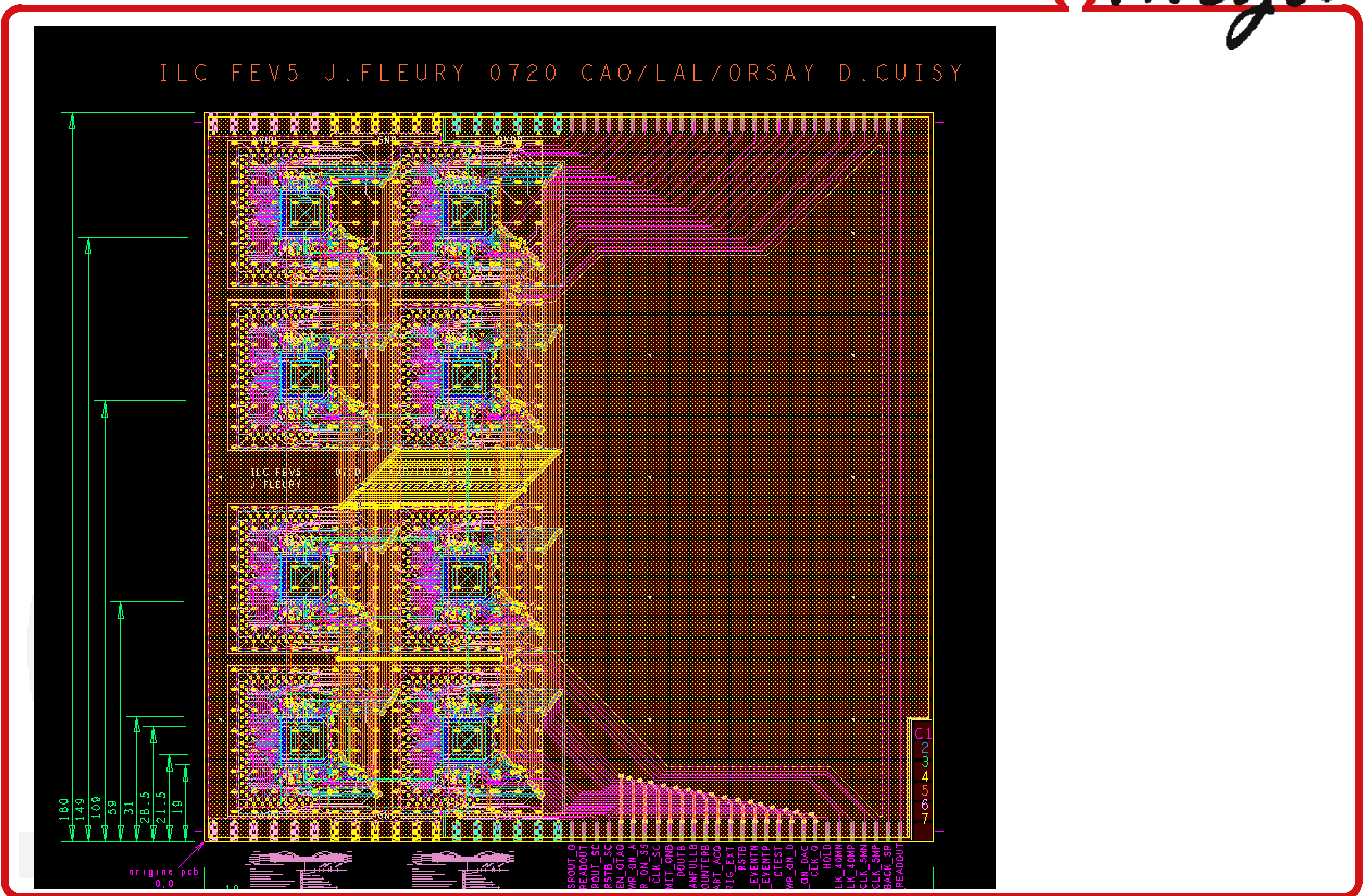
<u>Pile-up</u>

TOP	GND+routing
C2	AVDD+routing
C3	AVDD+DVDD
C4	GND + horizontal routing
C5	AVDD+ vertical routing
C6	GND+pads routing
C7	GND (pads shielding)
BOT	PADS

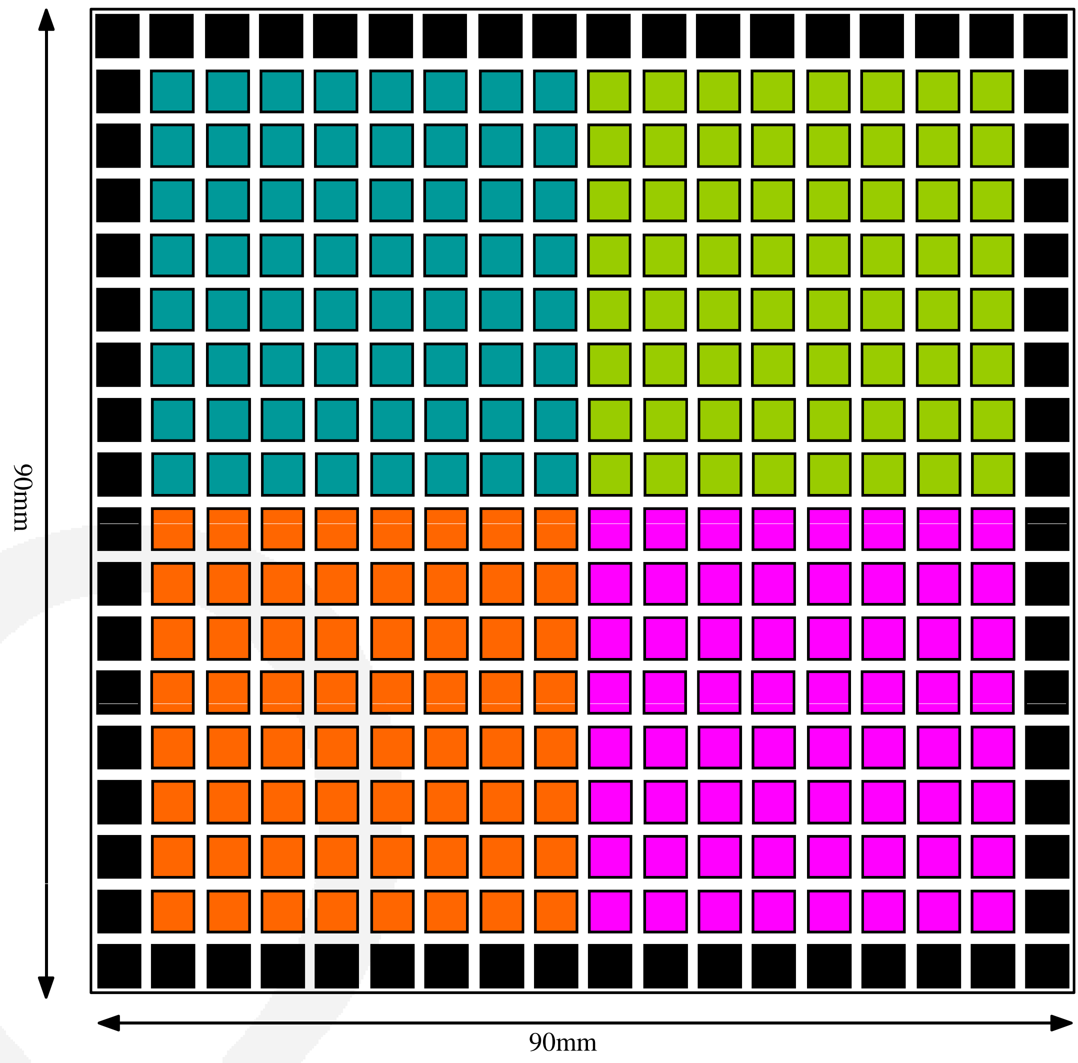
<u>3 drilling sequences</u> :
- Laser C7-C8 120µ filled
- Laser C6-C7 120µ
- Mechanical C1-C7

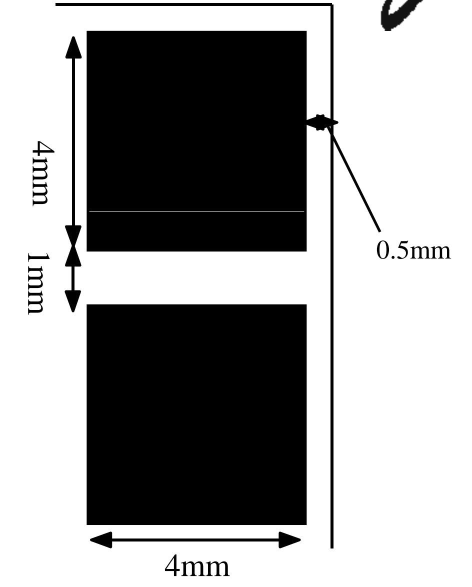


Layout : general



Wafer : channel equipped





Chip 1

Chip 2

Chip 3

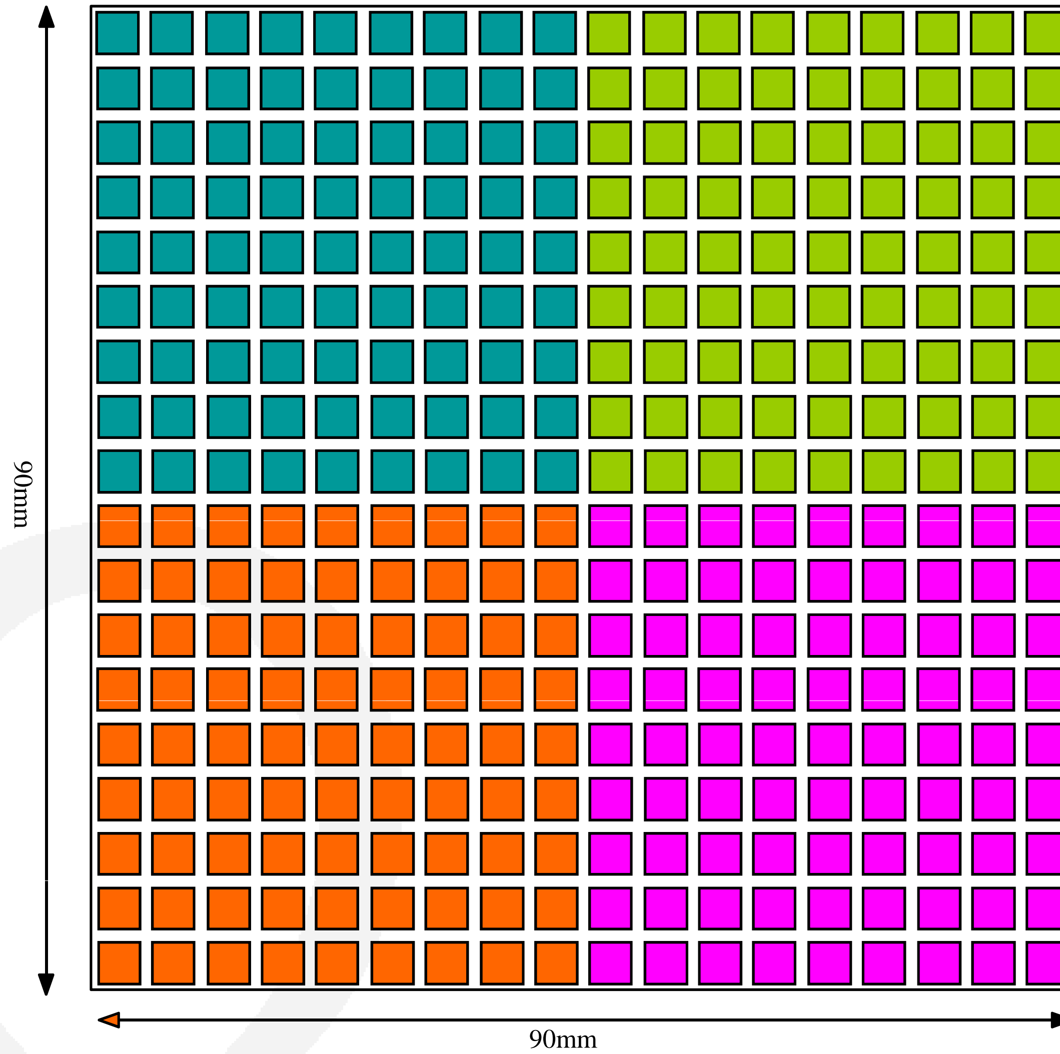
Chip 4

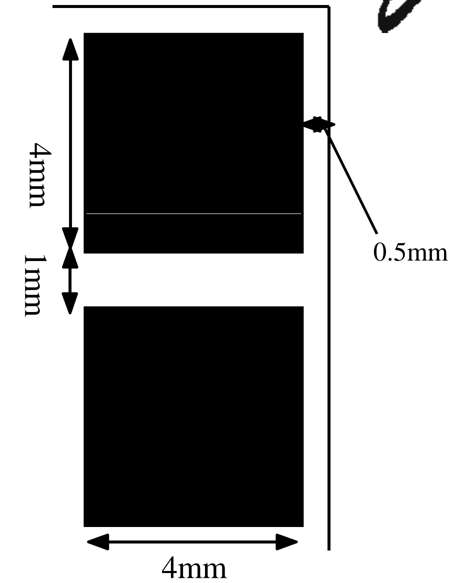
NC

FEV7

- First EUDET compliant PCB, using SPIROC2 in SKIROC mode.
- several pads merged for each electronics input
- Halfway from expected granularity and physics prototype granularity

Ωmega





Chip 1

Chip 2

Chip 3

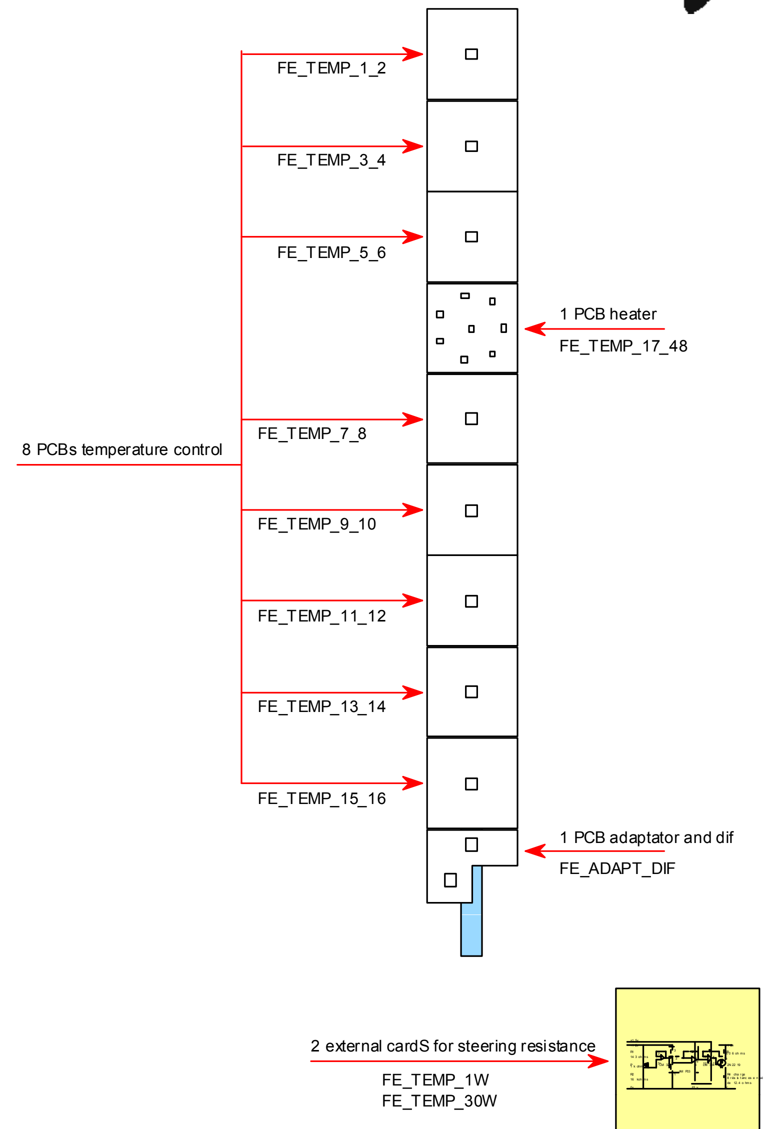
Chip 4

Heating test in slab
Work by P. Cornebise

Heating test

The choice is to manufacture:

- 1 PCB able to simulate the power down to 14.4 mW (1PCB) and power up to 1 W (>7 PCBs)
- 6 PCBs for temperature control
- 1 external card for steering resistance

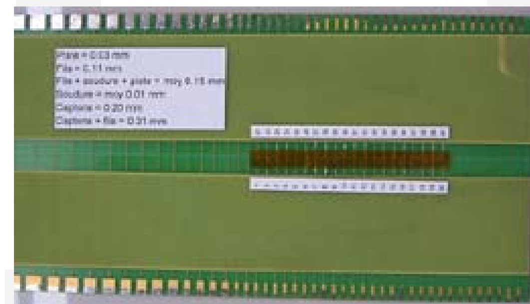


LAL.SE.Interconnexions.P.Cornebise

Test of capton combs

Step 1
Comb 20 ways
Capton width = 19 mm
Wire = 0.25 mm
Track = 0.03 mm
Wire + solder + track = moy 0.29 mm
Solder = moy 0.01 mm

Step 2
Comb 32 ways
Capton width = 19 mm
Wire = 0.11 mm
Track = 0.03 mm
Wire + solder + track = moy 0.15 mm
Solder = moy 0.01 mm



Step 3
Comb 20 ways
Capton width = **5 mm**
Wire = 0.11 mm
Track = 0.03 mm
Wire + solder + track = **moy 0.15 mm**
Solder = moy 0.01 mm
T max relieved on the top = **45.6 °C**
T max relieved on the lower side wafers = **42.5 °C**

The combs are made by positioning the wires on a layer of capton scotch and covered by another layer of capton scotch.
Then the wire are solder alternately starting with wire n° 1 and n° 10, 20, 2, 11, 21…
Soldering iron used: Weller ws50 at 350°C
The temperature is controlled step by step with PT100 placed on the top and on the bottom (wafers side)

LAL.SE.Interconnexions.P.Cornebise

Conclusion

Omega

- PCB design
  - FEV5 engineering done
  - NOT SO EASY TO BUILD → 6 months delayed !
  - Opportunity to have 256 ch. Wafers ? (5.5mm pads)
    - For FEV8 design
    - To be available in Spring 09
  - FEV7 design using hamamatsu Wafer and Spiroc 2 in 2008
- Front-end ASIC design
  - Skiroc2 planned for march 09
  - All test with Spiroc2 before then
- Heat simulation
  - Using first mechanical demonstrator to validate thermal models