CALICE Collaboration Meeting

Power efficient 12-bit PIPELINE ADC for the ECAL

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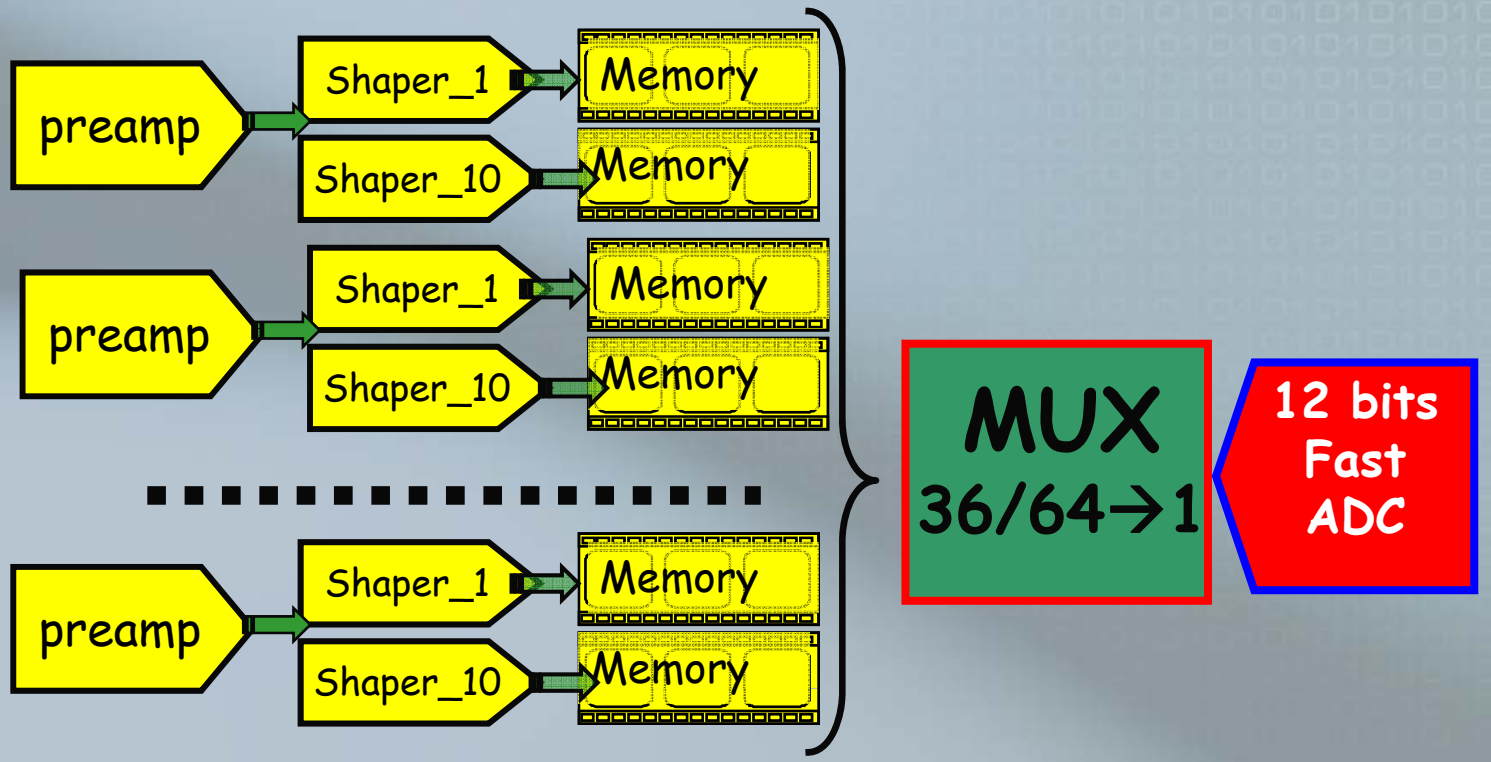
Outline

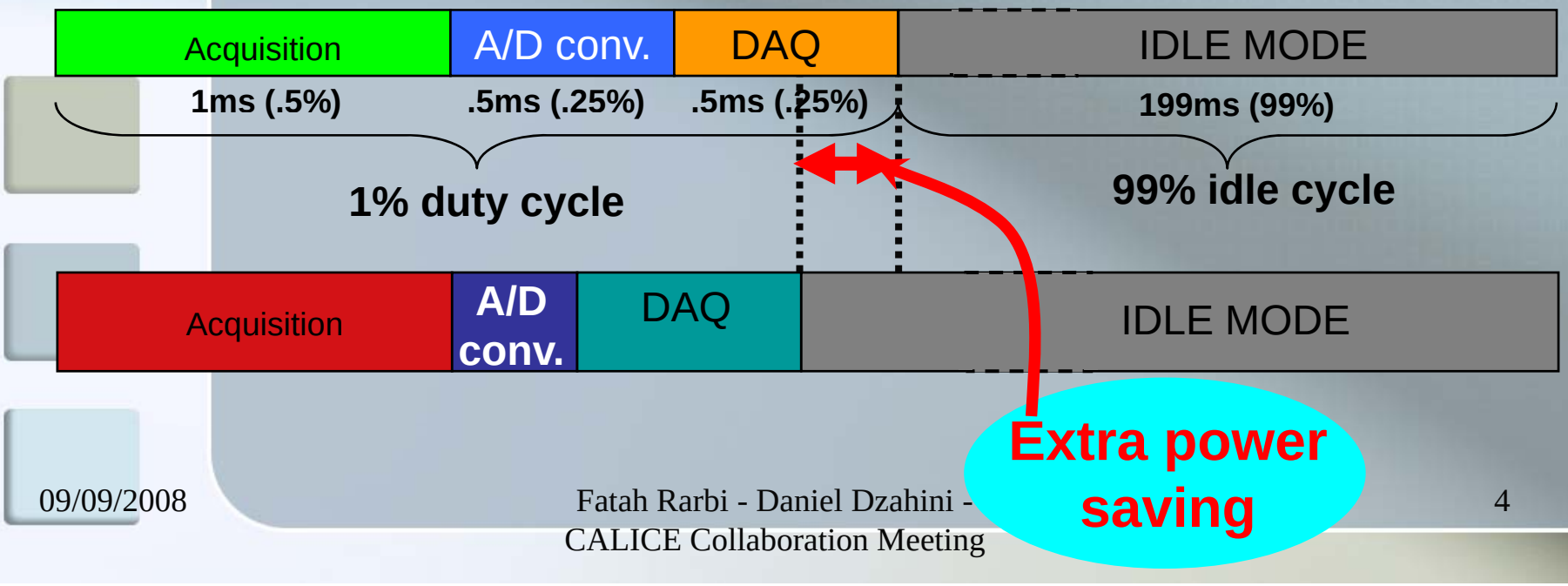
- Digitizer for CALICE
- Why a high speed ADC?
- Pipeline ADC
  - Full 1.5 bit
  - Multi-bits prototype
- Analog MUX 36 to 1
- Conclusion

Digitizer for CALICE

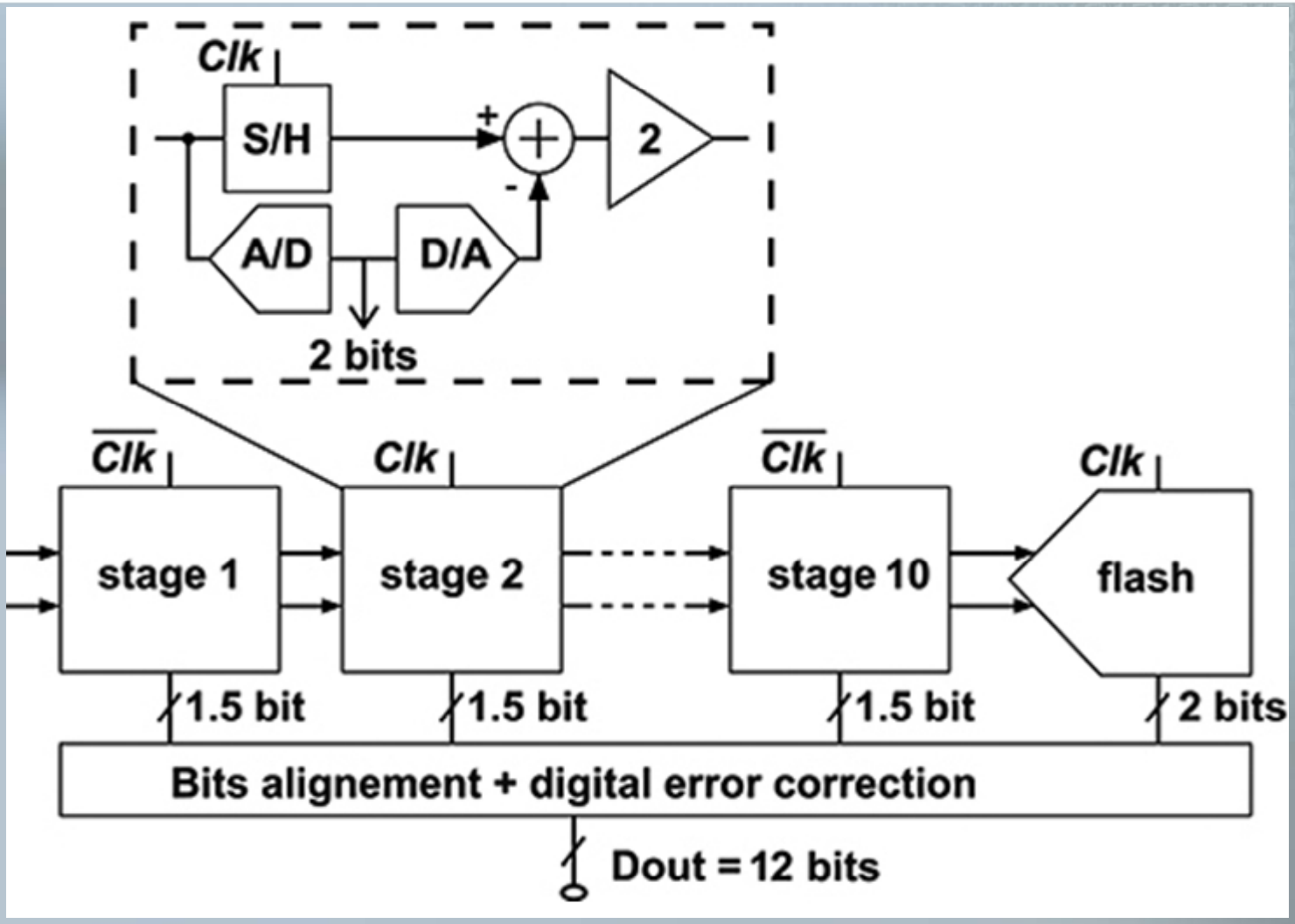


Why a high speed ADC?

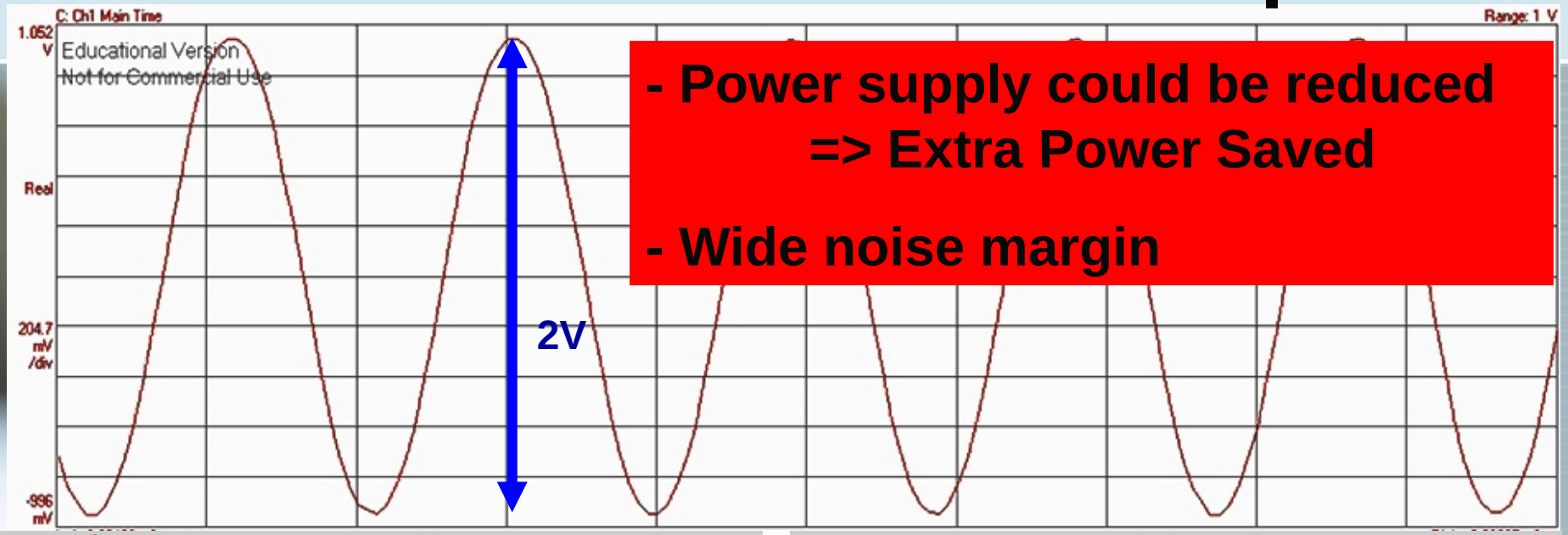
- Multiplex 36 to 1 ADC
- High speed converter:
  - Read all channels faster
  - More “IDLE mode” time => **Saving power**
  - digital noise source from one ADC



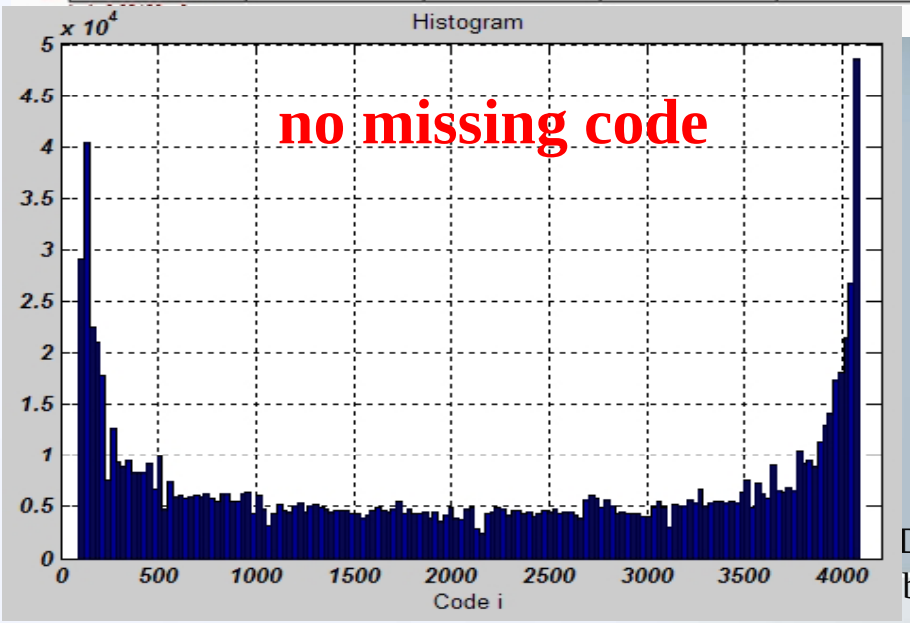
Pipeline ADC

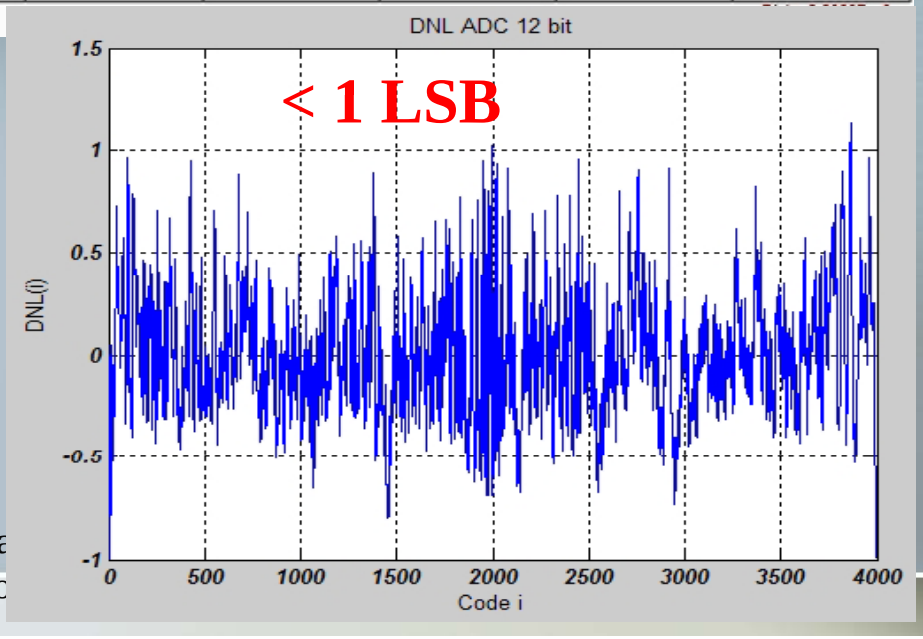


Measurement Test of ADC Pipeline

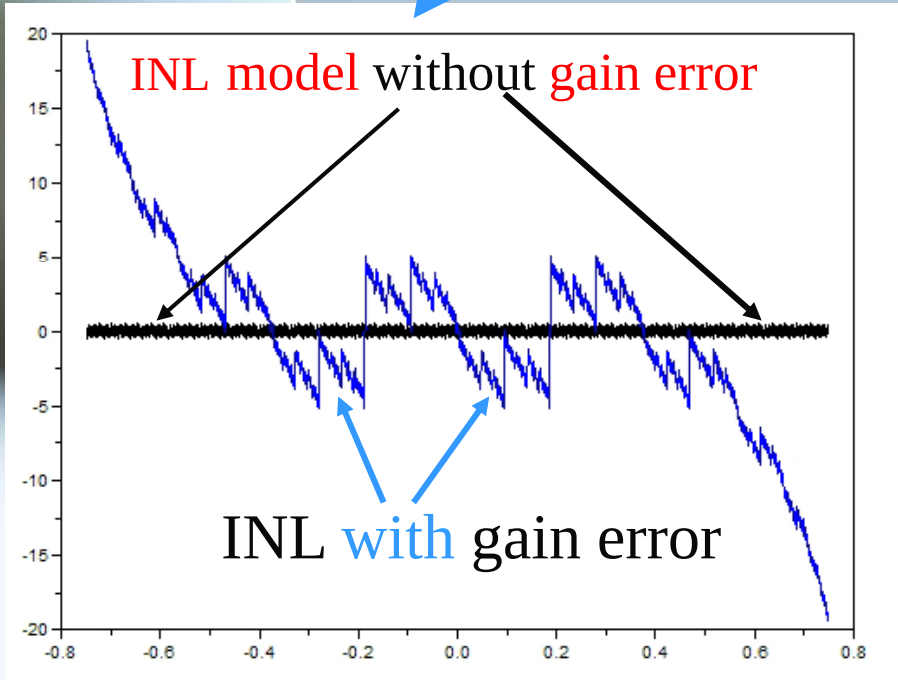


- Power supply could be reduced
  => Extra Power Saved
- Wide noise margin





INL from ADC Model with and without gain error versus testing results

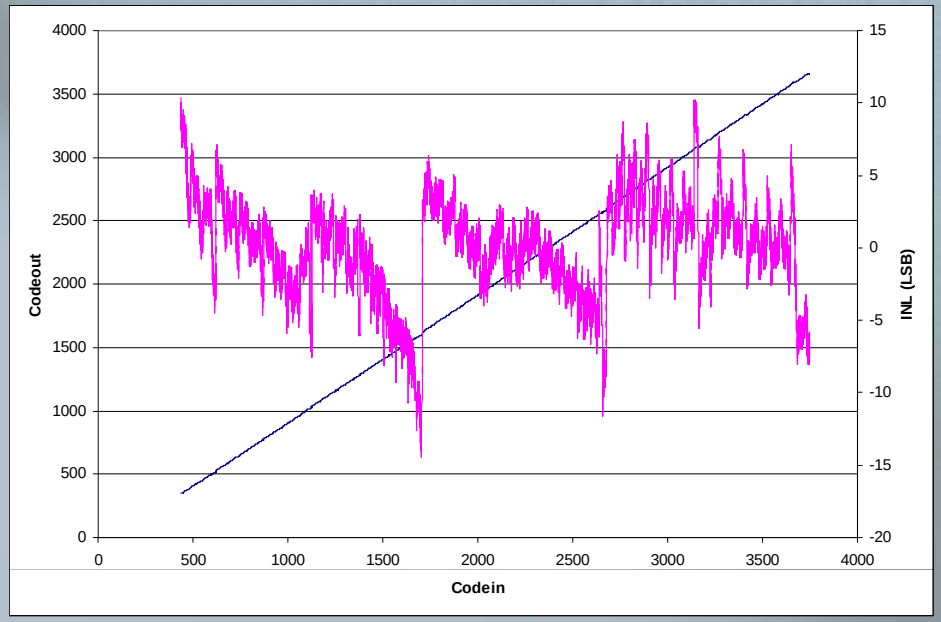


This shape corresponds to:

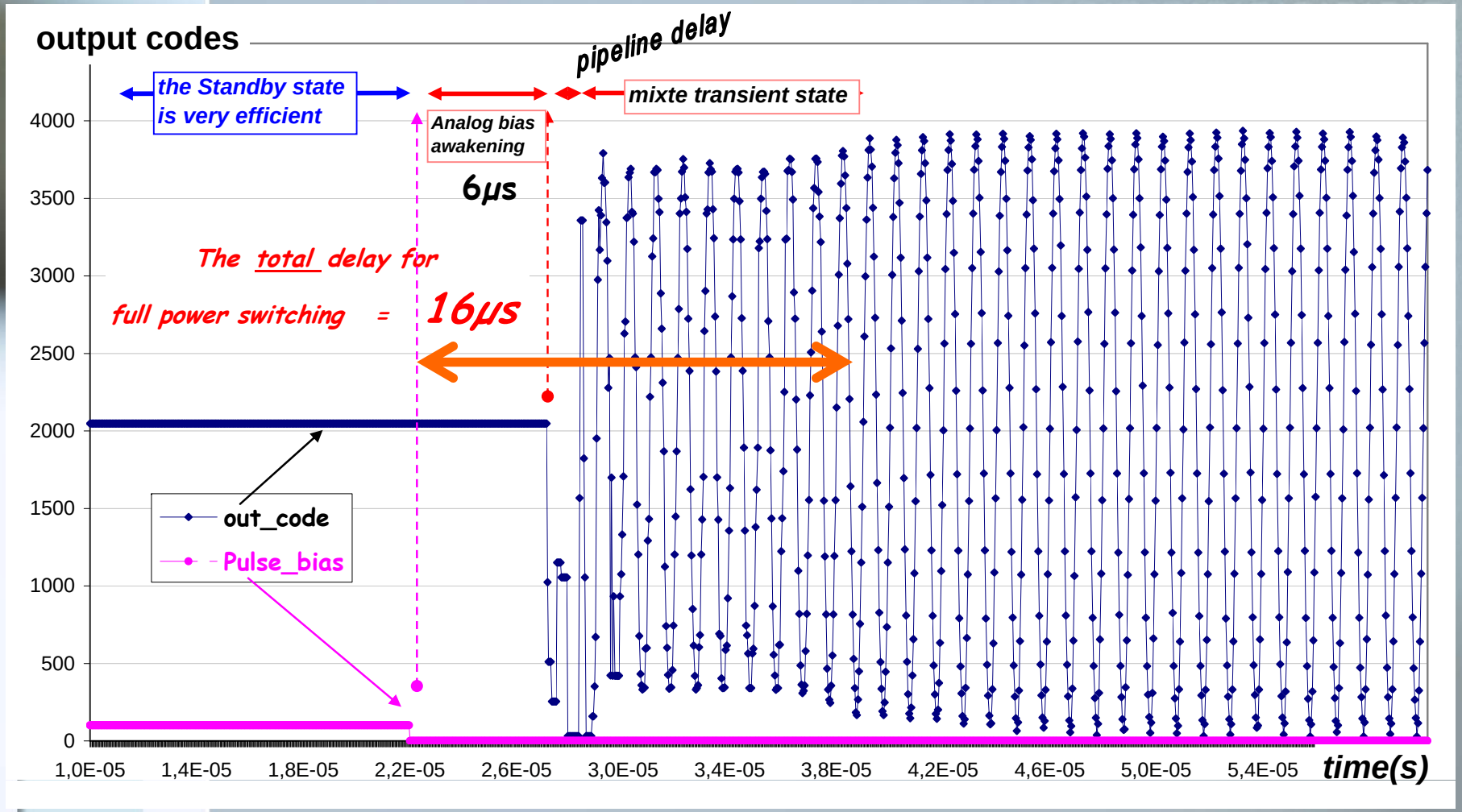
→ Capacitance matching

→ Parasitic capacitances

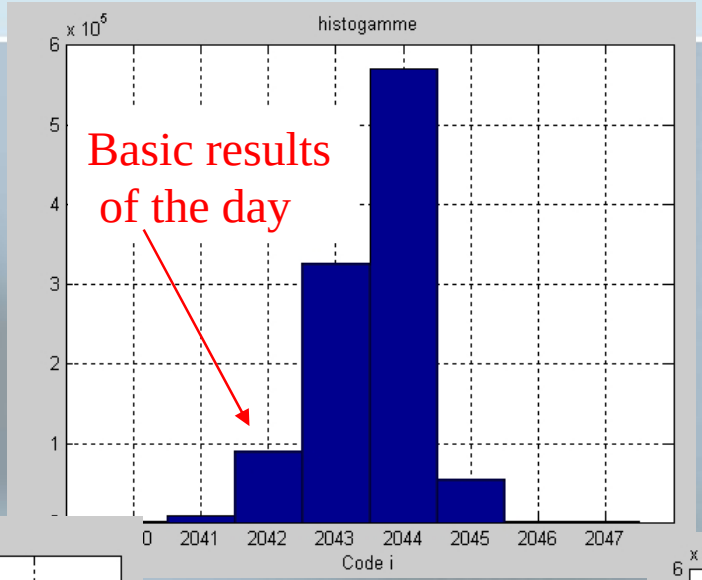
→ Jitter

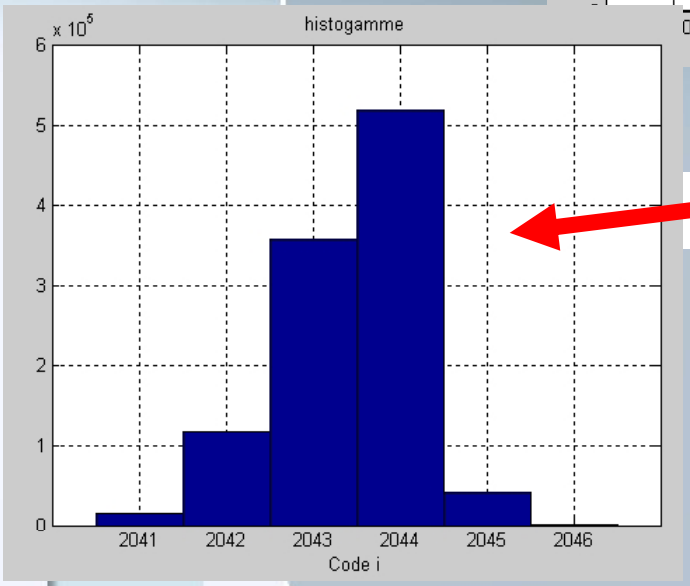


Power pulsing:
output codes point of view=>16 to 20µs



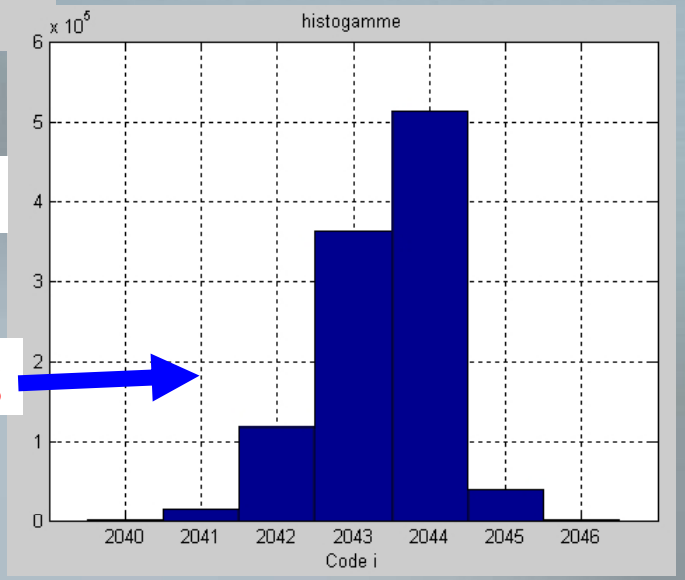
Power Pulsing reliability



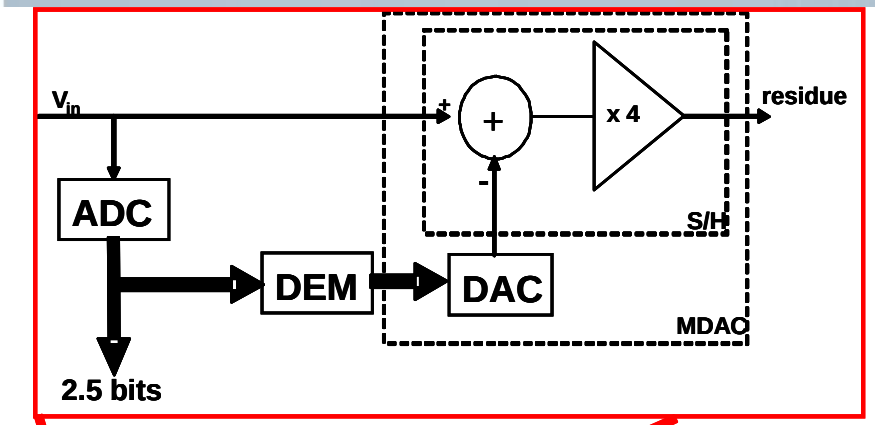


After 20 power cycling

After 40 power cycling



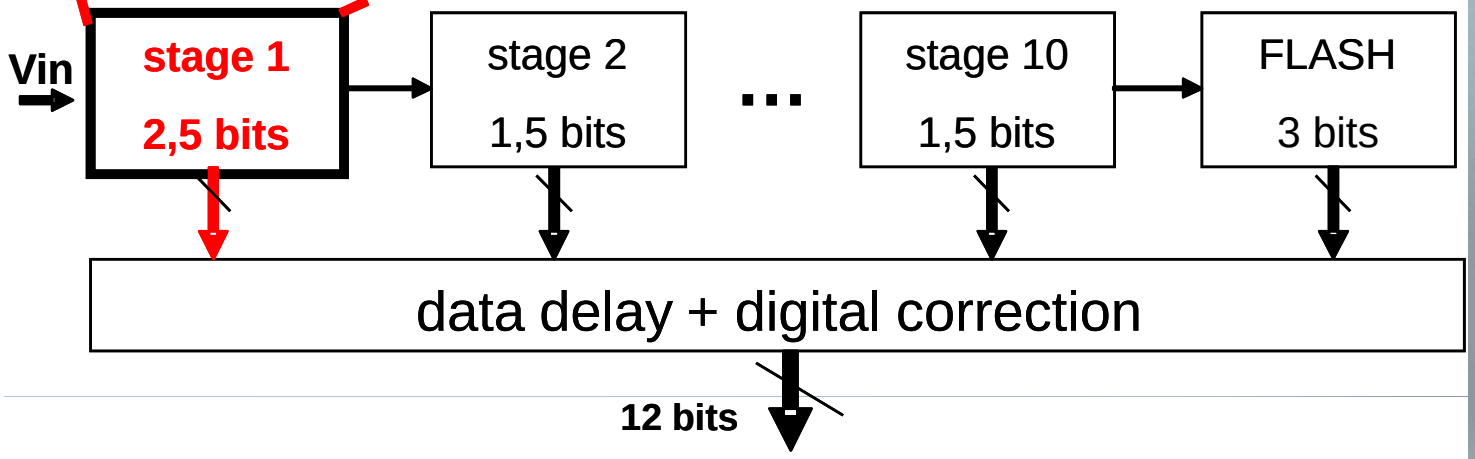
New prototype



More logic for DEM
Should work @**25-30MHz**
Power => **< 40mW**

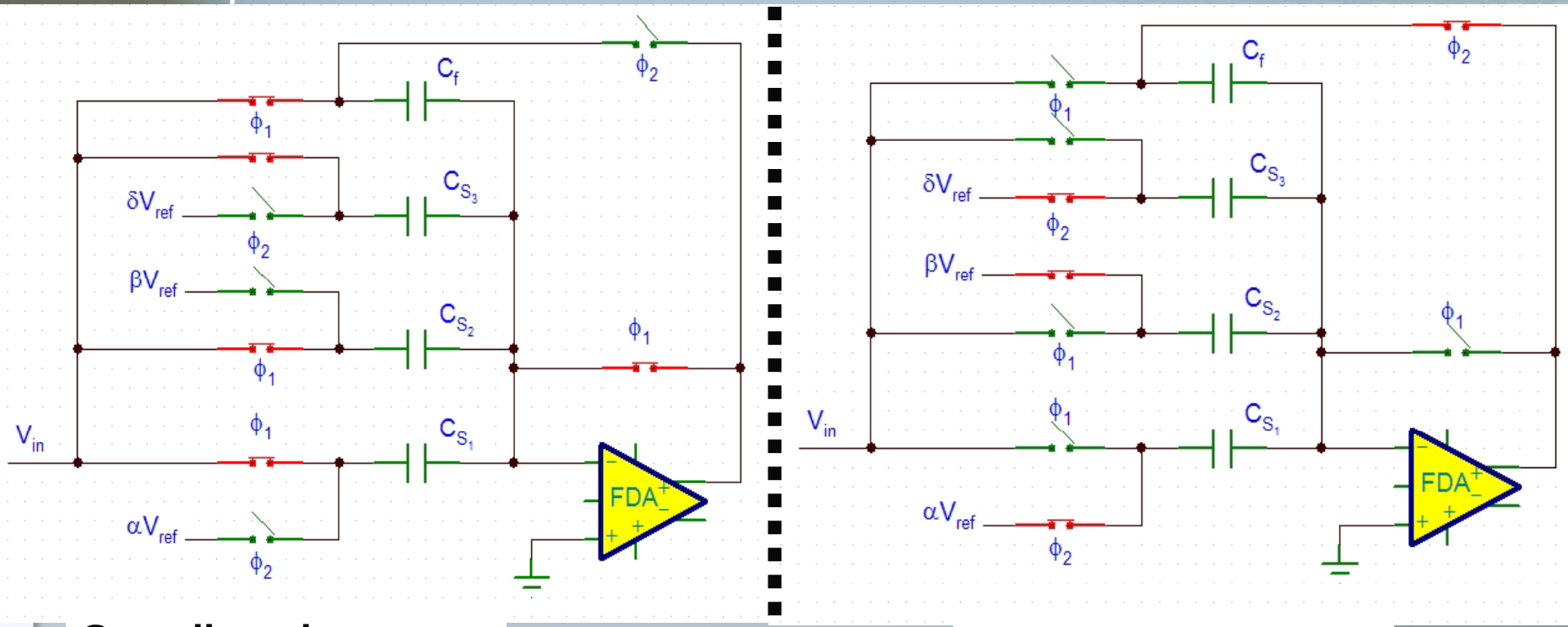
Front-end stage

Back-end ADC



MDAC 2.5 bits

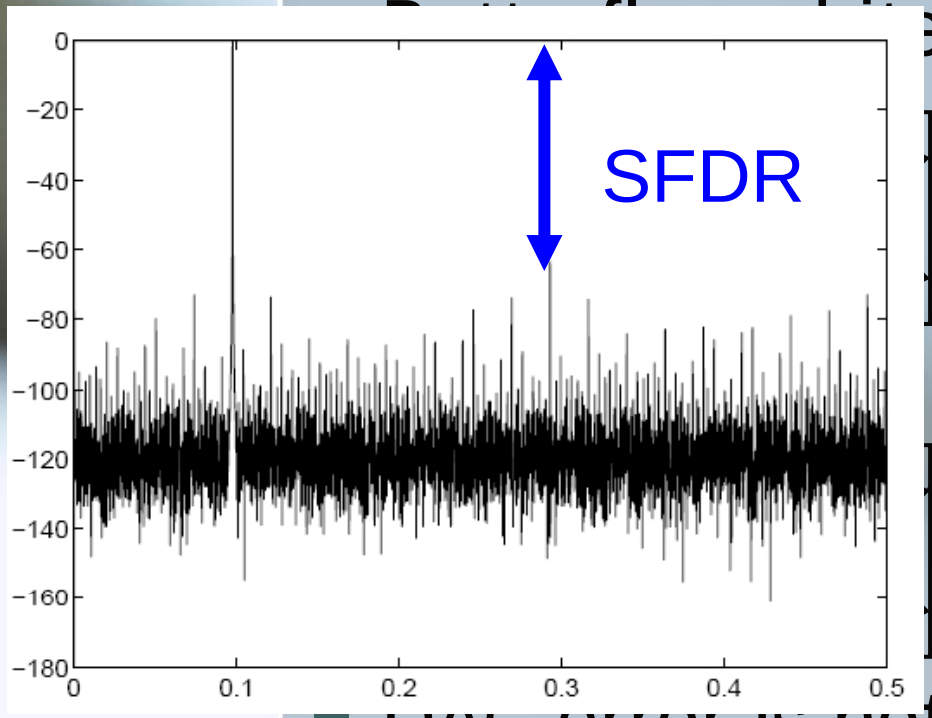
- Architecture

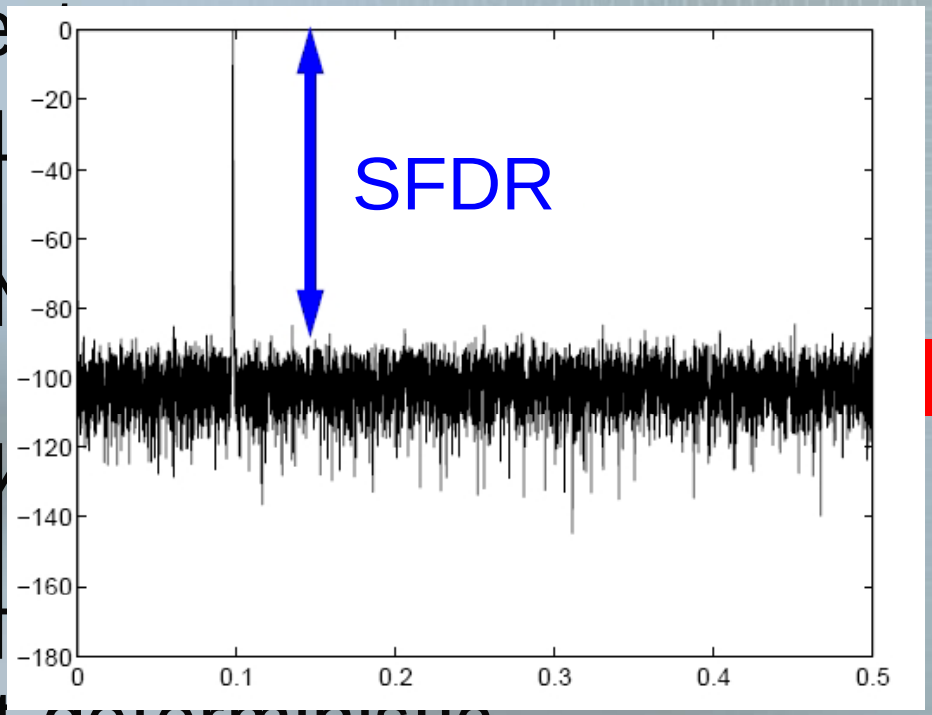


Sampling phase | **Hold phase**

$V_s = 4 \times V_{in} - 3 \times \mu V_{ref}$, μ=[-1, 0, +1] depends on sub-ADC output

Dynamic Element Matching

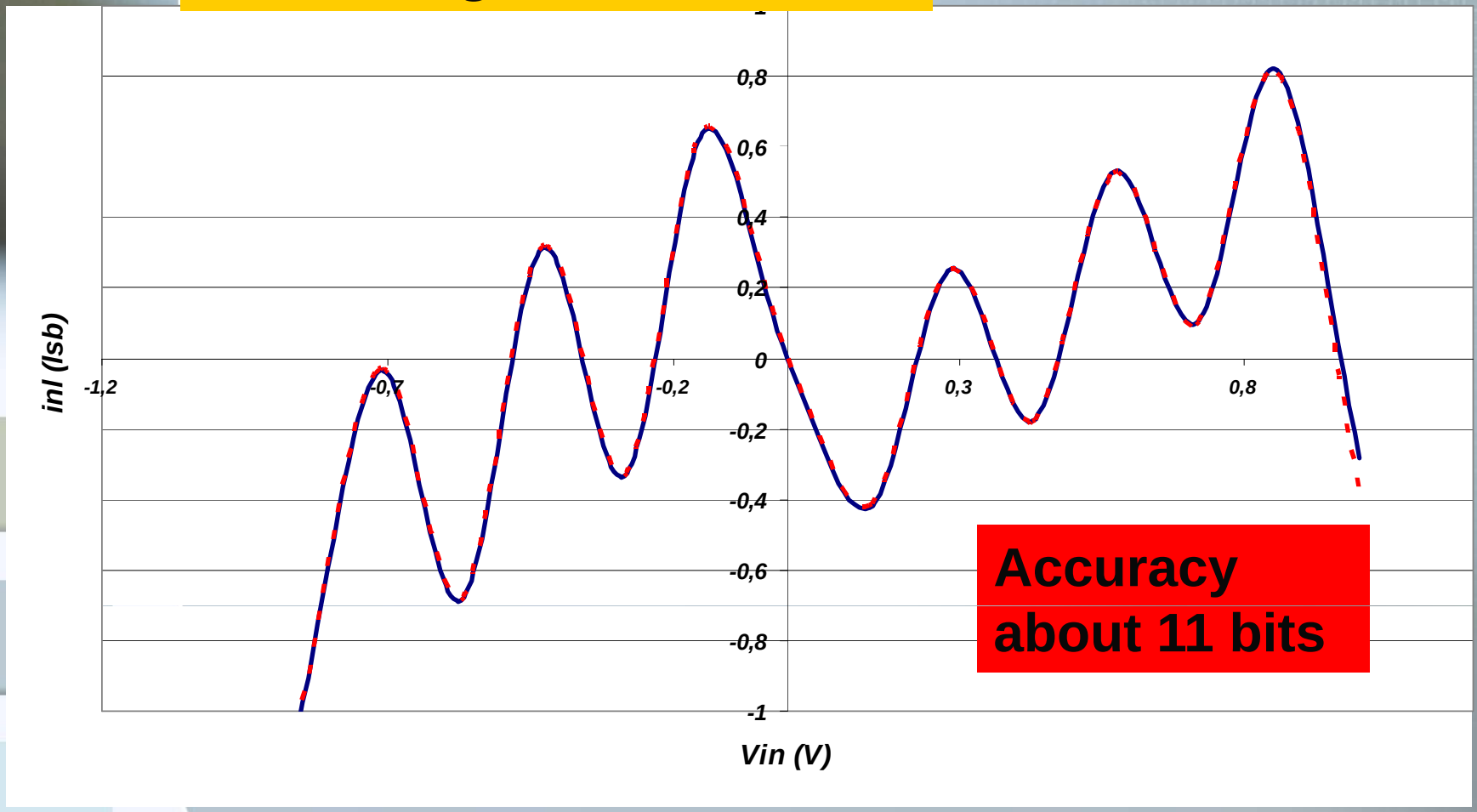




- DAC error is not deterministic
- Converts distortion into white noise with a DC component

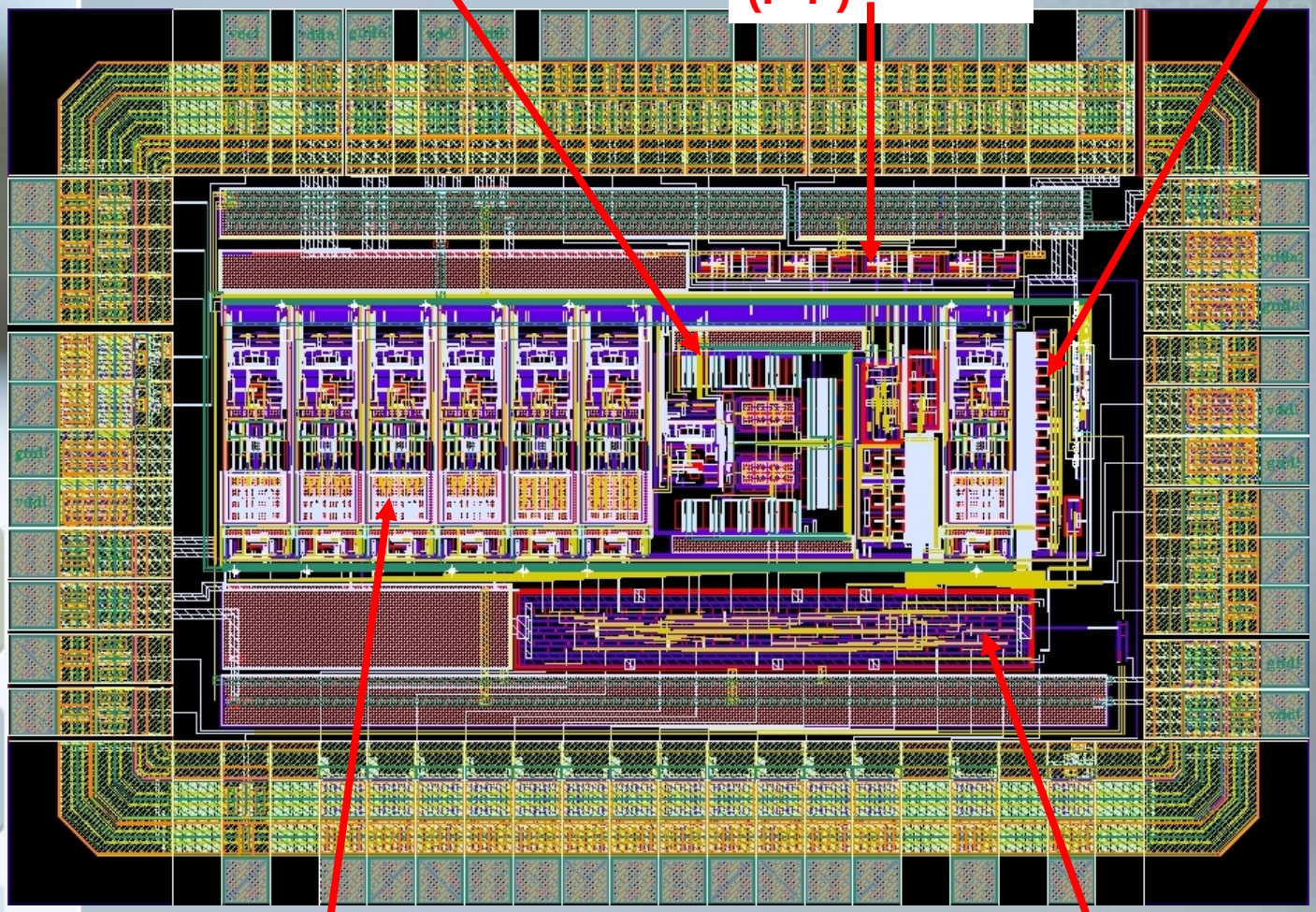
MDAC 2b5: Linearity

First stage of the ADC



Accuracy about 11 bits

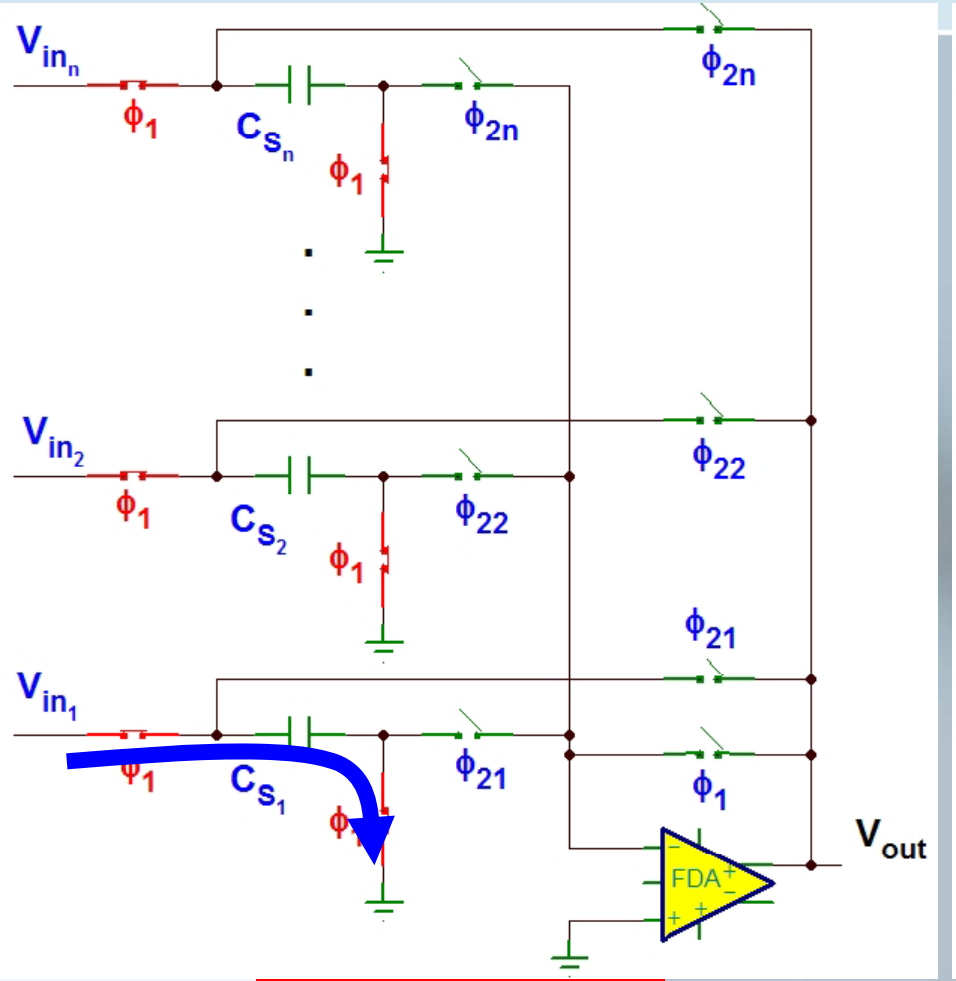
Prototype: July 08 (4mm² or .9*1.9 mm² (core))



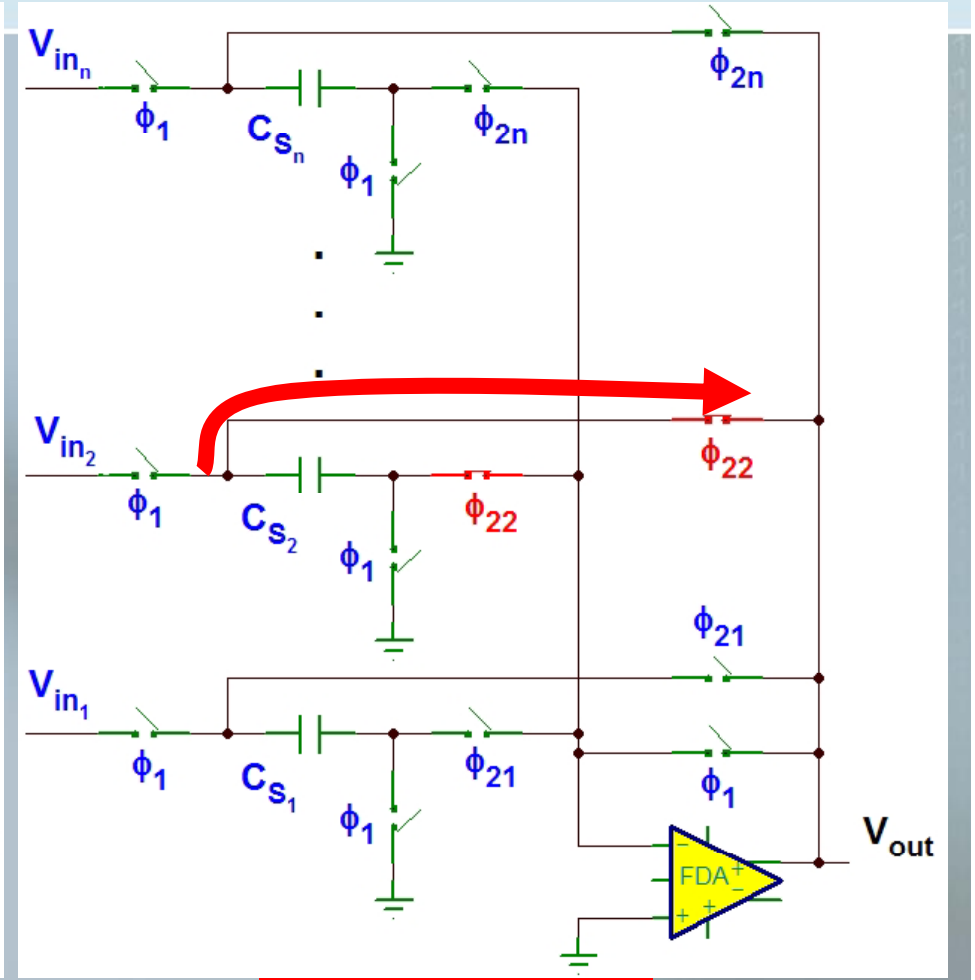
Analog MUX 36 to 1

- Architecture:
  - Flip-Flop
  - Pseudo differential input
- Power dissipation
- Linearity

Architecture



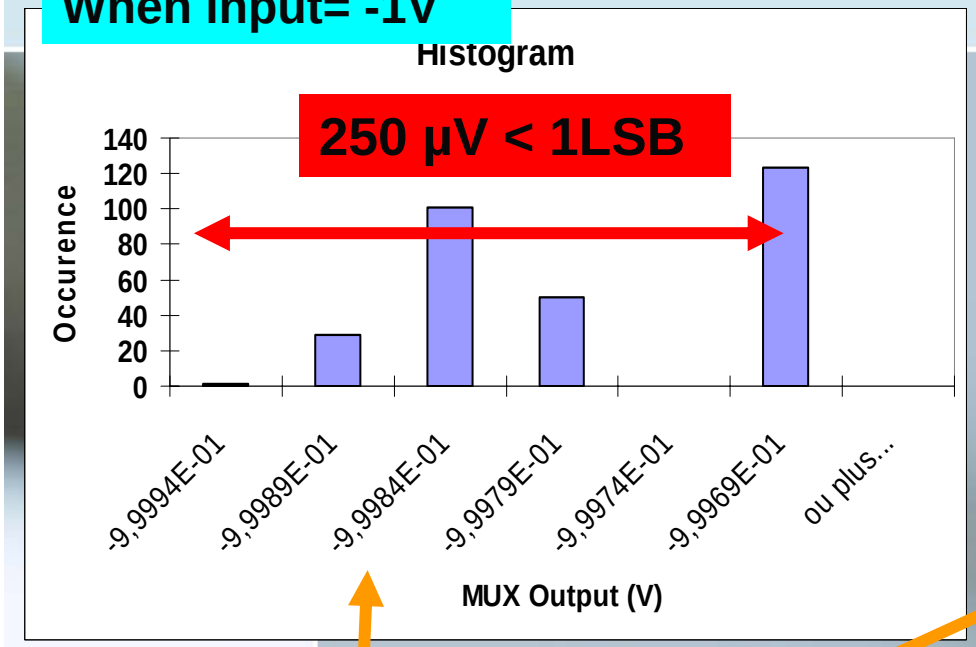
Write mode



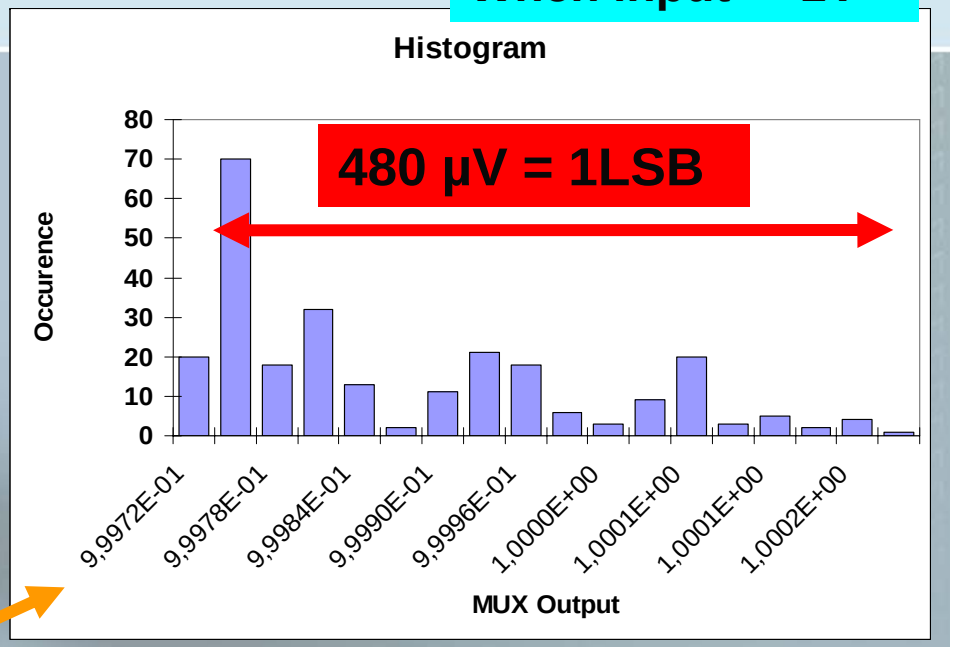
Read mode

MUX Accuracy

When input= -1V

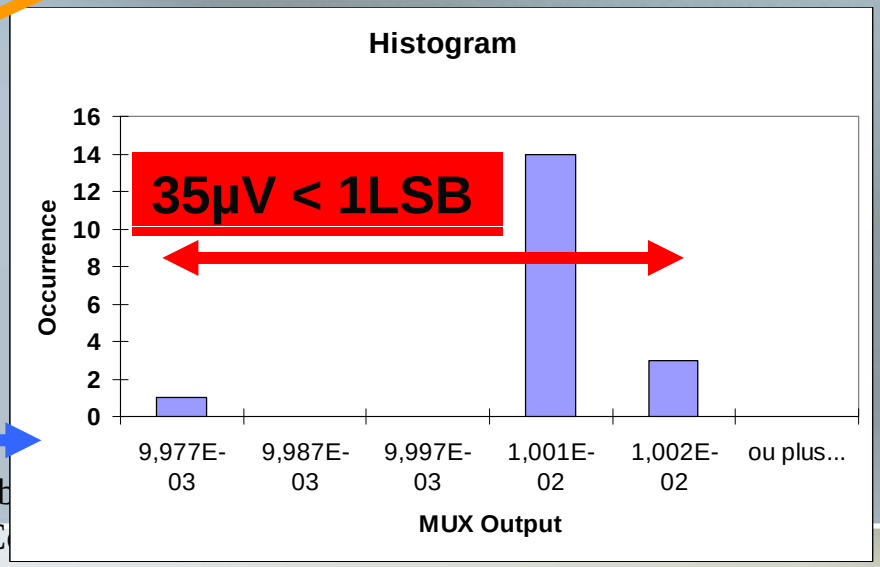


When input= +1V

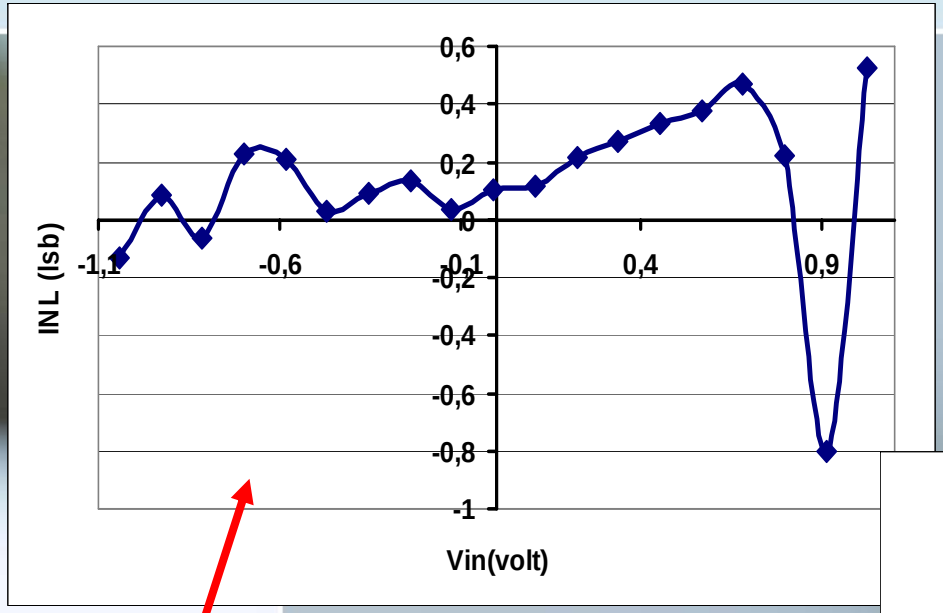


High signal => +/- 1V

Small signal => 10mV

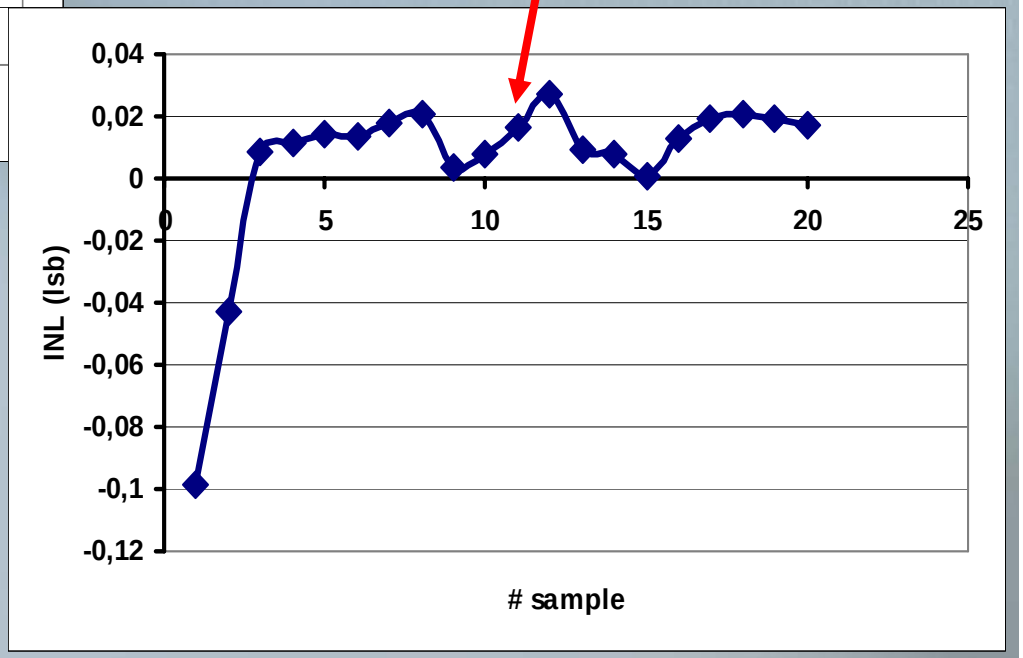


Linearity

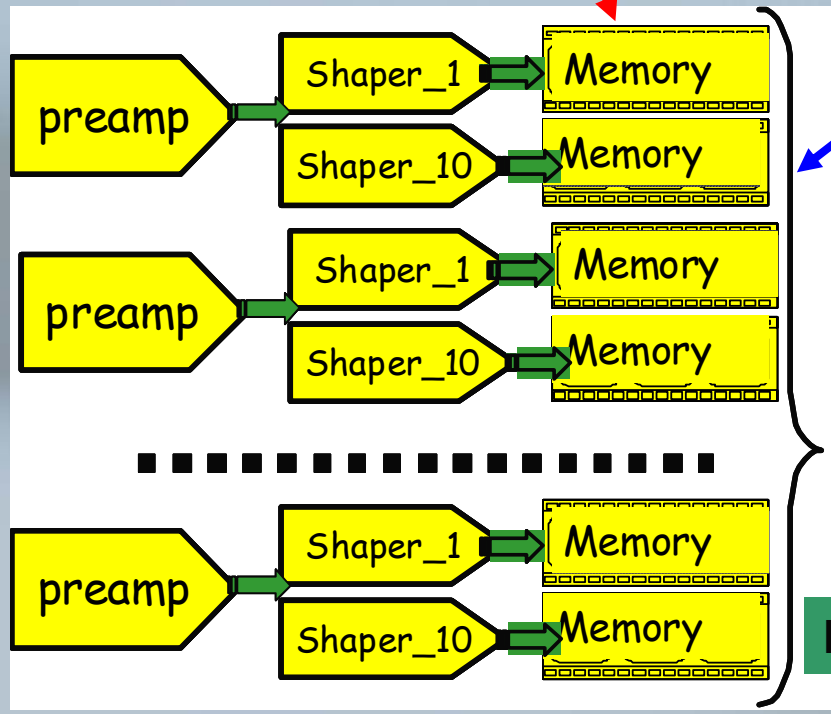


Ramp signal

Constant signal (10mV)



Total Power consumption



P_{MUX}<10mW

T_c=40ns/code

P_{ADC}=37mW

T_T (Total Time conversion) = 40ns x 36 x 5

= 7.2µs

ADC Power Consumption per chip = (P_{tot} x T_T)/200ms

= 1.6µW → 45nW/channel

Conclusion

- Pipeline ADC: 12 bits
  - V_{dd} = 3.3V
  - **Dynamic range:** 2V
  - **Sampling rate: 25MS/s**
  - **Power dissipation**: **37mW**
  - **FOM**: **1.48mW/MHz**
- Analog MUX 36 to 1
  - Pseudo differential input
  - **Dynamic range :** 2V
  - **Power dissipation: <10mW**
- Total Power= **45nW/Channel** if 36 channels to 1 ADC
- Next steps
  - Test of this prototype
  - Power Supply reduction to 2.5V → 1V dynamic
  - Gain error Correction → Extra power reduction

CALICE Collaboration Meeting

Thank you for your attention

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