# A 12-bit cyclic ADC
## dedicated to the VFE electronics of Si-W Ecal

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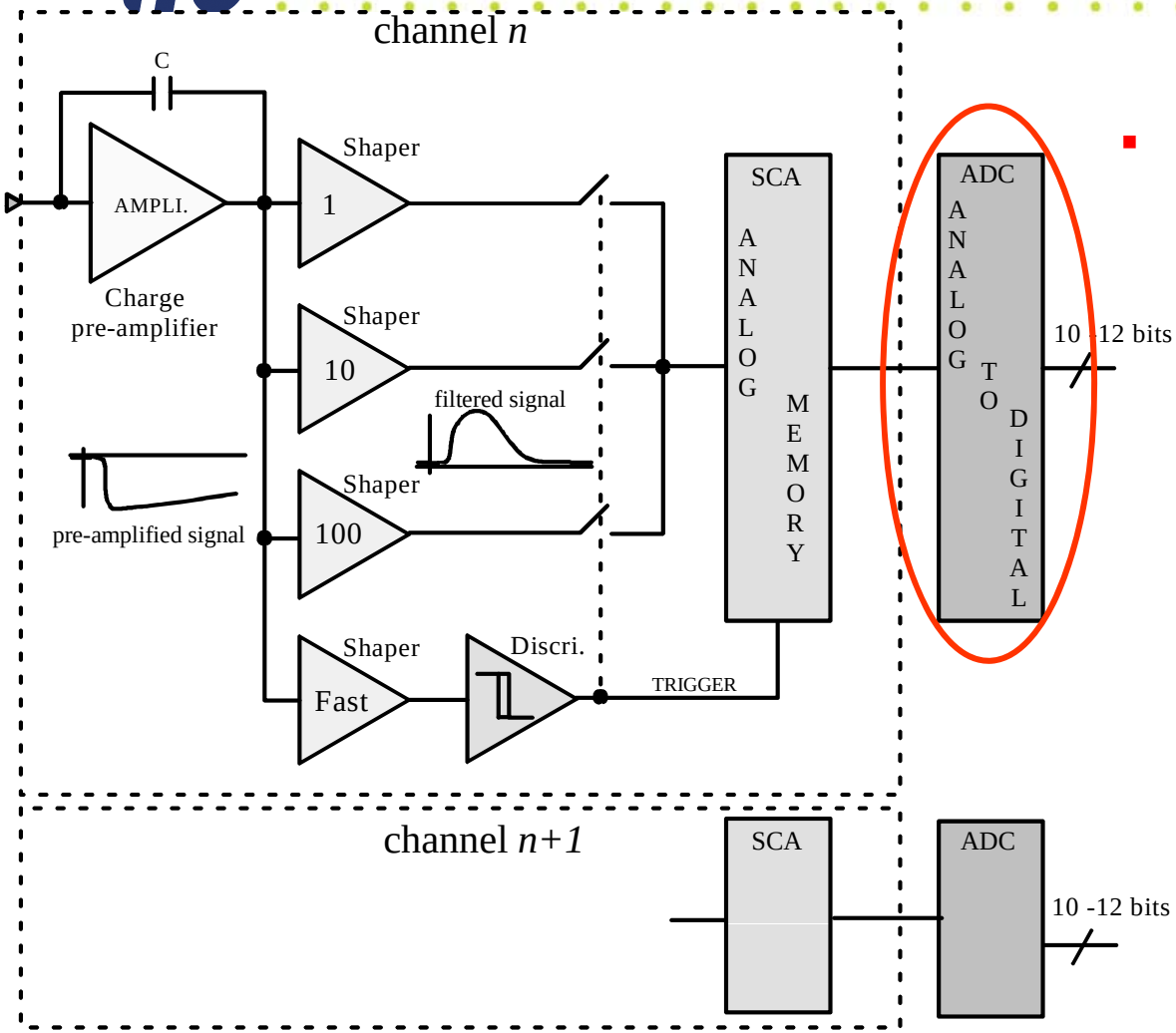
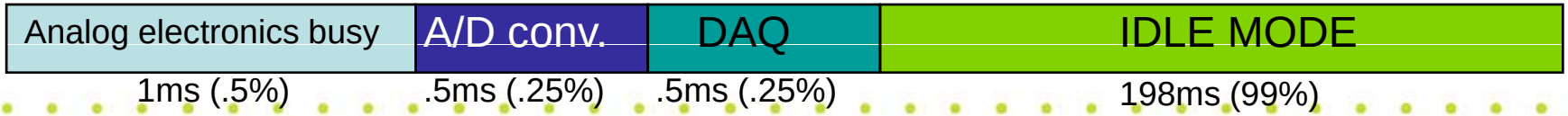
# VFE electronics of Si-W Ecal

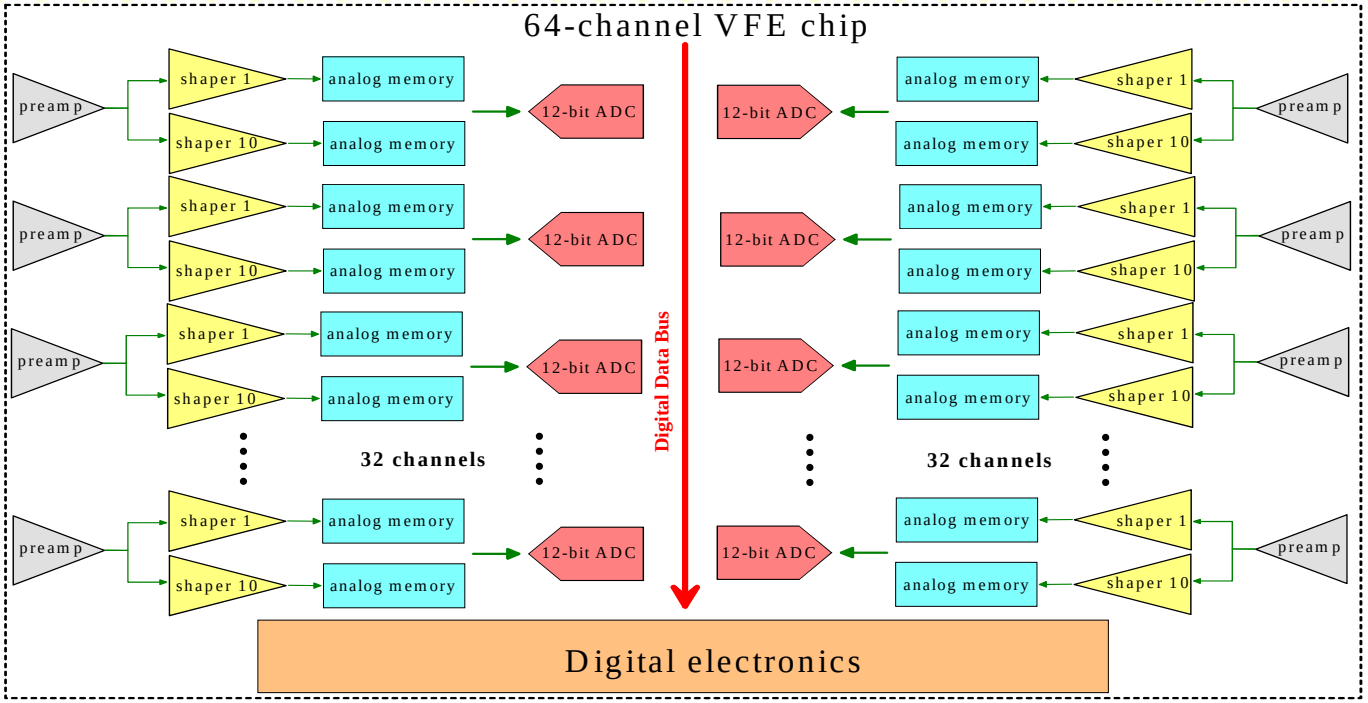



- **Main requirements for the ADC:**
  - Ultra low power:
    - **2.5µW/ch** (10% of the VFE power budget)
    - **Power pulsing needed**
  - Resolution:
    - **10 bits if 3-gain shaping**
    - **12 bits if 2-gain shaping**
  - Time of conversion: time budget of 500 µs to convert all data of all triggered channels
  - Die area:
    - **as small as possible…**

    **(0.225 mm2 per each channel of Skiroc without ADC)**



# Proposal: one ADC per channel




**With <u>one-ADC-per-channel</u> architecture:**

☺ **Short analog sensitive wires from memory to ADC**

☺ **A digital Data Bus far from sensitive analog signals**

⇒ **Integrity of analog signals saved**

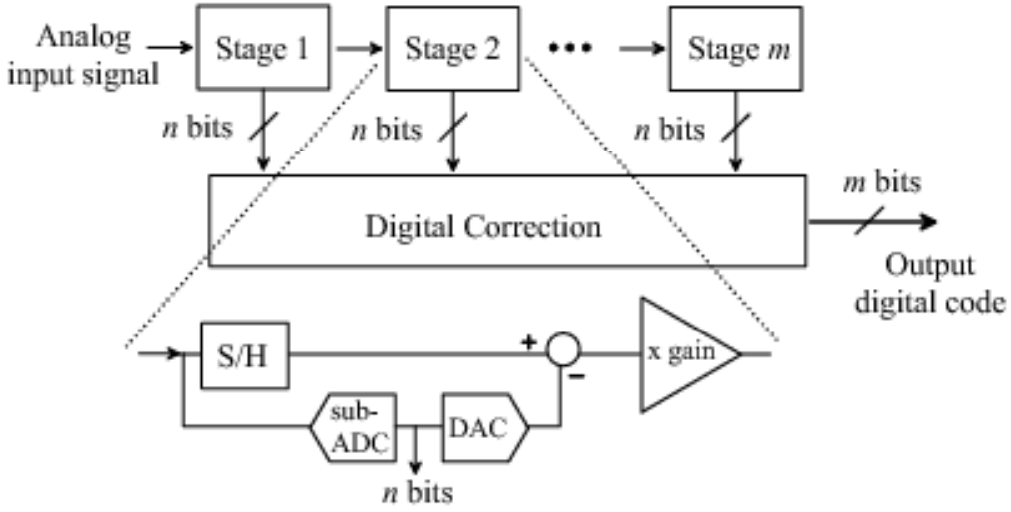
☺ **Only ADCs of triggered channels powered ON** ⇒ **Power saved**

☺ **Conversions of channels done in parallel** ⇒ **No "fast" ADC required**

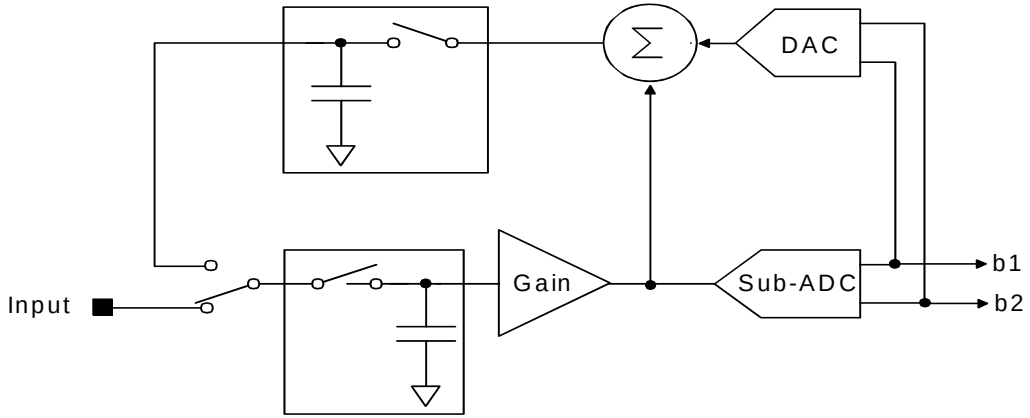
☹ **Pedestal dispersion of ADC "added" to the dispersion of the analog part .... but calibrated**

# Two candidates for the architecture of the ADC

**Pipeline ADC**




**Cyclic ADC**



# Pipeline and Cyclic performance

| | Cyclic | Pipeline |
|---|---|---|
| Resolution | 12 bits | 12 bits |
| Time for one conversion | 12 clock periods | 1 clock period(1) |
| Power consumption (norm.) | 1 | 12 down to ≈ 6(2) |
| Integrated power cons. (time * power cons.) | 12 | 12 down to ≈ 6(2) |
| Area | 1 | 12 down to ≈ 10(3) |

[1] after a latency of 12 clocks period for the first conversion
[2] if a power optimization on each stage is implemented
[3] if a capacitor size optimization per each stage is implemented

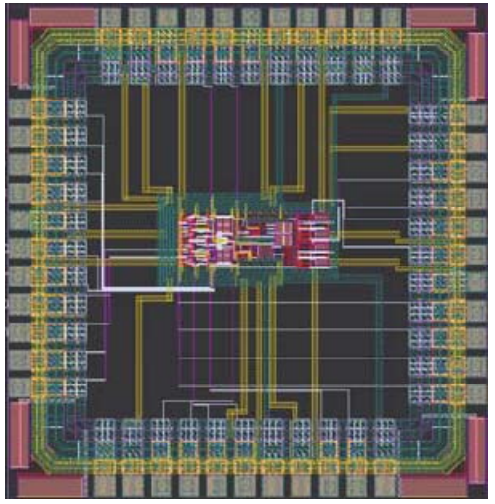
# A 12-bit cyclic ADC (1)

The 12-bit cyclic ADC prototype designed @ LPC Clermont:

- Sent to fabrication in March 08, 10 chips delivered with delay in July
- Technology: 0.35 µm CMOS Austriamicrosystems
- ADC designed with the validated building blocks (Amplifier & Comparator) of our 10-bit pipeline ADC (published in IEEE NS in June 08) but optimized for the 12-bit precision requirement

  → enhanced building blocks tested with a dedicated chip (July 07)
- 1.5 bit architecture (2 bits per cycle)

  → relaxed constraints on offsets of comparators
- External bits processing (deserializer & 1.5bit algorithm)
- Power pulsing system implemented



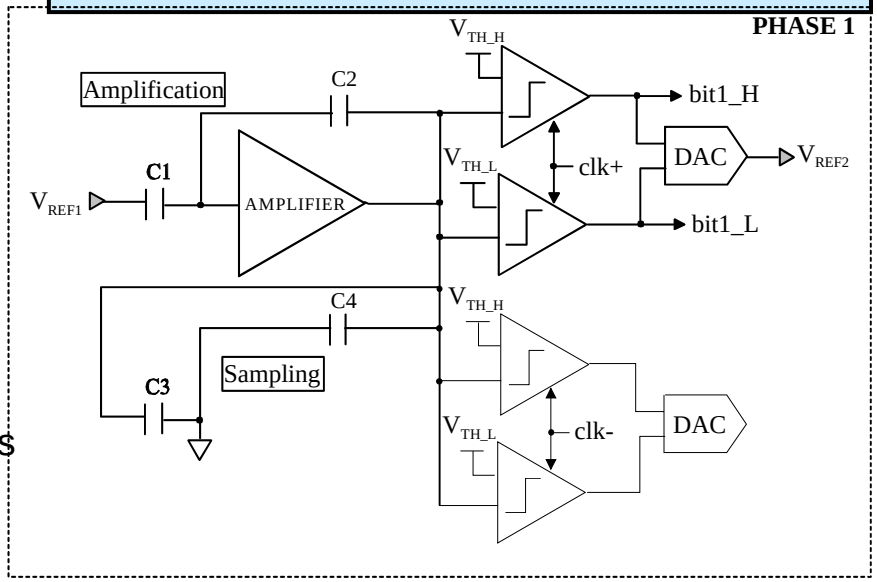
**Layout of the chip**

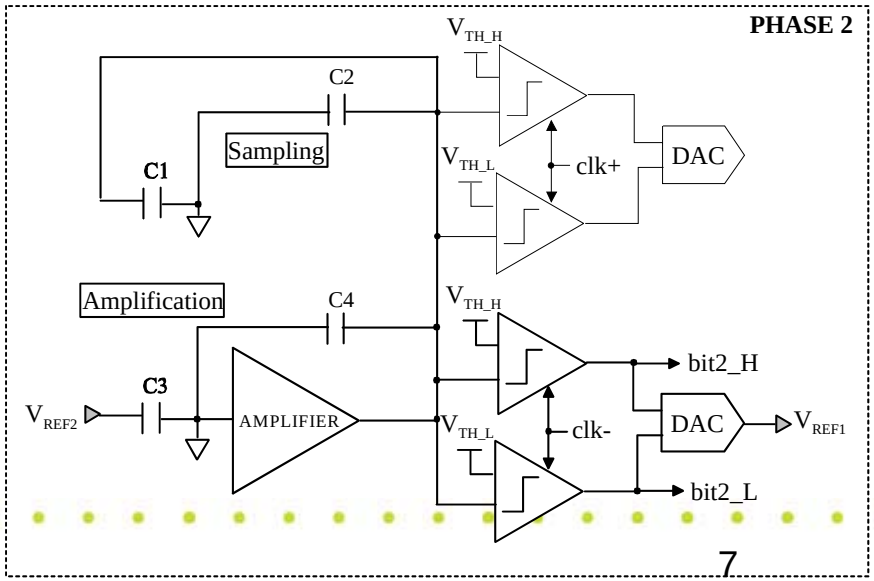
# A 12-bit cyclic ADC (2)

- Performance of the cyclic ADC:
  - Improved architecture: calculation of two bits during one clock period
  - → Time of conversion: 7µs w/ 1MHz clock freq.
  - → 1 ampli. + 2*2 comp. + 2 capacitors arrays
  - Consumption: 4 mW/3.5V
  - Integrated cons. with power pulsing:
    - ✓ 0.7 µW with analog memory depth of 5 events
    - ✓ 2.2 µW with analog memory depth of 16 events
  - Area: 0.175 mm$^2$

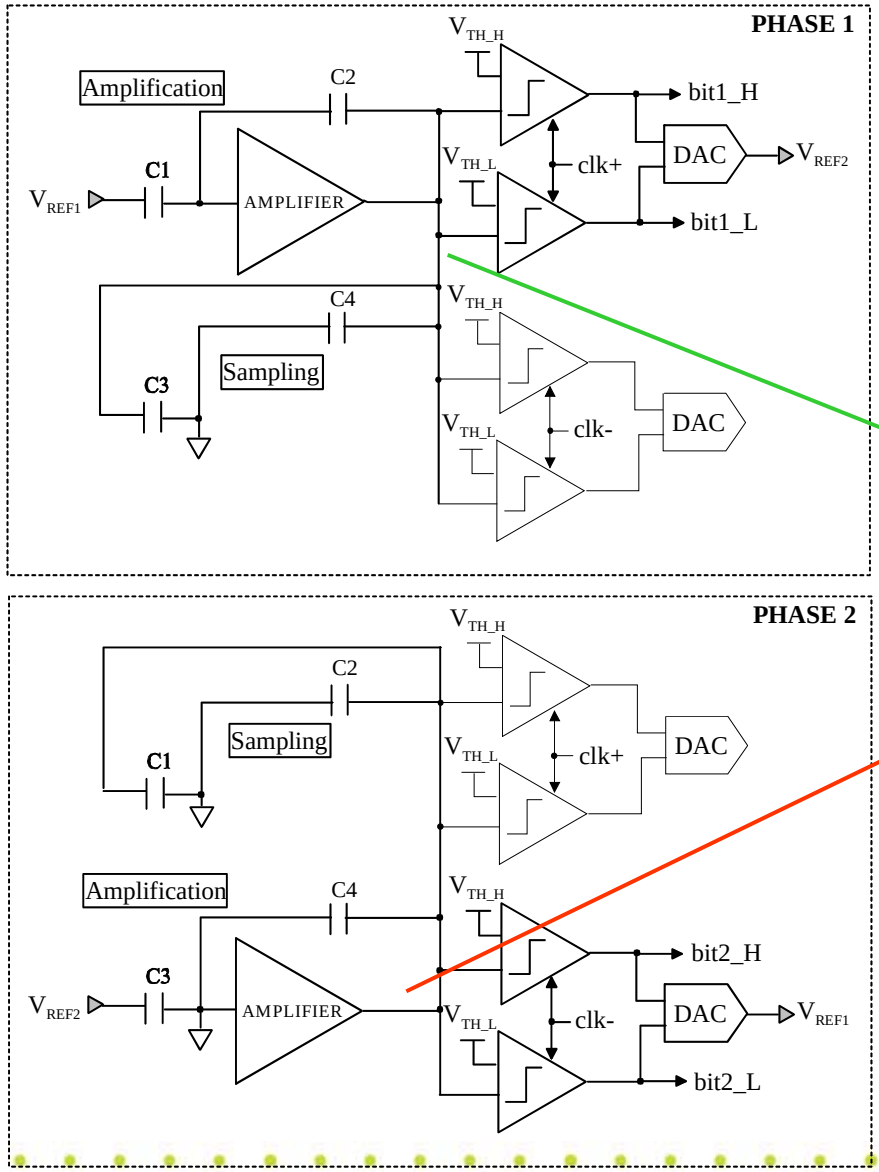
| | Optimized Cyclic | Pipeline |
|---|---|---|
| Resolution | 12 bits | 12 bits |
| Time for one conversion | ~~12~~ **7** clock periods | 1 clock period(1) |
| Power consumption | ~~1~~ **≈ 1.1** | 12 down to ≈ 6(2) |
| Integrated power | ~~12~~ **≈ 7.7** | 12 down to ≈ 6(2) |
| Area | ~~1~~ **≈ 1.5** | 12 down to ≈ 10(3) |

2 conversion phases with a single ampli.

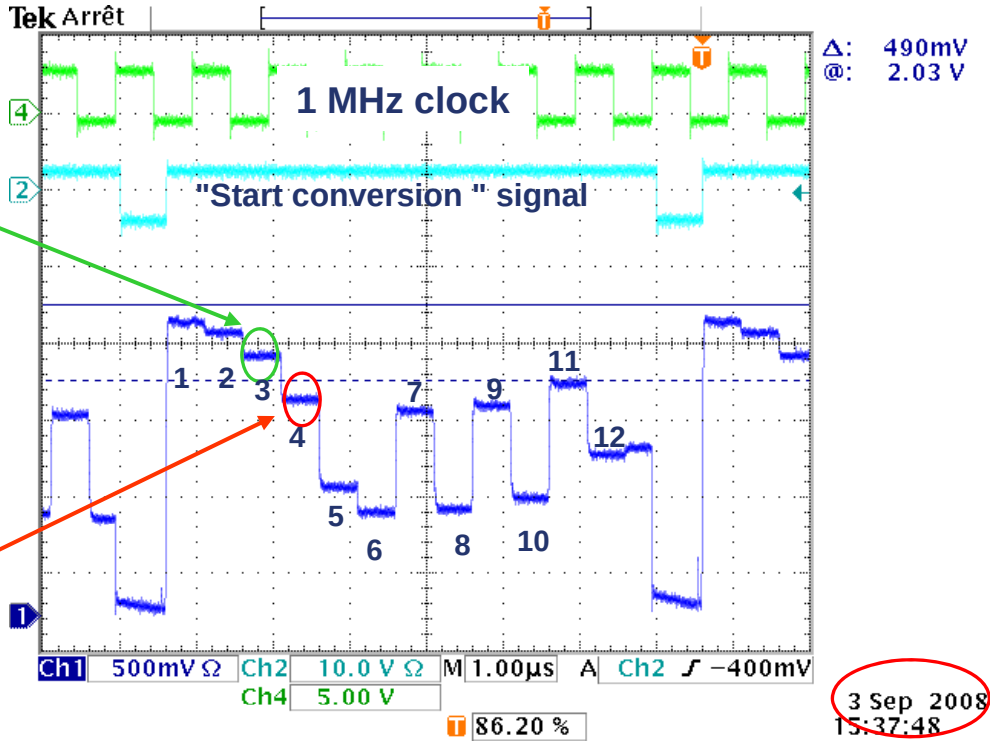


# Very First results of measurement




**Oscillogram of the chip under test**



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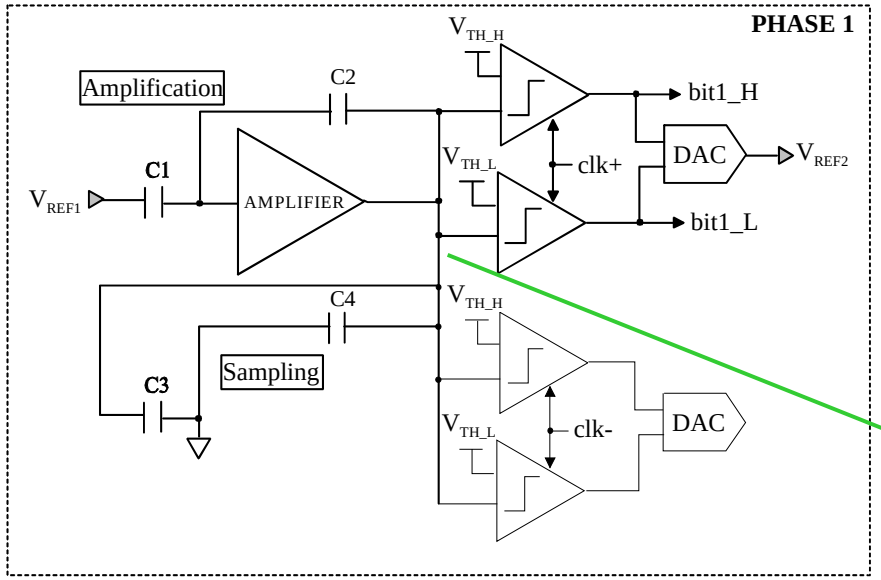


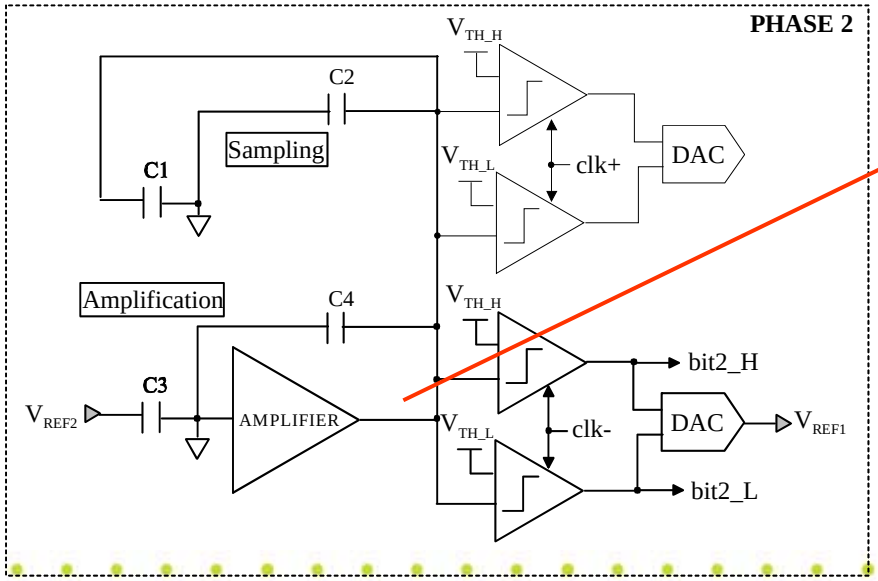


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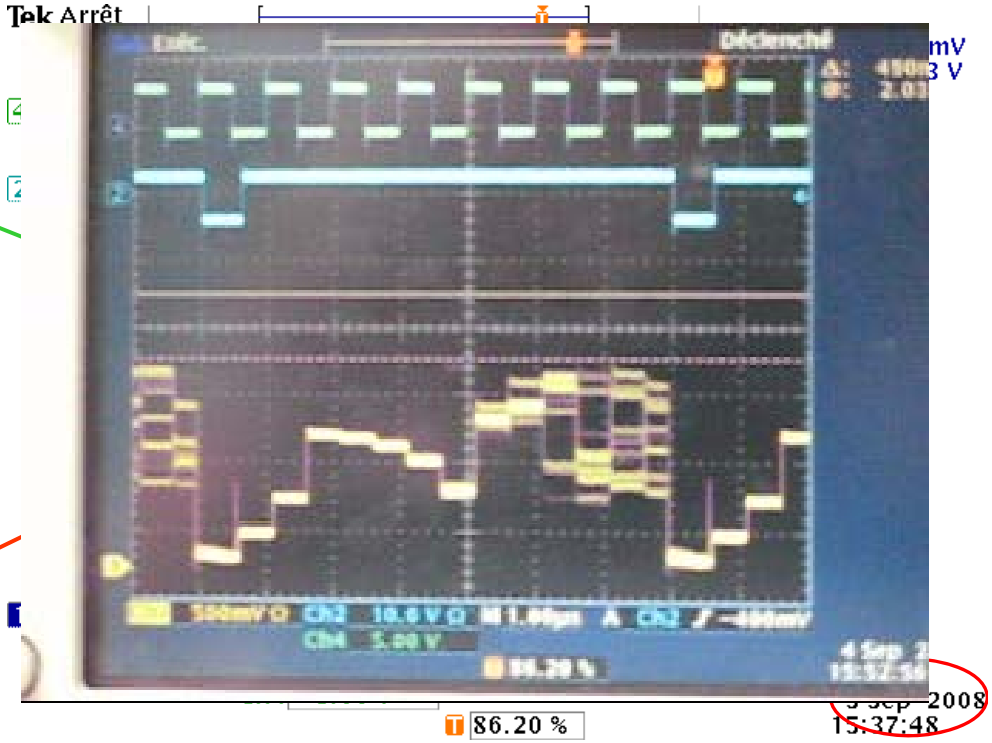
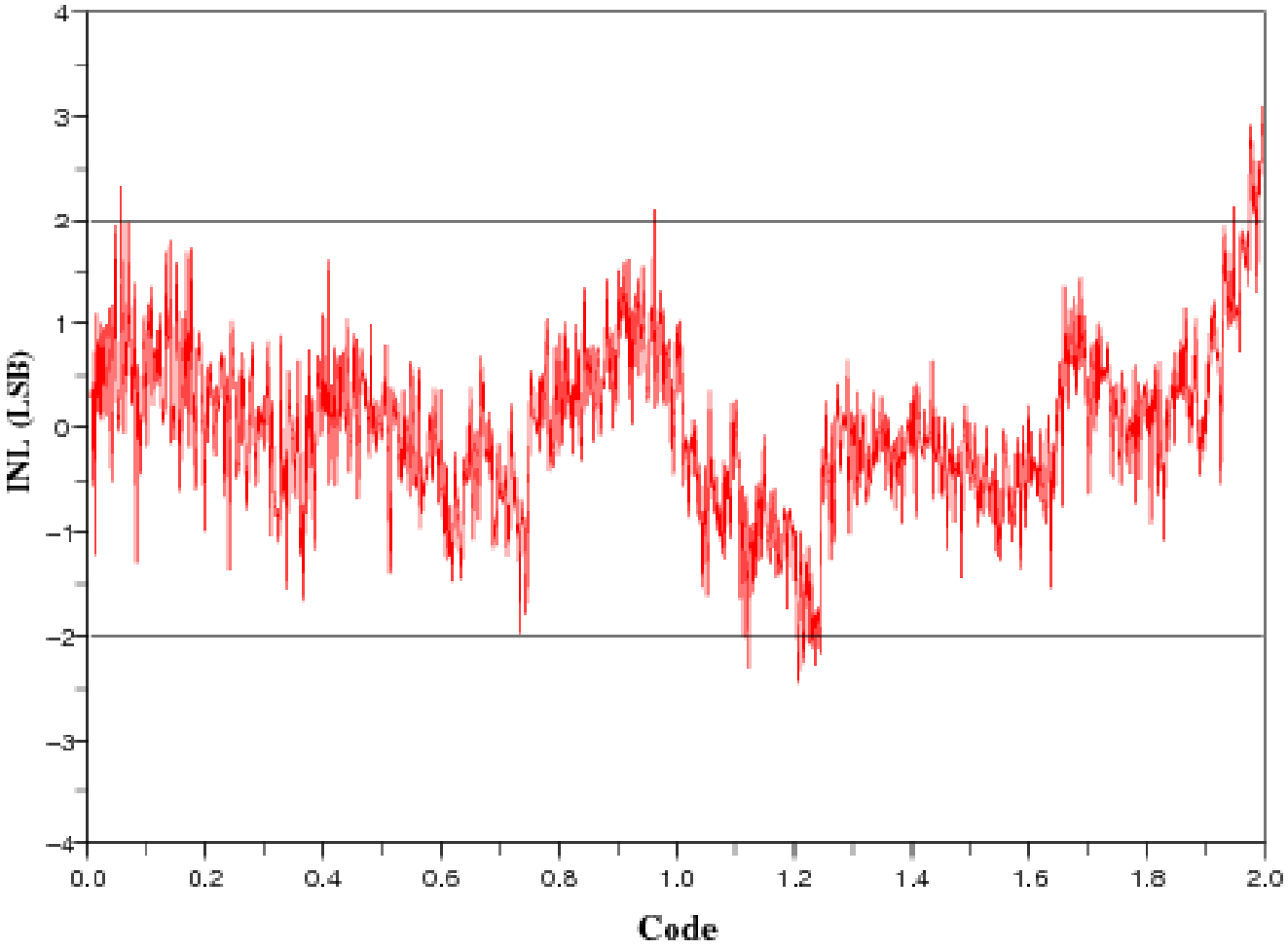
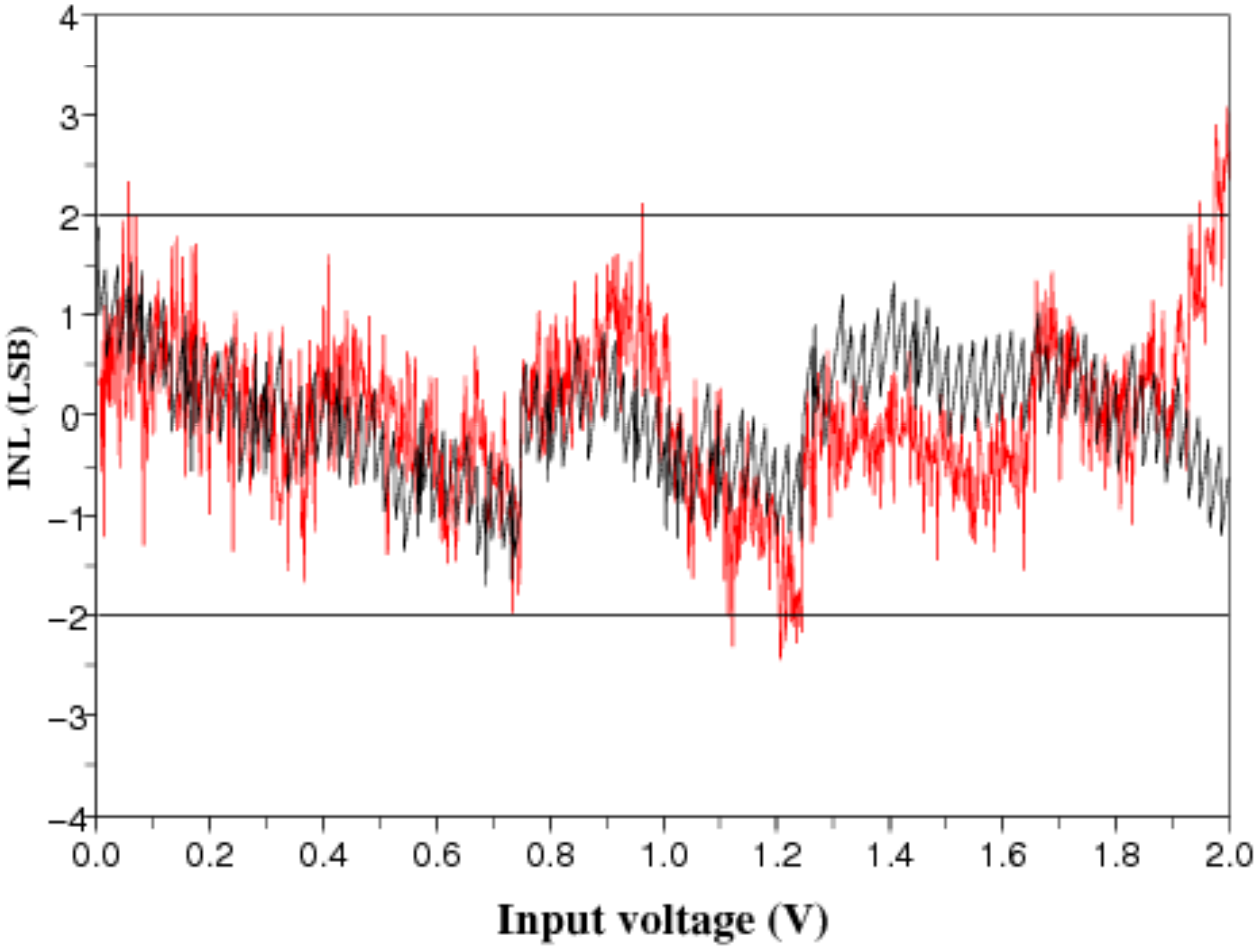


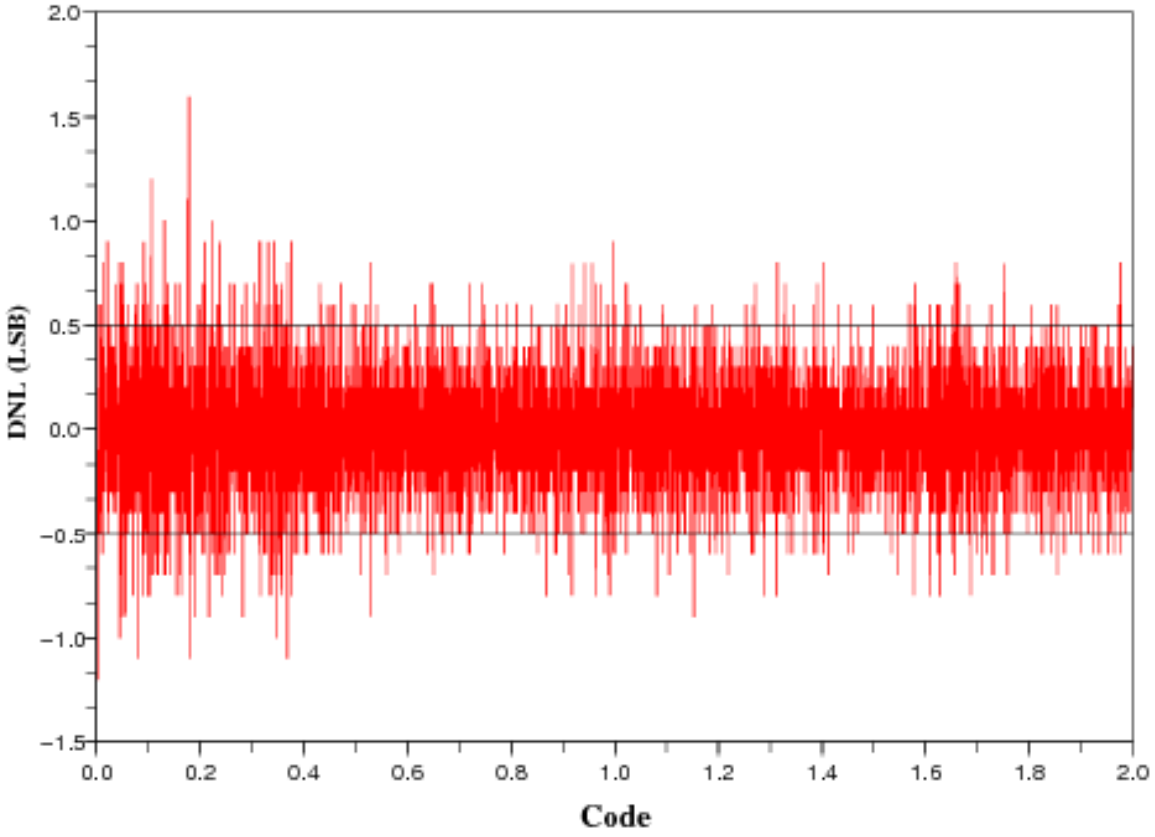
# Measured Integral Non-Linearity (INL)



# Both simulated and measured INL

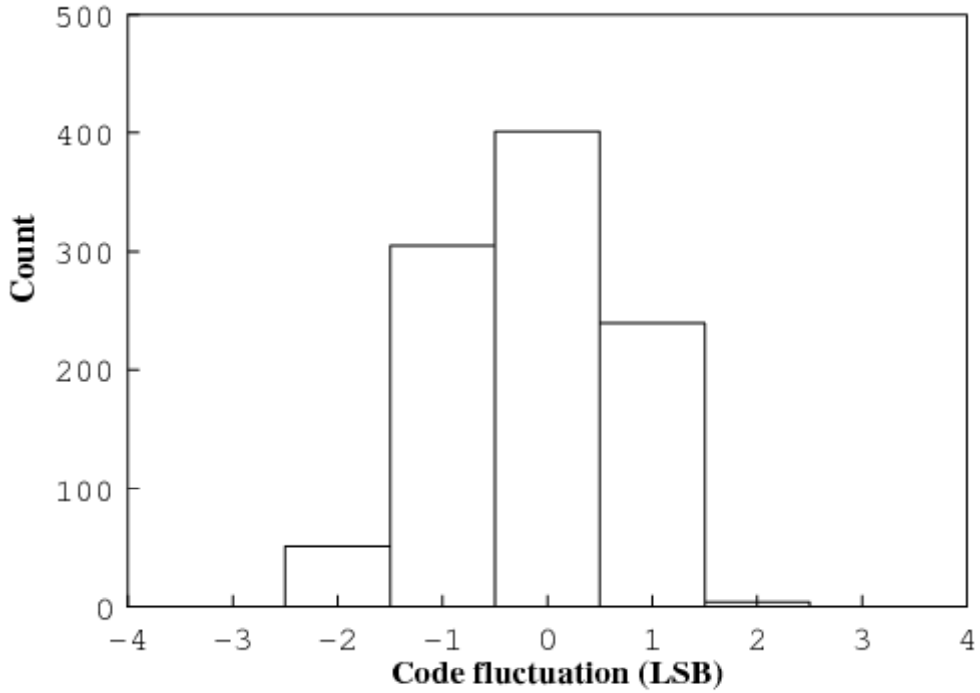


# Measured Differential Non-Linearity (DNL)



# Noise measurement

## Code fluctuation @ 1V




## Standard deviation = 0.84 LSB (420µV)

# Conclusion

- A 12-bit cyclic ADC prototype, dedicated to Calice, is fabricated and under test
- First measured performance is in accordance with simulations (speed, resolution, power cons., noise)
- Next measurements have to evaluate:
  - Dispersion of the performance on the 10 chips produced
  - Dependence of performance with clock frequency
  - Performance of the Power pulsing (recovery time of the biasing)

Results will be presented during the next IEEE meeting in Dresden

# One ADC per *n* channel