DAQ and Electronics

presented by

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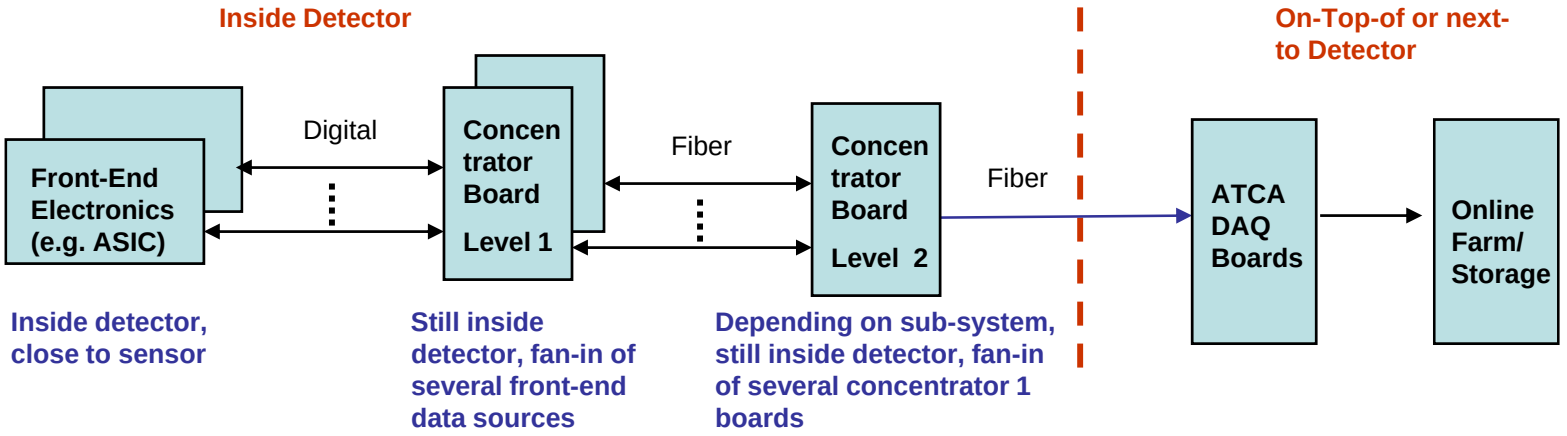
Overview

- Electronics Architecture
- Example front-end electronics options
  - ECAL
  - KPIX7 Status
  - GEM
  - TKR
  - BeamCal
  - Muon (see Henry's talk)
- DAQ
- LOI preparation

Overall Electronics/DAQ Architecture



- Total data rate from each front-end relatively small, thus can combine data from several front-ends to reduce number of connections to the outside of the detector
- Front-End ASICs/electronics transmit event data to concentrator 1 boards
  - Digital interface (optical or electrical, e.g. LVDS)
  - Concentrator 1 boards close to front-end, combining data-streams from several front-end ASICs
  - Zero-suppression either at front-end or on concentrator 1 boards
    - No additional processing needed at this stage
- Event data from concentrator 1 boards are combined in concentrator 2 boards
  - Multiplexing of concentrator 1 board event data onto fewer fibers
- Event data is transmitted to top or side of detector
  - ATCA crate (see later) to process and switch data packets
  - Online farm for filtering (if necessary)

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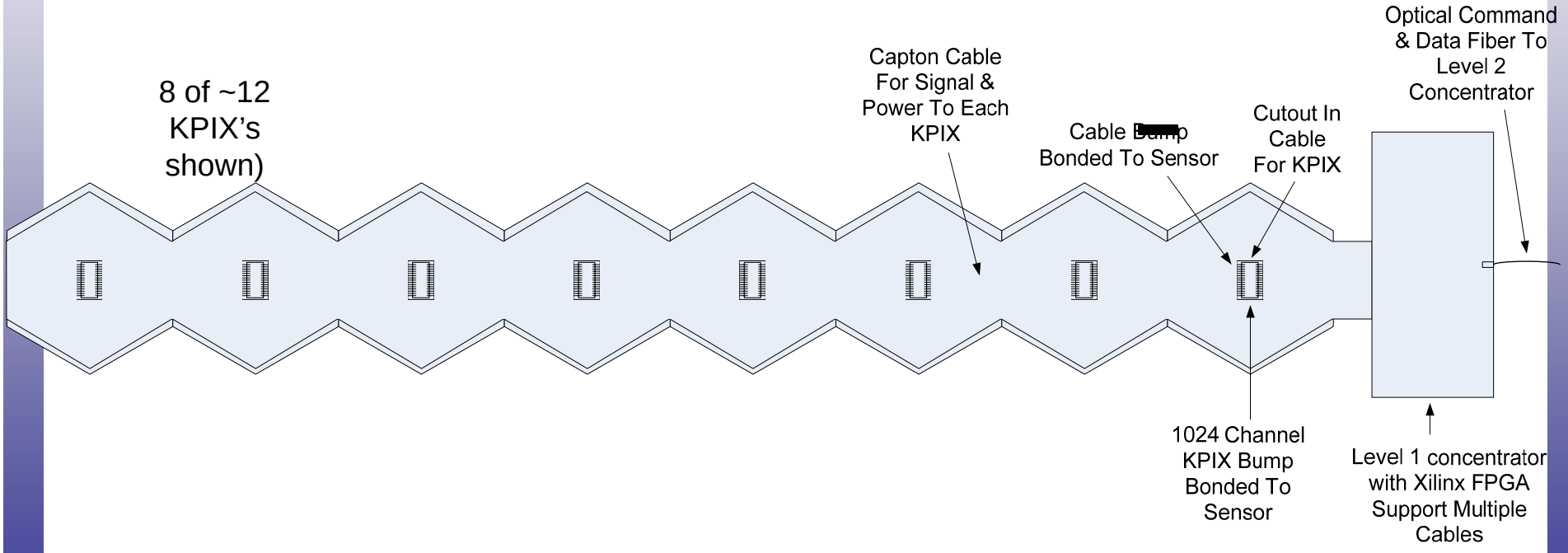
Front-End Electronics Option: SiD E-CAL

- ~ 12 KPIX bump-bonded to detectors mounted to a cable
- Cables routed to each end of the detector
- Concentrators at the ends of the cables combining data from several cables



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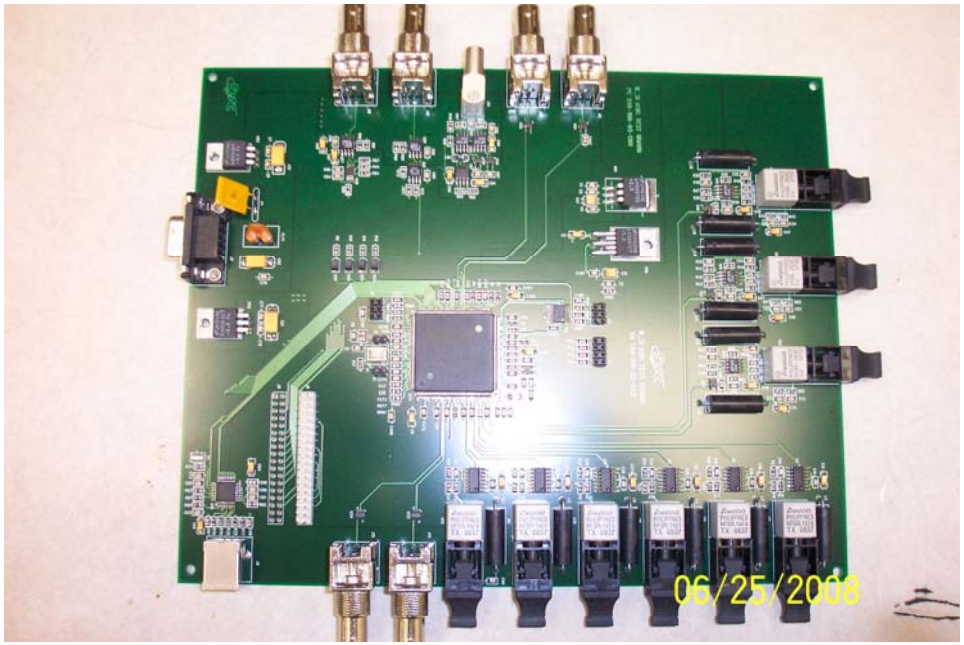
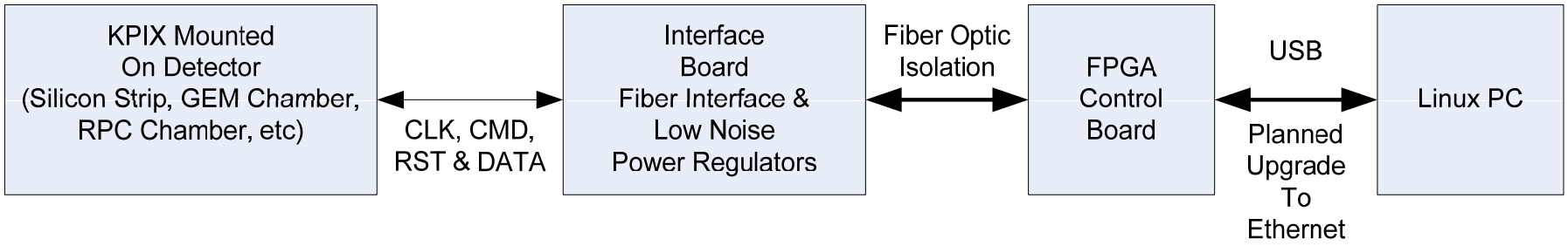
Test-Setup: KPIX Data Acquisition

- FPGA Control Board
  - USB Interface to PC
    - Ethernet IO being added
  - Interface To External Logic
    - Beam Line Triggers
    - Scintillators
    - Laser Triggers
- Optically Isolated To KPIX Interface Board
- C++ API Under Linux





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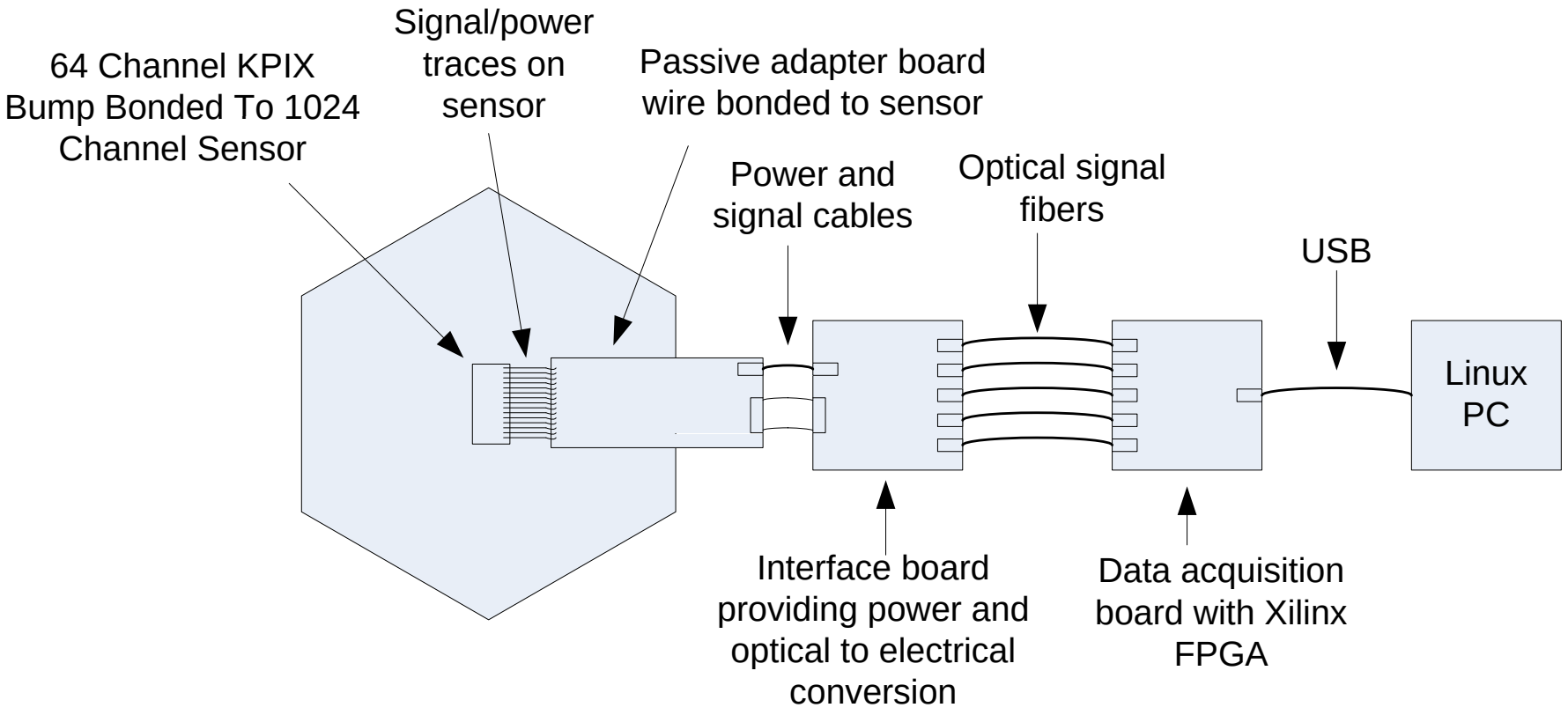
E-CAL Testing



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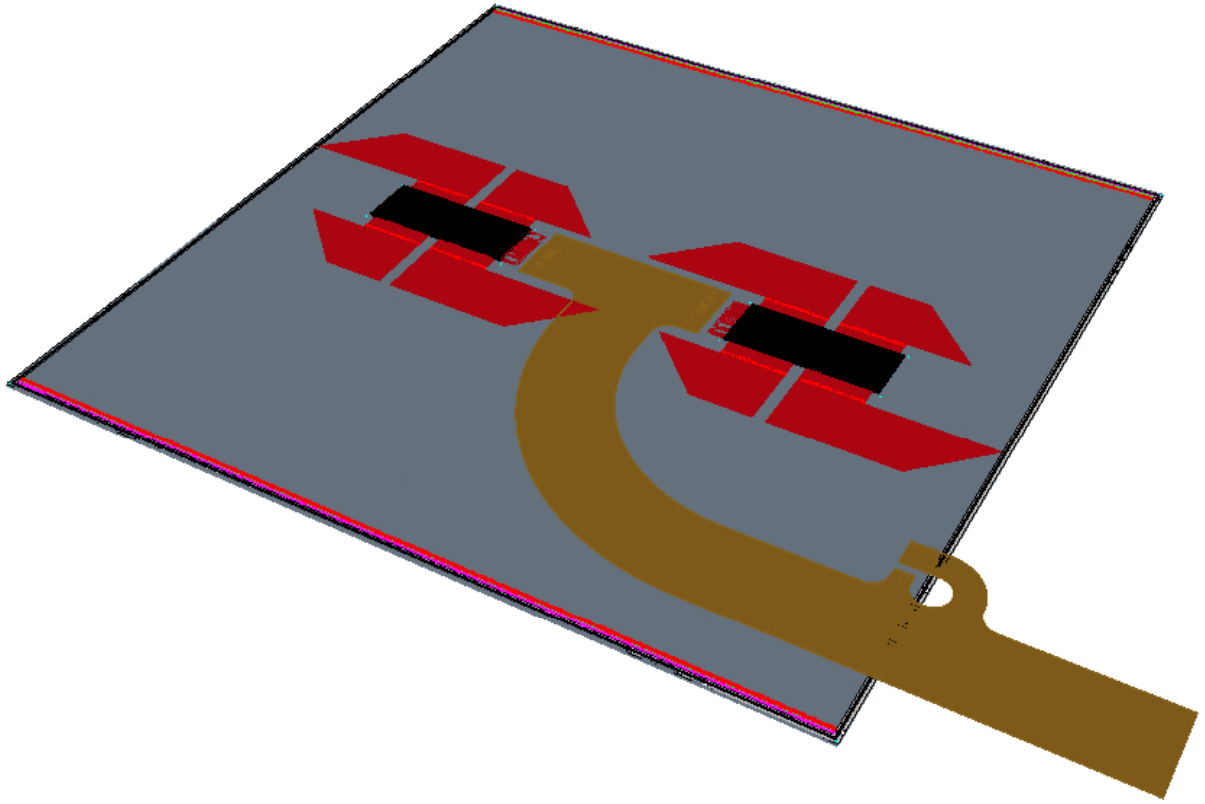
KPIX 7 Status

- Actively being used/tested
  - GEM Chamber Tests @ UTA
  - RPC Chamber Tests @ SLAC
  - Planned E-Cal detector tests @ SLAC & Oregon
  - Planned Tracker detector tests @ SLAC
- Improved routing of signal traces and power busses
  - Digital crosstalk in readout traces eliminated
  - Geographic influence on pixel performance eliminated
    - Gained confidence for moving to larger number of pixels
- DC reset feature added
  - Reduced ADC & Trigger noise by 50%
  - Improved operation in asynchronous environments such as cosmic ray & source testing.

Tracking: KPIX Front-End Electronics Option

- Similar to ECal: double metal power/readout of pair of KPiX ASICS
- Low noise is important for best position resolution: <1000 e^- for 20 pF load
- K*PiX*7 is close to this goal with discrete load
- Must test double-metal power and readout: many possible mechanisms for introducing additional noise.



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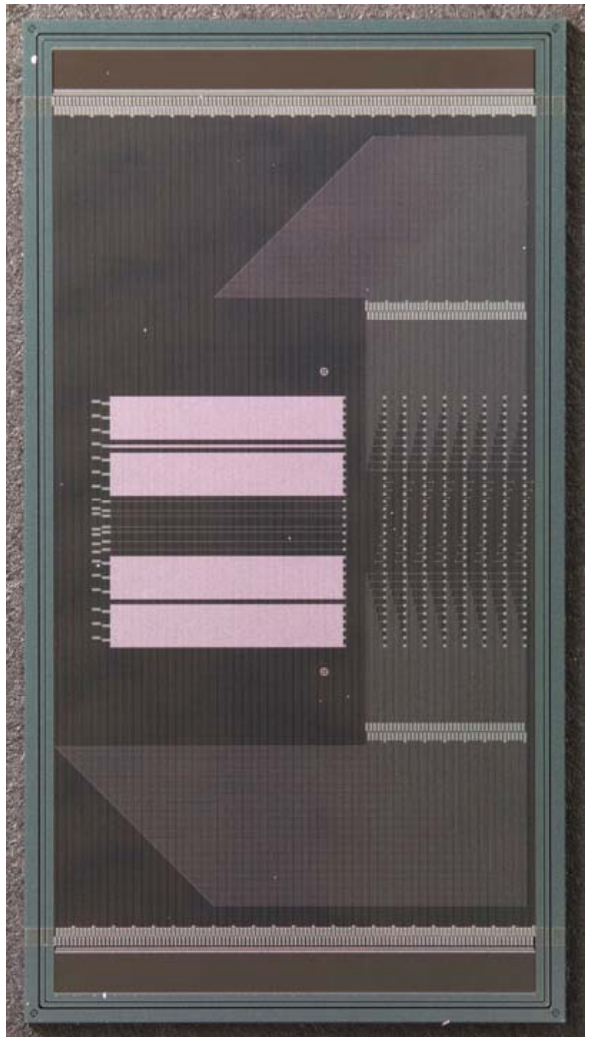
Prototype Sensors

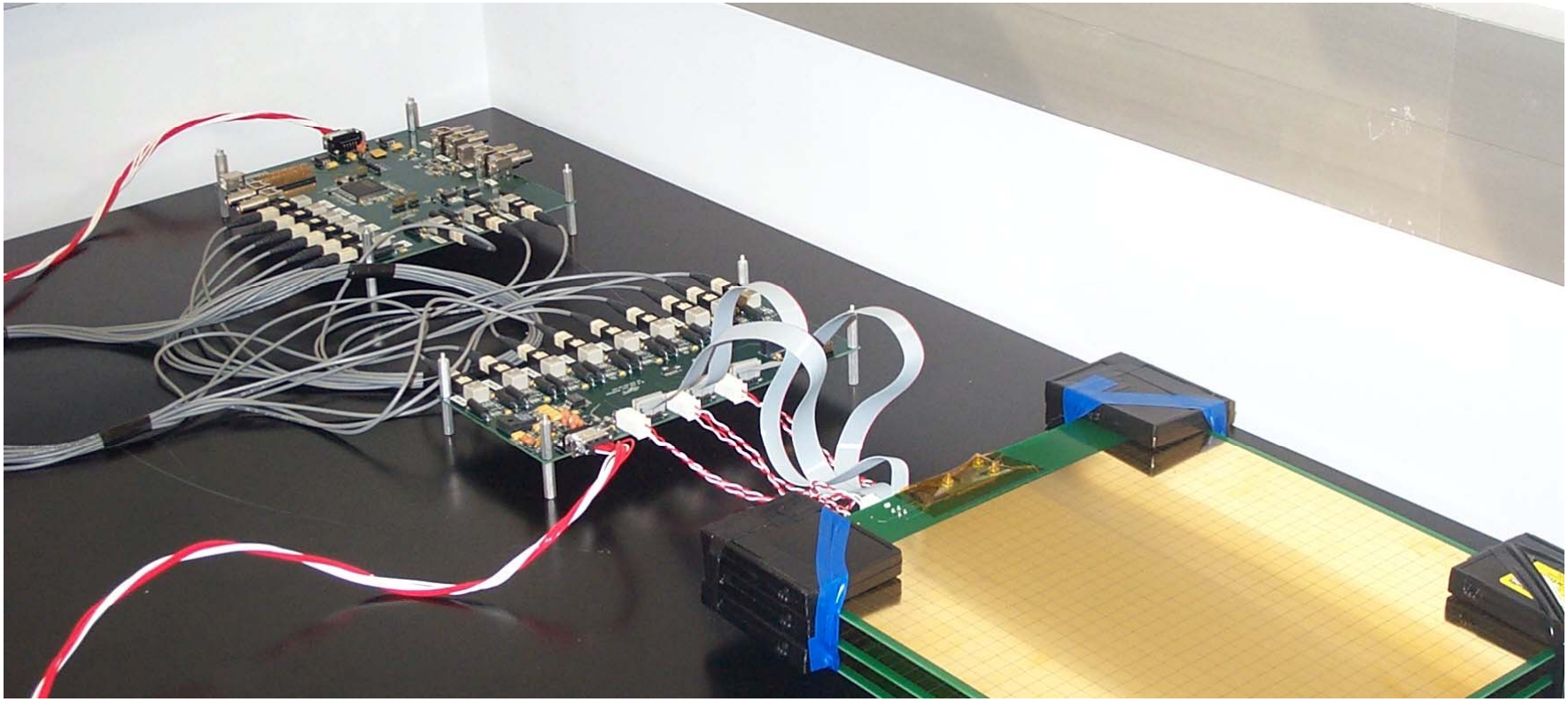
- Single-sided design with 1840 channels (2 K*PiX)* at 50(25)μm readout(sense) pitch
- 20 full-sized sensors from HPK
- Quality is excellent:
  bad channel rate <1/10000
- Testing is underway at UCSC:
  I-V, C-V, trace resistances, etc.
- Requires full-sized K*PiX* to instrument strips underneath power/readout traces

K*PiX* Test Sensors

- HPK submission included 40 smaller sensors for testing double-metal readout with smaller K*PiX* variants.
- Sense strips under power/readout traces are instrumented for 64-256 channel K*PiX* chips
- Sending sensors to UC Davis/Palomar Technologies for bump bonding to K*PiX*
- Plan laser, source and beam testing of these parts to provide proof-of-principle for double-metal readout required in SiD tracker and ECal designs.



GEM-DHCAL KPiX boards with Interface and FPGA boards



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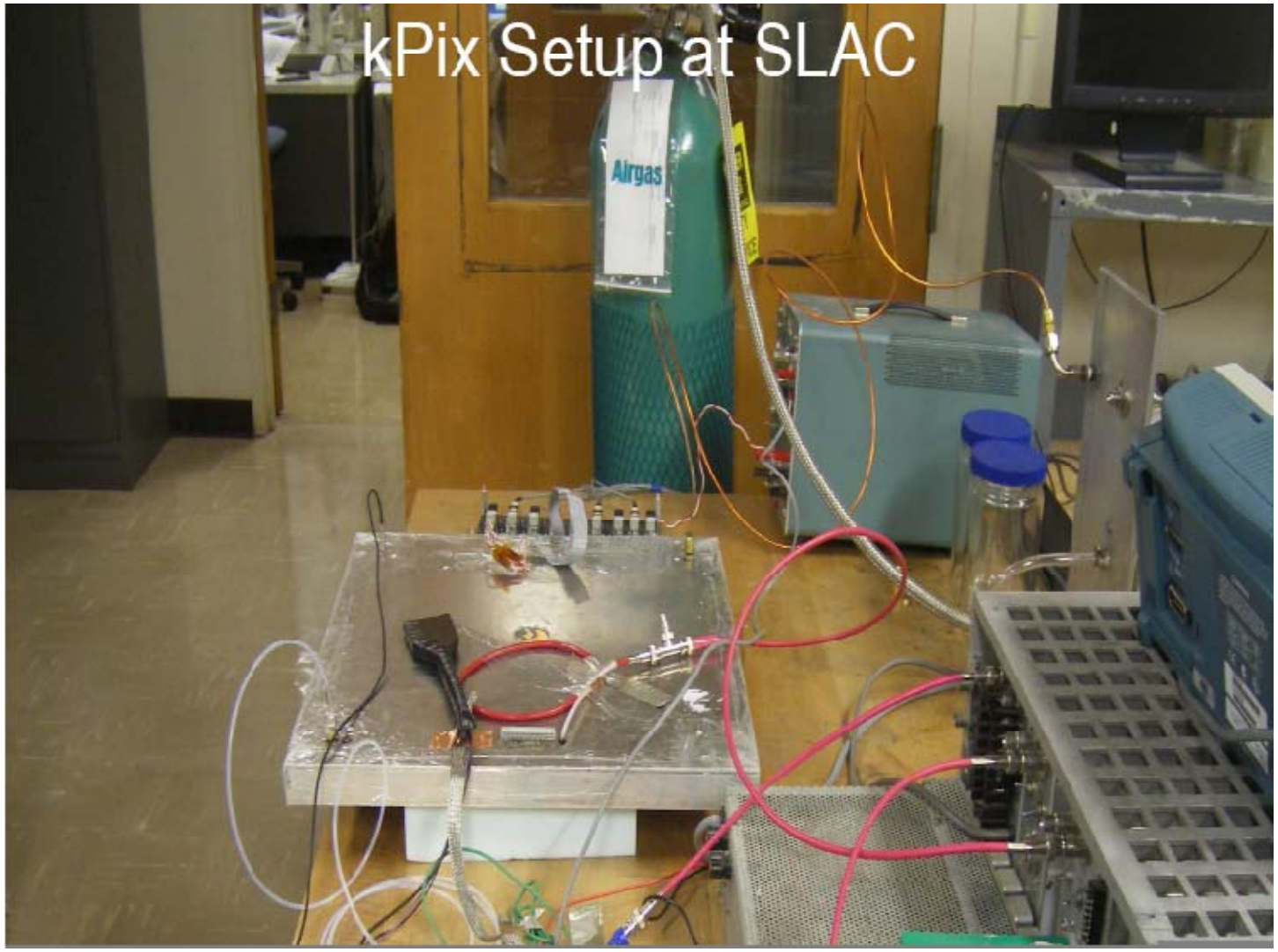
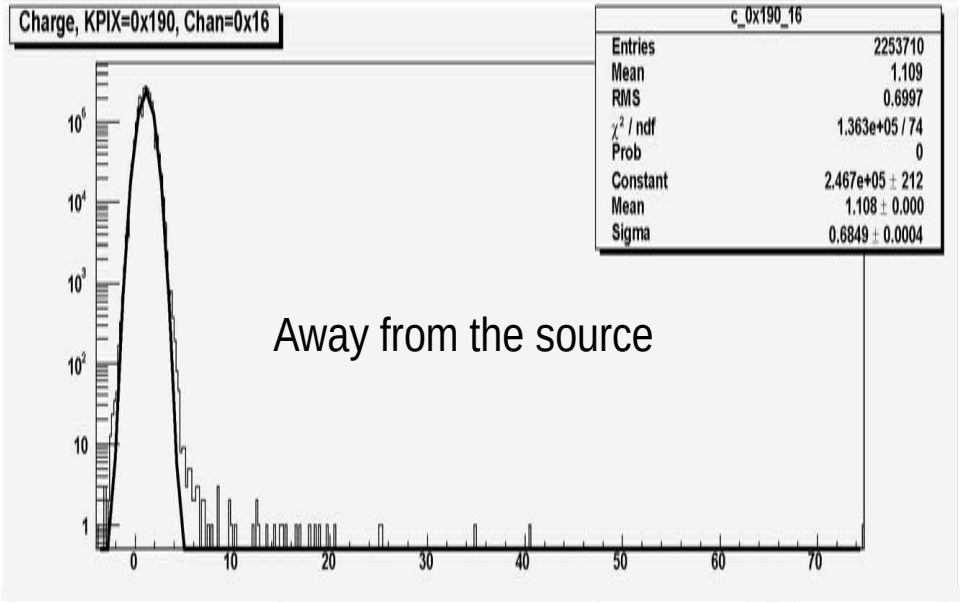
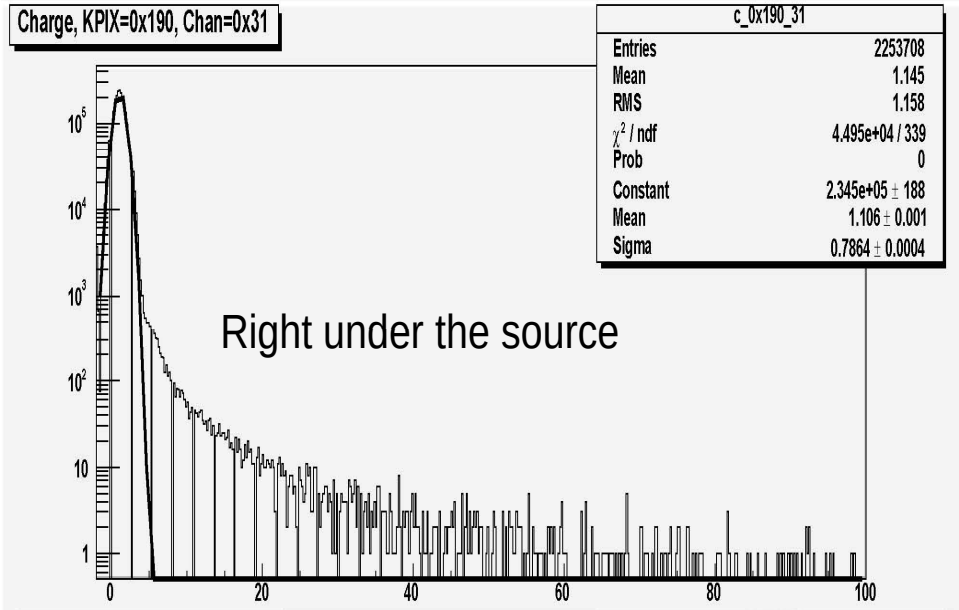
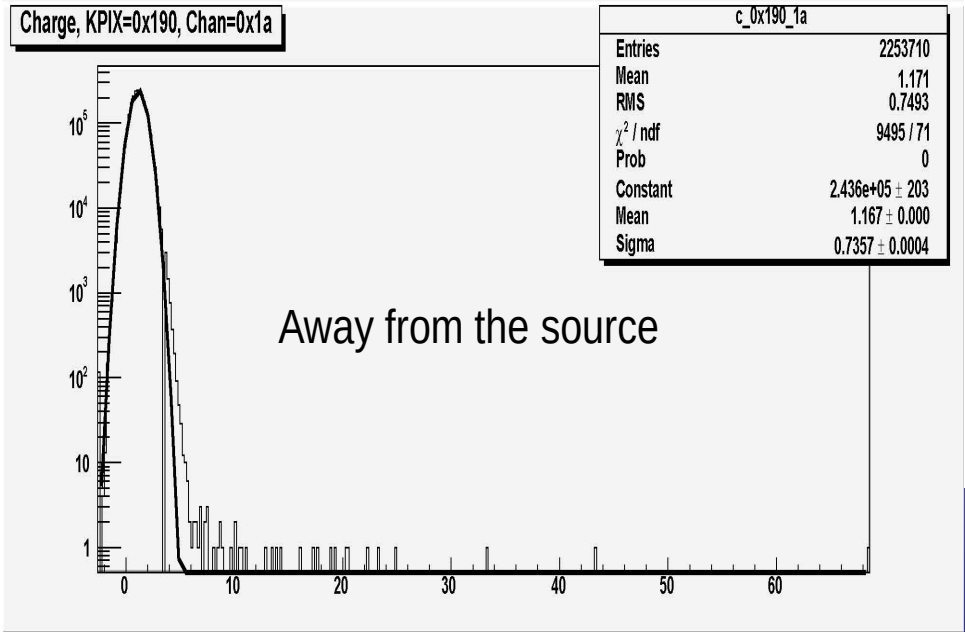
GEM chamber with KPiX v4 – early 2008

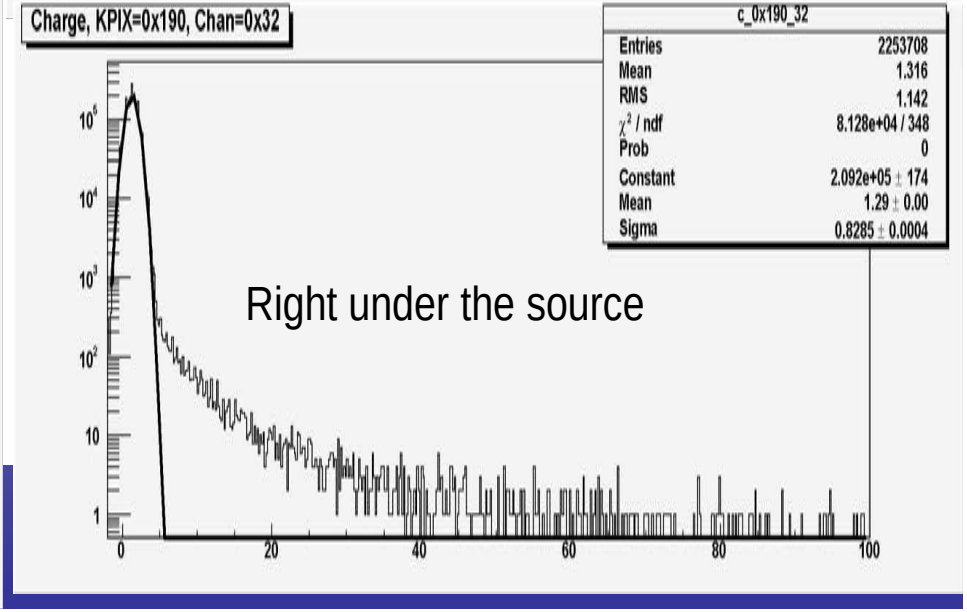


GEM + KPiX response in lab at SLAC







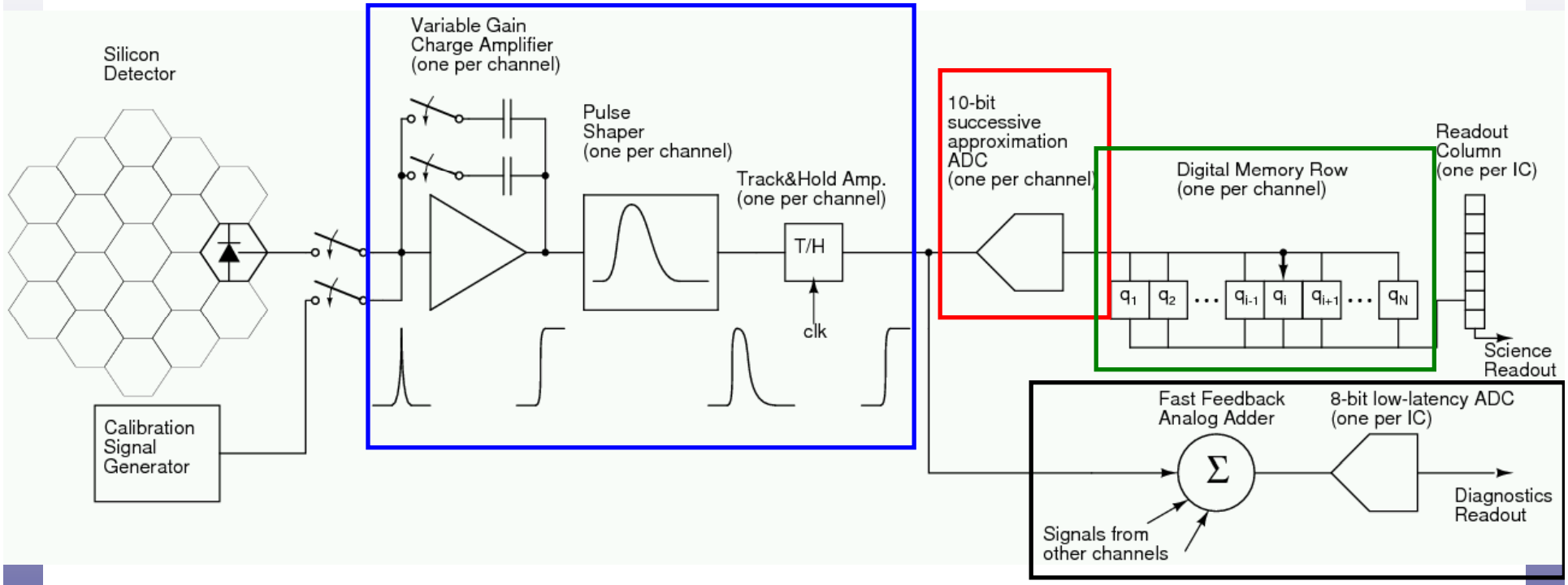


FCAL: BeamCal Electronics Specs and Challenges

- High input rate (3.25 MHz)
- High occupancy (100%)
- Large input signals (~40pC)
- Large input capacitance (~40pF detector + wires)
- High resolution (10 bits)
- Dual gain (50x) for different modes of operation
- Low latency (~1us) output for beam diagnostics
- High radiation (1Mrad total dose)

- Integrated circuit in design at SLAC (Angel Abusleme)

BeamCal ASIC: Simplified Block Diagram (only one channel shown)



- Dual-gain front-end electronics: charge amplifier, pulse shaper and T/H circuit
- Successive approximation ADC, one per channel
- Digital memory, 2820 (10 bits + parity) words per channel
- Analog addition of 32 channel outputs for fast feedback; low-latency ADC

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BeamCal Electronics: Techniques and Solutions

- g_m/I_D technique for precise analysis
- Time-variant filtering
- Differential circuitry
- Time budget (308ns per event) sparingly used, quasi-triangular weighting function:
  - Switched capacitor filter for pulse shaper
  - Slow reset
- Digital memory
  - No leakage
  - More choices against single-event effects
  - High density in 0.18-um TSMC
- Front-end precharge to take advantage of output swing

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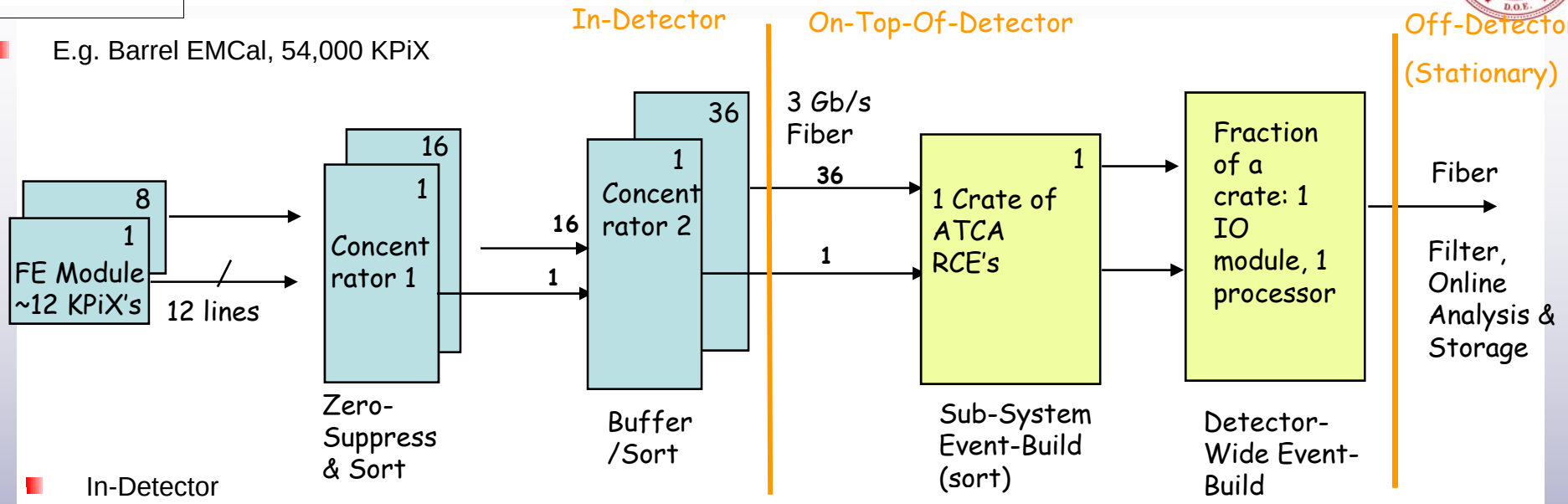
DAQ: EM Barrel Example

- E.g. Barrel EMCal, 54,000 KPiX



- In-Detector
  - KPiX Readout via two levels of concentrator boards (FPGA-based, reconfigurable)
  - L1 concentrator: zero-suppress. Sort total 20 hits/train/Kpix -> 20 hits * (2 words of 14 bits + 26 bit total system address) * 1 KHz * 96 KPIX;s = 12 Mbytes/sec
  - To L2 concentrator:
    - Out of L2 concentrator: 12 Mbytes/sec * 16 = 192 Mbytes/sec
  - Readout to On-Top-Of-Detector crates via 3 Gbit/s fibers
    - Only need 1 fiber, assume 2
- On-Top-Of-Detector
  - Event-Builder for sub-system
- Off-Detector (Stationary)
  - Filter, Online-Analysis, Storage

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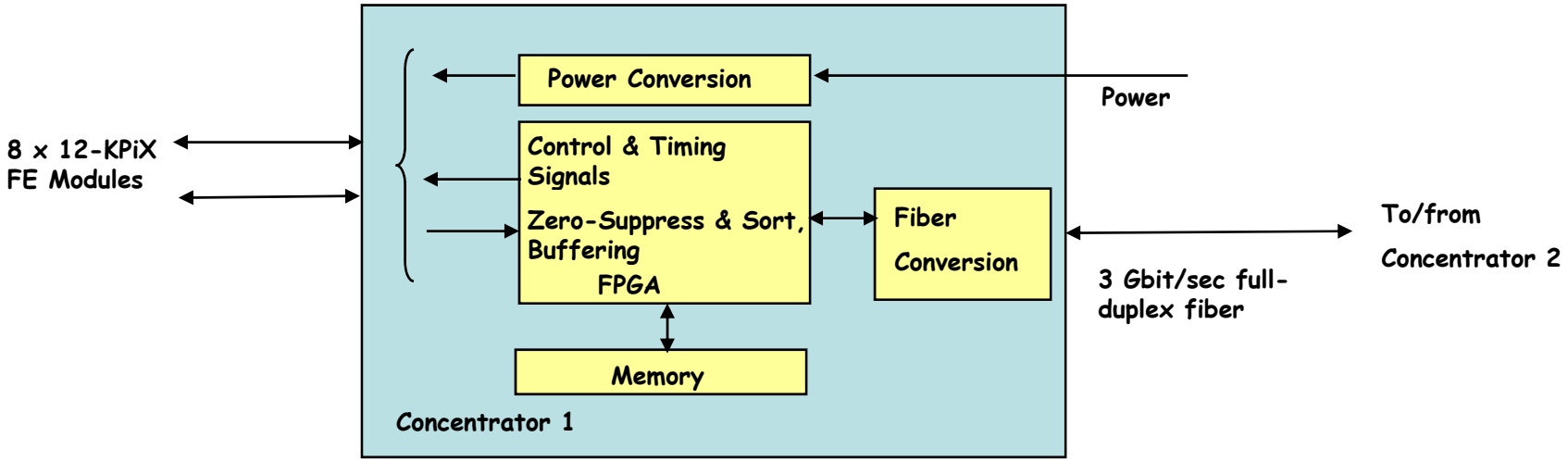
Concentrator-1



- Electrical interface to KPIX (or other front-end electronics)
- Buffer, Sort, Zero-Suppress (if needed) function
- Fiber connection to DAQ, standard SiD protocol

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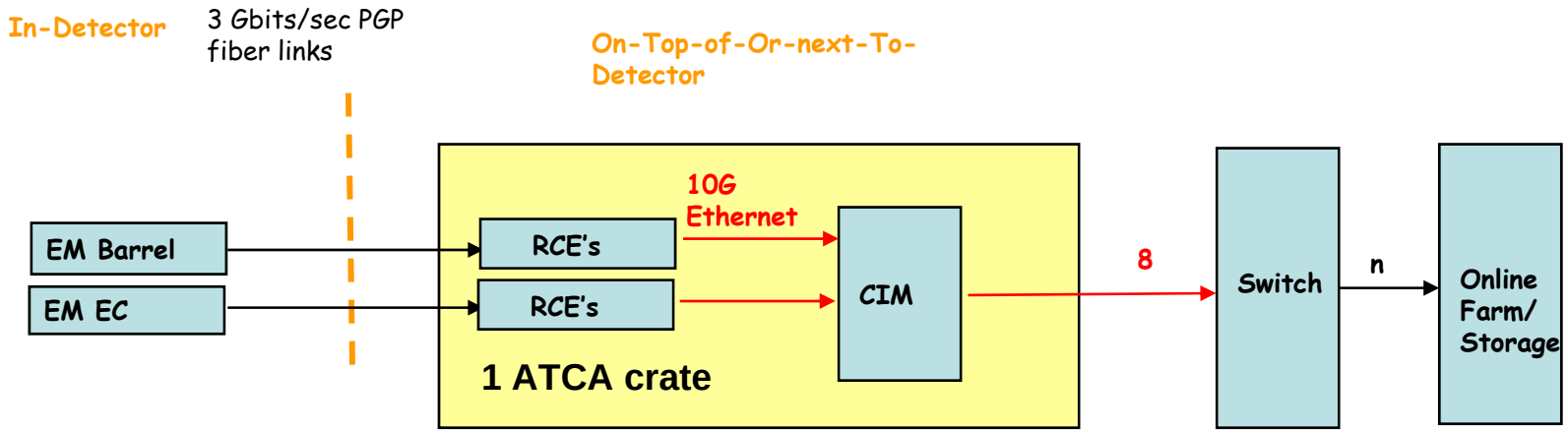
DAQ Architecture



- 1 ATCA crate for each sub-system for partitioning reasons
  - Two ATCA custom modules
    - RCE: Reconfigurable Cluster Element
    - CIM: Cluster Interconnect Module

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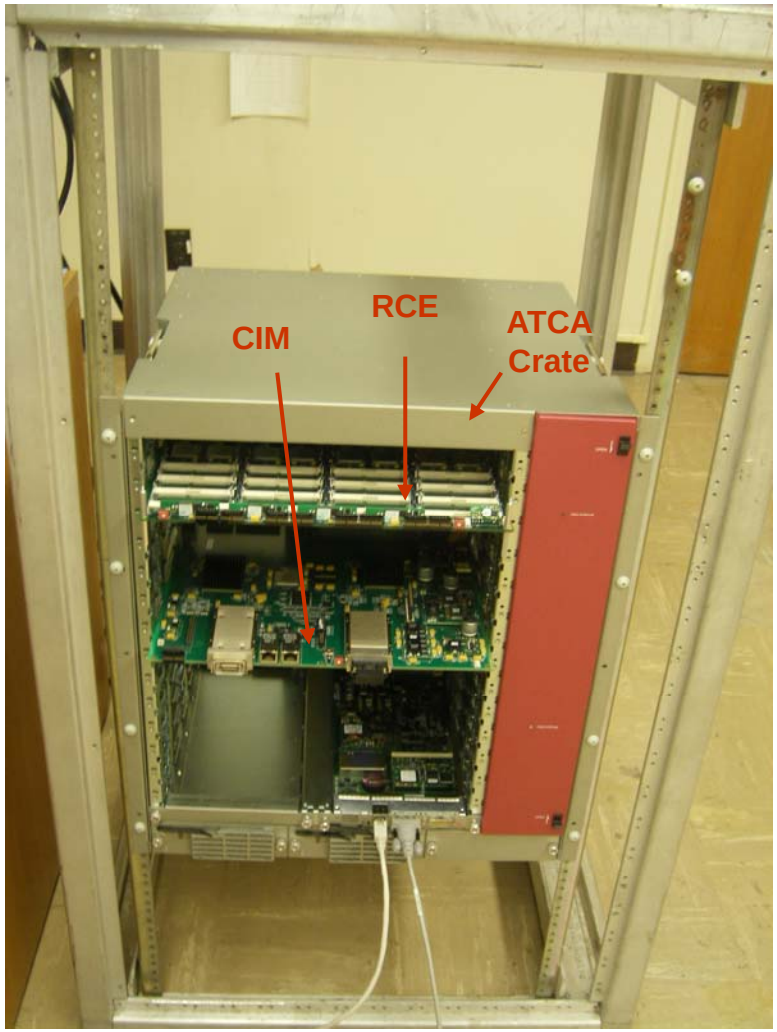
DAQ Sub-System

- Based on ATCA (Advanced Telecommunications Computing Architecture)
  - Next generation of “carrier grade” communication equipment
  - Driven by telecom industry
  - Incorporates latest trends in high speed interconnect, next generation processors and improved Reliability, Availability, and Serviceability (RAS)
  - Essentially instead of parallel bus backplanes, uses high-speed serial communication and advanced switch technology within and between modules, plus redundant power, etc

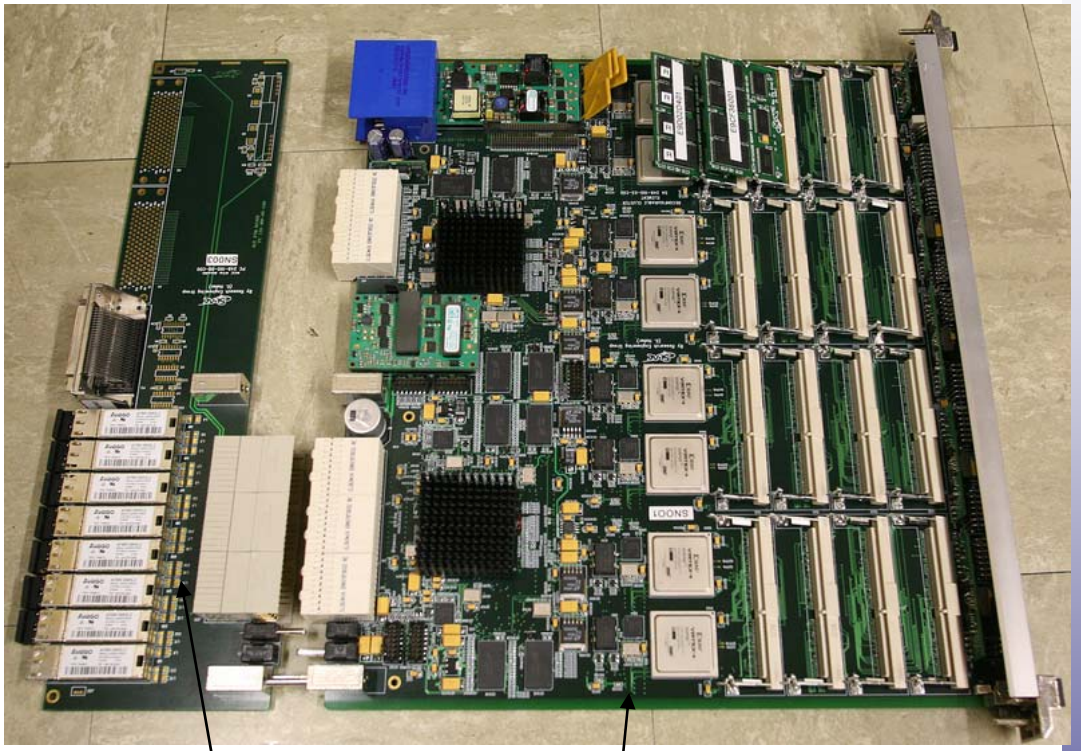
ATCA Crate

- ATCA used for e.g. SLAC LUSI (LCLS Ultra-fast Science Instruments) detector readout for Linac Coherent Light Source hard X-ray laser project
  - Based on 10-Gigabit Ethernet backplane serial communication fabric
- 2 custom boards
  - Reconfigurable Cluster Element (RCE) Module
    - Interface to detector
    - Up to 8 x 2.5 Gbit/sec links to detector modules
  - Cluster Interconnect Module (CIM)
    - Managed 24-port 10-G Ethernet switching
- One ATCA crate can hold up to 14 RCE's & 2 CIM's
  - Essentially 480 Gbit/sec switch capacity
  - SiD needs only ~ 320 Gbit/sec including factor of 4 margin
  - Plus would use more than one crate (partitioning)



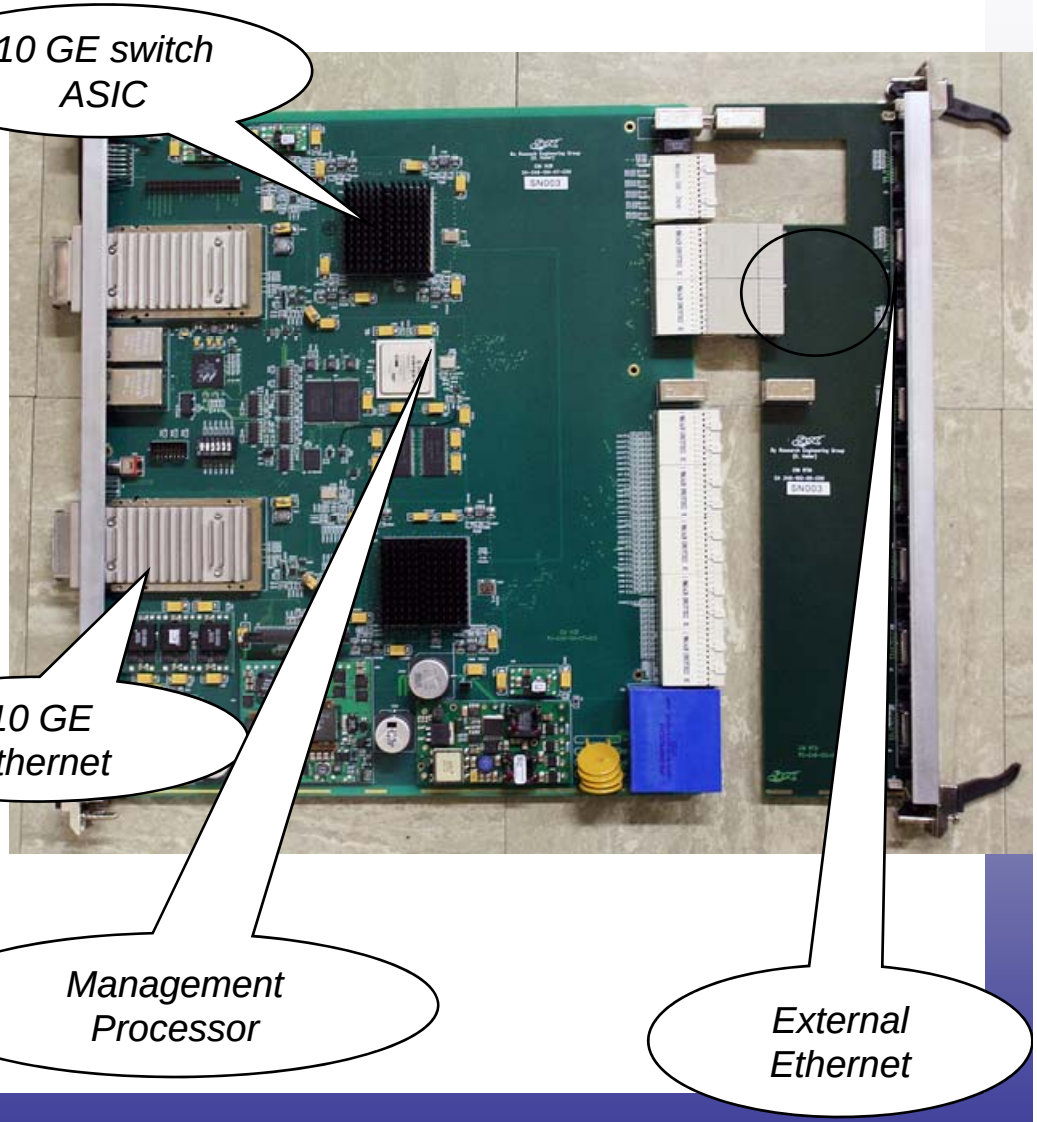
SLAC PPA Reconfigurable Cluster Element (RCE) Boards

- Used for LSST, Peta-Cache, LCLS DAQ
- Reconfigurable Cluster Element module with 2 each of following
  - Virtex-4 FPGA
    - 2 PowerPC processors IP cores
  - 512 Mbyte low-latency RLDRAM
  - 8 Gbytes/sec cpu-data memory interface
  - 10-G Ethernet event data interface
  - 1-G Ethernet control interface
  - RTEMS operating system
  - up to 512 Gbyte of FLASH memory
    - 1 TByte/board



SLAC PPA Cluster Interconnect board

- Network card
  - 2 x 24-port 10-G Ethernet Fulcrum switch ASICs
  - Managed via Virtex-4 FPGA
- Network card interconnects up to 14 in-crate RCE boards
  - Serves up to 28 detector-specific front-end cards
  - Up to 480 Gbit/sec transfer
- Network card interconnects multiple crates or farm machines
  - Additional scalability



LOI Preparation

- DAQ design being implemented for LCLS already higher performance than required for SiD
  - Good fit to SiD, can write-up as is for LOI
- Areas to be addressed
  - Data-management
    - Filtering
      - No filtering required in DAQ, large margin in throughput, scalable
      - Could move event data to online farm/off-line for further filtering/analysis
      - Still: investigate filtering in ATCA processors as well as in farm
    - Offline data systems (processing/archiving)
  - Needs volunteers

Main Contributors (not complete)

- ECAL
  - UC Oregon (David Strom, Ray Frey, Jim Brau, students)
  - UC Davis (Mani Tripathi, Britt Holbrook, Richard Lander)
  - SLAC (see below)
- Muon
  - U. of Wisconsin (Henry Band)
  - SLAC (see below)
- GEM
  - University Of Texas @ Arlington (Andy White, Jae Yu, Jacob Smith)
  - SLAC (see below)
- TKR
  - SLAC (Tim Nelson, Richard Partridge)
  - SLAC (see below)
- BeamCal
  - SLAC (Angel Abusleme)
- KPIX plus involved in above KPIX electronics systems
  - SLAC (Ryan Herbst, Dieter Freytag, Marty Breidenbach, Gunther Haller, Angelo Dragone)
  - UC Oregon (David Strom, Ray Frey)
  - BNL (Velco Radeka)
- DAQ
  - SLAC (Mike Huffer, Amedeo Perazzo, Matt Weaver, Chris O'Grady, Remi Machet, Ryan Herbst, Gunther Haller)