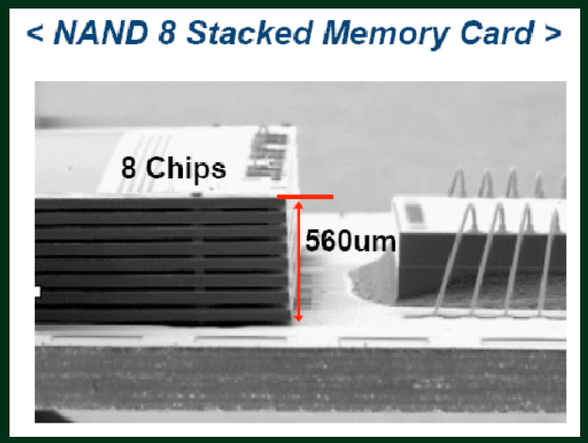
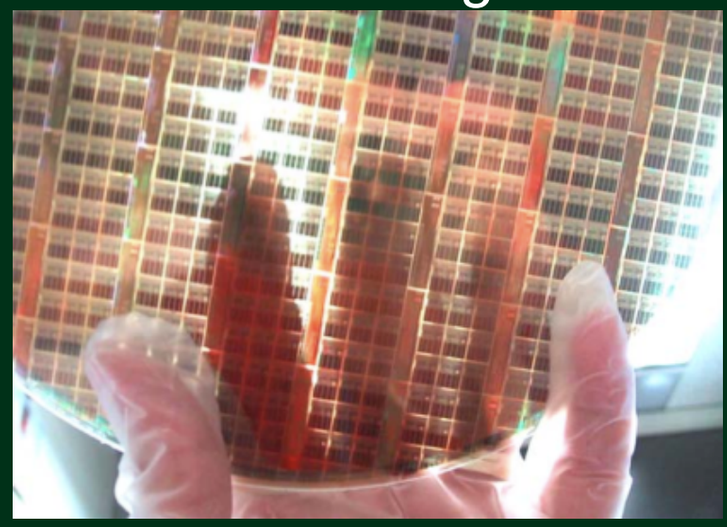
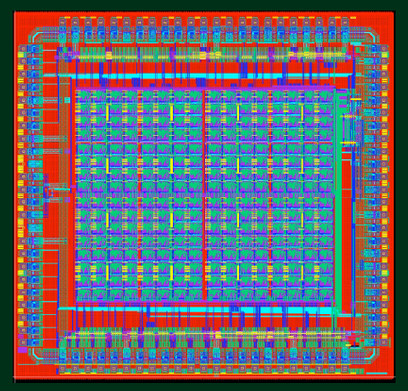
Status of 3D R&D at Fermilab

- 3DIC - vertical integration of electronics
- 3D IC technology is likely to become an important component of future electronics
  - Reduces length and R,C of interconnects
  - Allows for heterogeneous device integration
  - Improves processing density/pixel
  - Increases circuit density without billions of investment in new fab facilities
  - Multicore processors are at the memory access limit more bandwith is crucial to continue Moore's Law performance
- This is a opportunity for HEP to build detectors with significantly improved performance



Samsung


IBM SOI on Glass Wafer

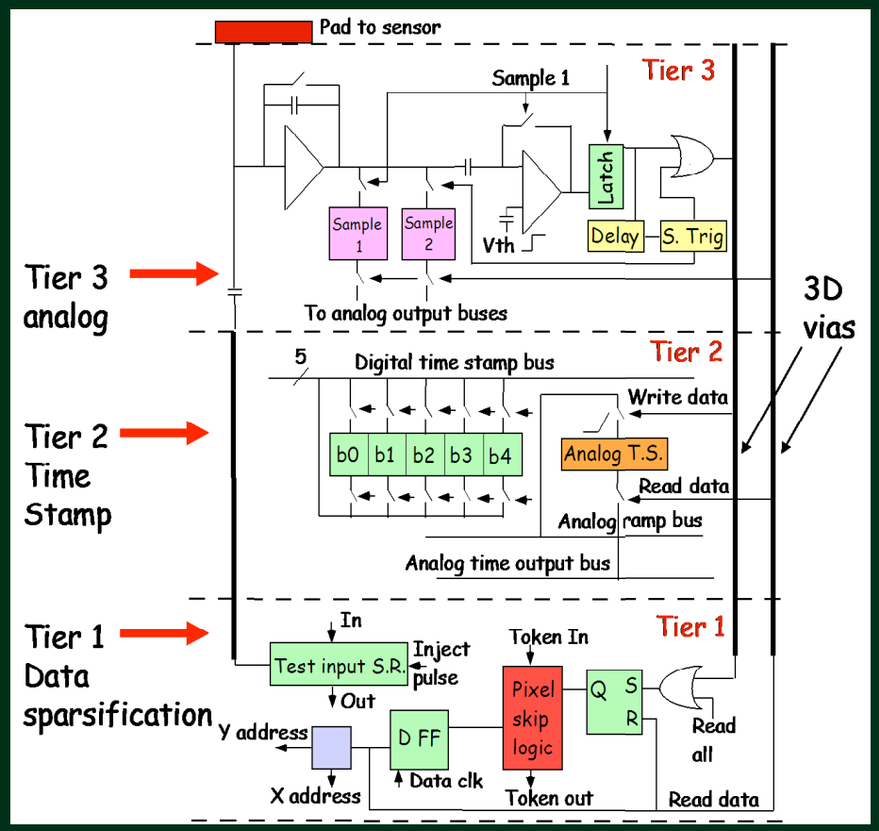

Tezzaron 3D FPGA

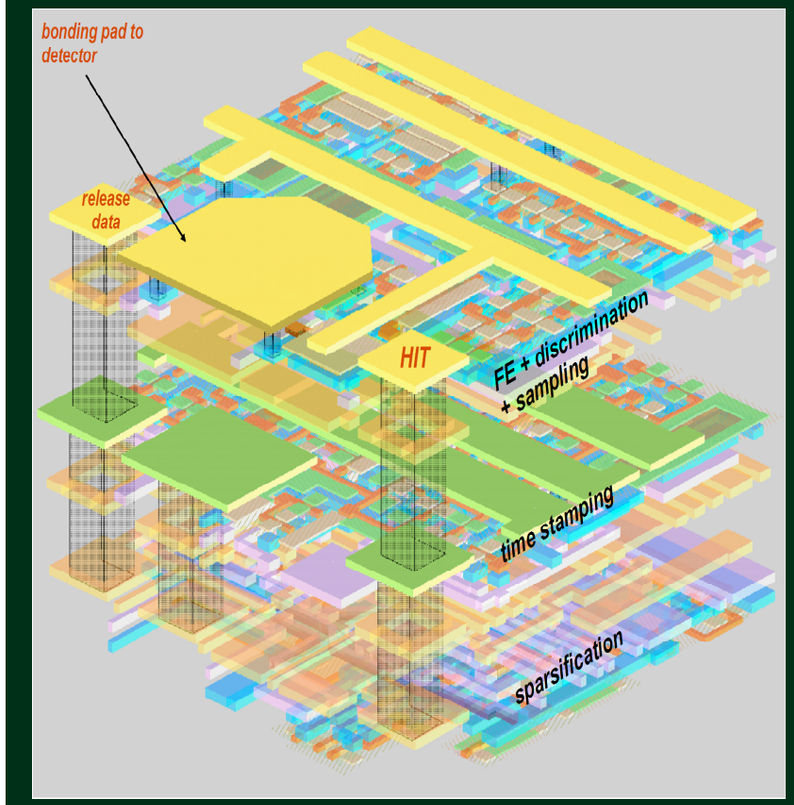
The VIP chip

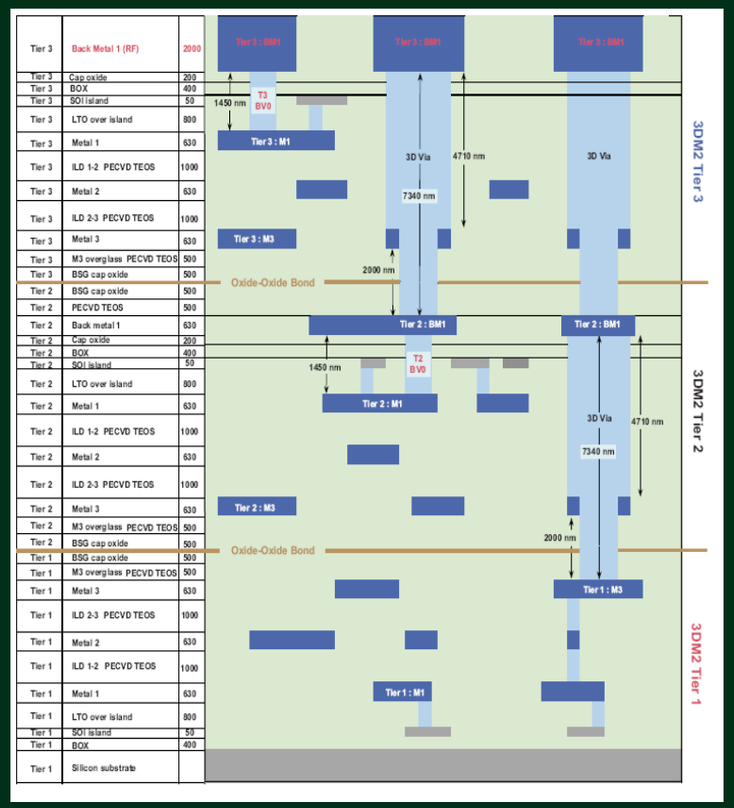
First 3D integrated circuit for HEP submitted by Fermilab to MIT Lincoln Labs October, 2006.

- **Three tiers of 0.18 micron CMOS 20 x 20 micron pixel**
- **5 bit time digital stamp, analog time stamp**
- **sparse readout**
- **low power, 500 na front end current**

Three levels of transistors, 11 levels of metal in a total vertical height of only 22 um.

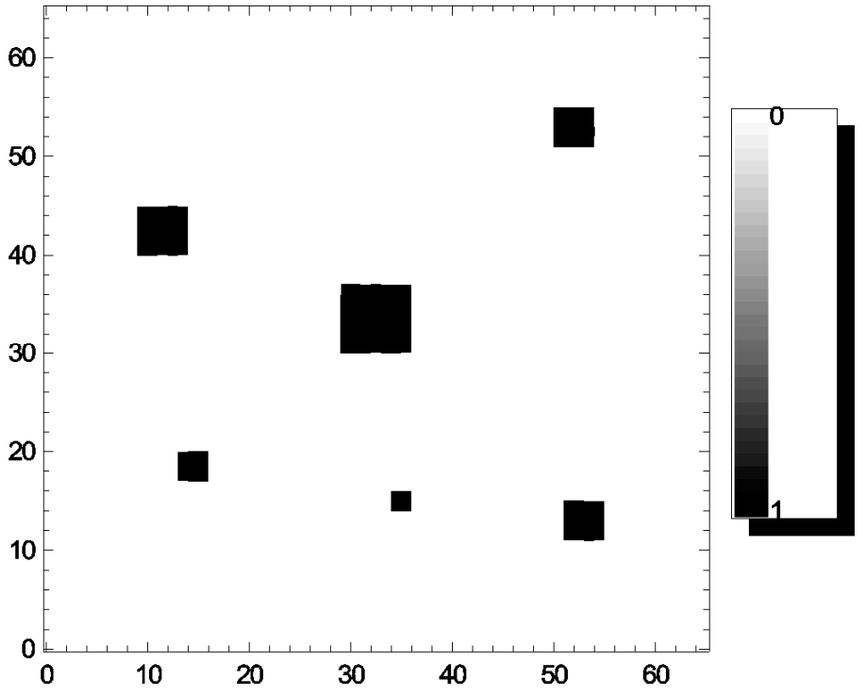




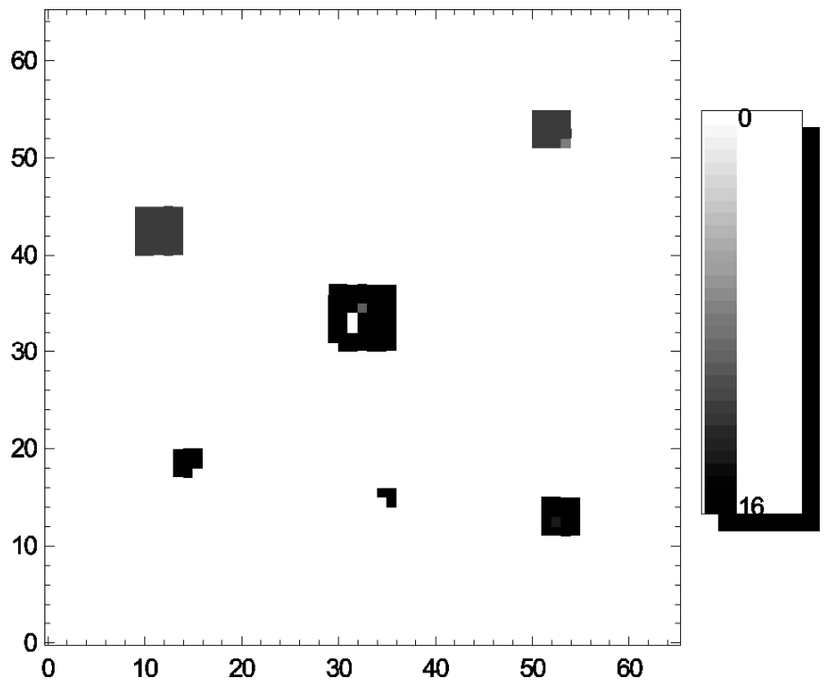


VIP Test results

- Basic functionality of chip has been demonstrated
  - Propagation of readout token
  - Threshold scan
  - Input test charge scan
  - Digital and analog time stamping
  - Full sparsified data readout
- Fixed pattern and temporal noise measurements
- No problems could be found associated with the 3D vias between tiers.
- Chip performance compromised by:
  - Poor transistor models
  - Large leakage currents in transistors and diodes
  - Poor current mirror matching
  - low yield



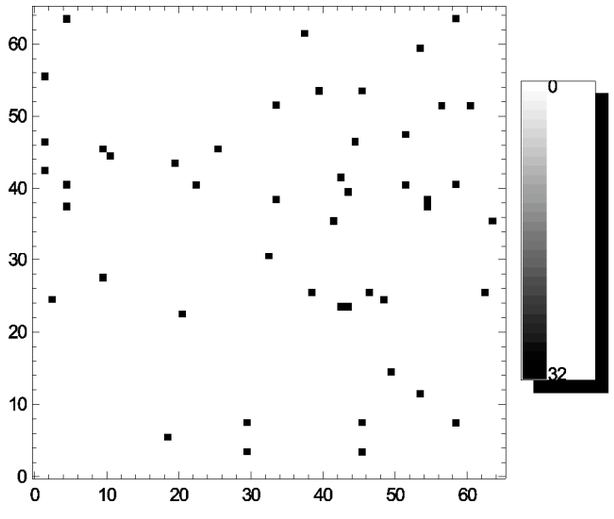
Preselected pattern of pixels for the injection of signal to the front-end amplifiers; pattern shifted into the matrix, than positive voltage step applied accross the injection capacitance; threshold levels for the discriminator adjusted according to the amplitude of the injected signal



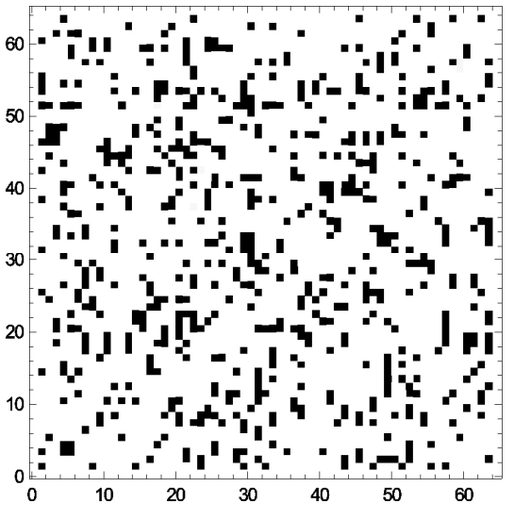
Pattern of pixels from the preselected injection pattern that after injection of tests charge reported as hit (grey level represents number of repetition – 8 times injection)

Injection of Test Charge into 119 Integrator Inputs of 64 x 64 Array

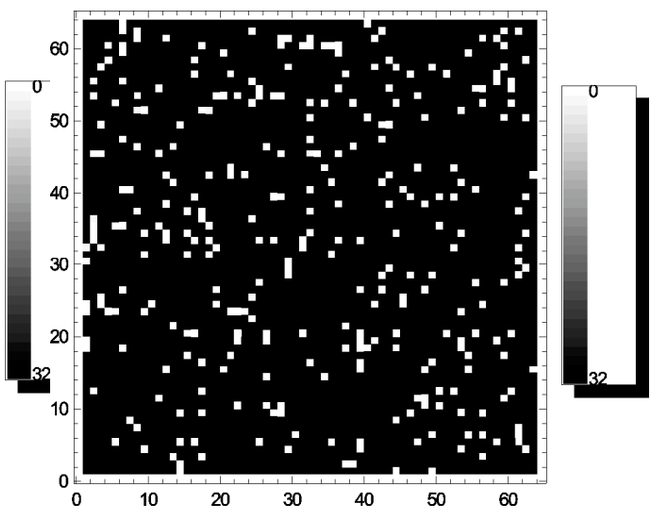
Data readout out using data sparsification scheme.



Maximum threshold



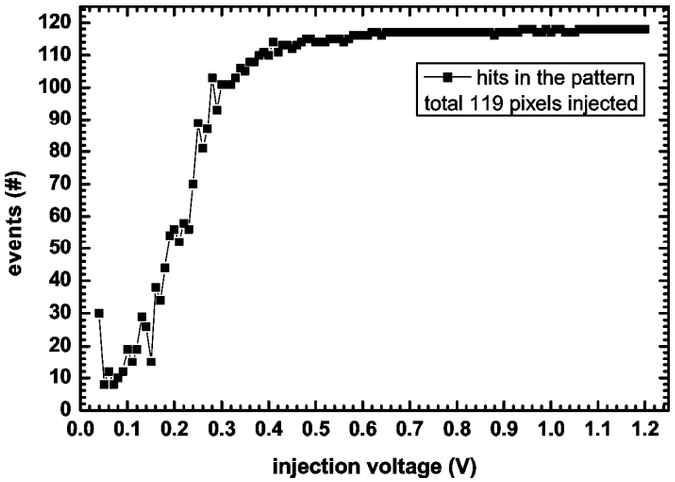
Intermediate Threshold



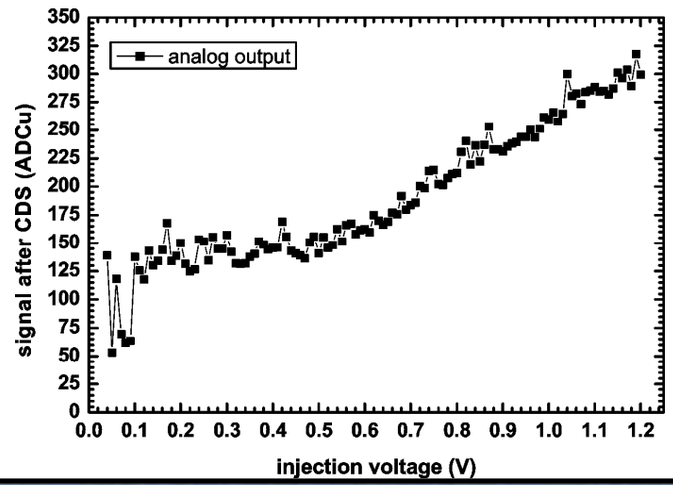
Minimum Threshold

Hit Pixels in Full Array as a Function of Threshold

As level of test charge through test capacitor (located between tier 2 and 3) is increased, more pixels exceed the threshold up to the maximum of 119 pixels

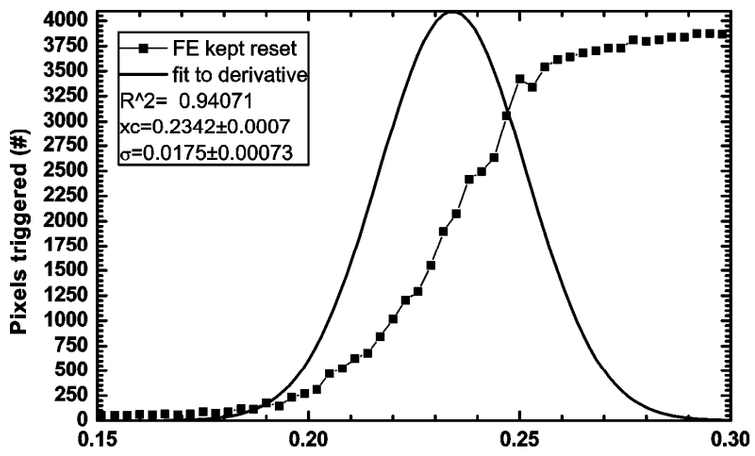


Mean analog signal level of pixels exceeding the threshold voltage. The red line is an indication of the linearity of the analog output signal (100 ADC units= 35 mv).
charge injection capacitor = 0.2 fF

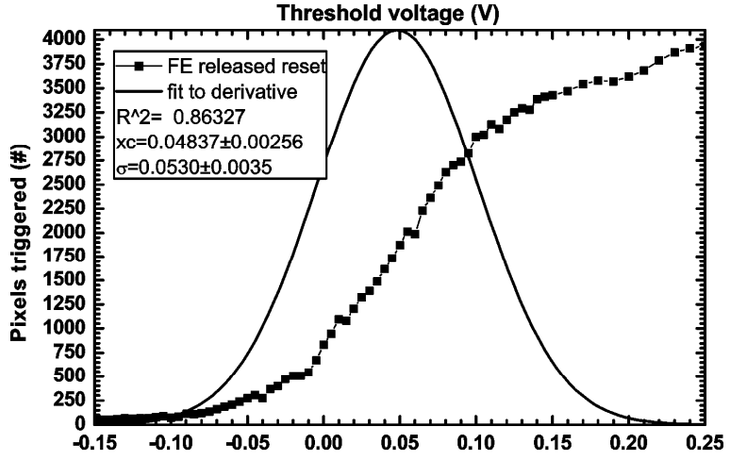


Analog response for 119 pixels in preselected pattern using sparsified readout.

A) With integrator held reset, threshold dispersion has a sigma of 1.6 mv or about 25e-.



B) With integrator reset and released, discriminator reset (autozeroed), threshold dispersion has a sigma of 4.9 mv or about 75 e-.



Pixel to Pixel Threshold Dispersion

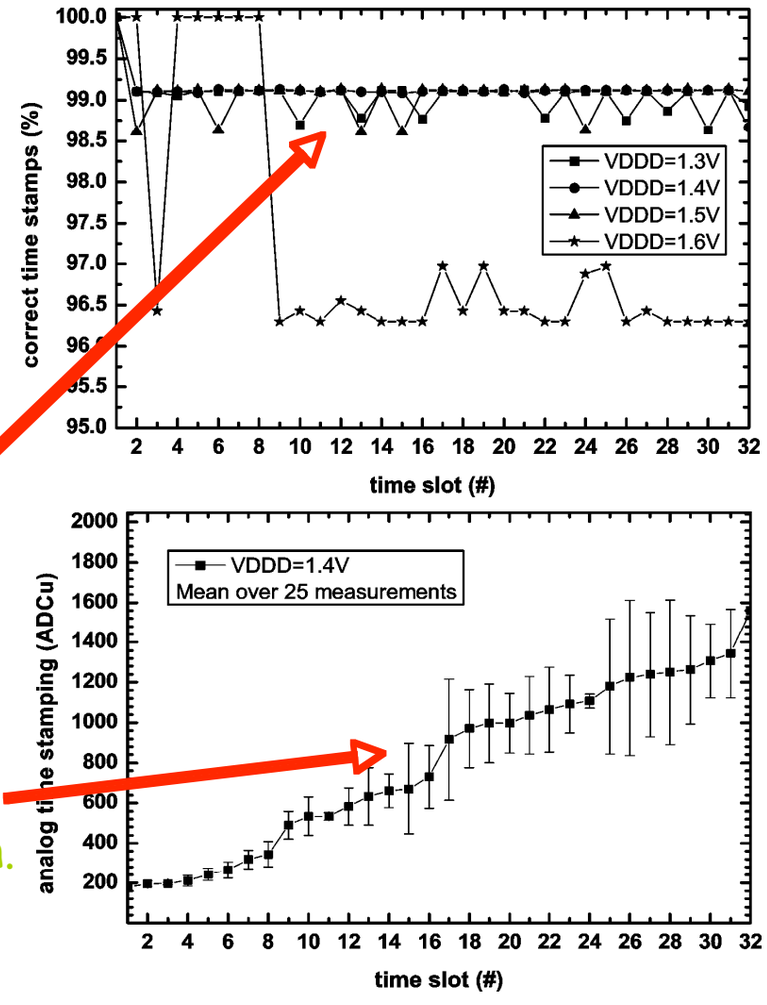
Threshold set at increasing levels and all pixels over threshold read out using data sparsification scheme.

Time Stamping Performance

Time stamping studied for 119 pixels in preselected pattern using sparsified readout. Digital time stamping uses inverted Gray code. External ADC used for analog time stamp

Charge is injected at a specific time, and time is compared to the digital time stamp. The readout shows a dependence on VDDD. Data shows that 118 of 119 pixels have correct time stamp for VDDD = 1.4V.

Analog time stamping suffers from high leakage current in sample and hold circuit. Problem to be corrected in next submission.

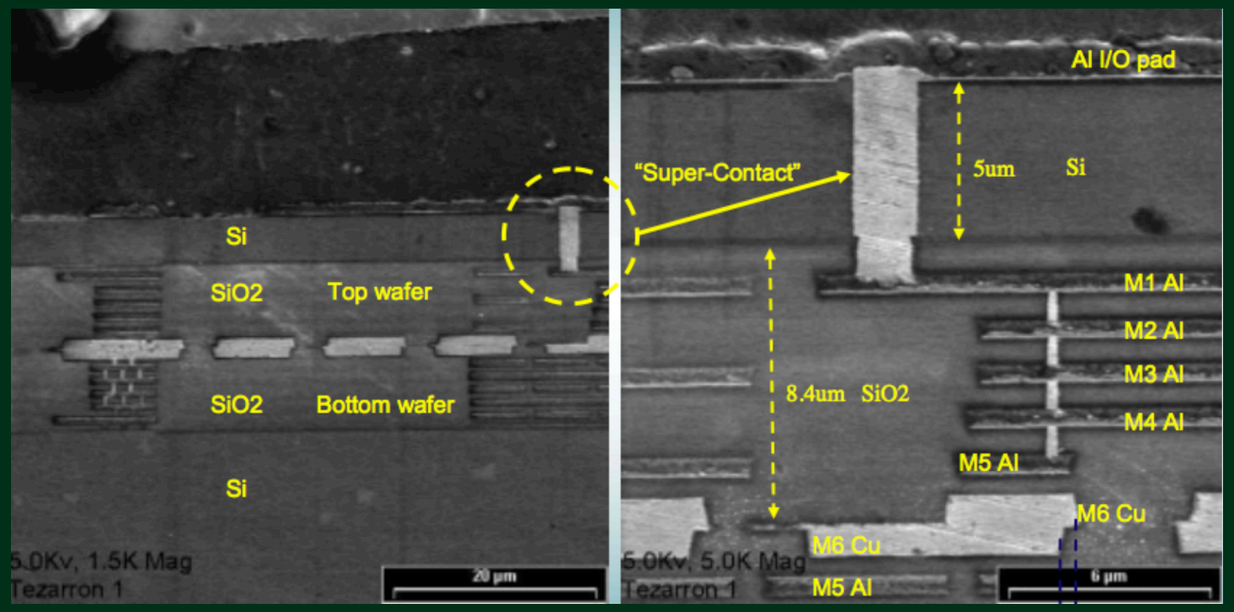


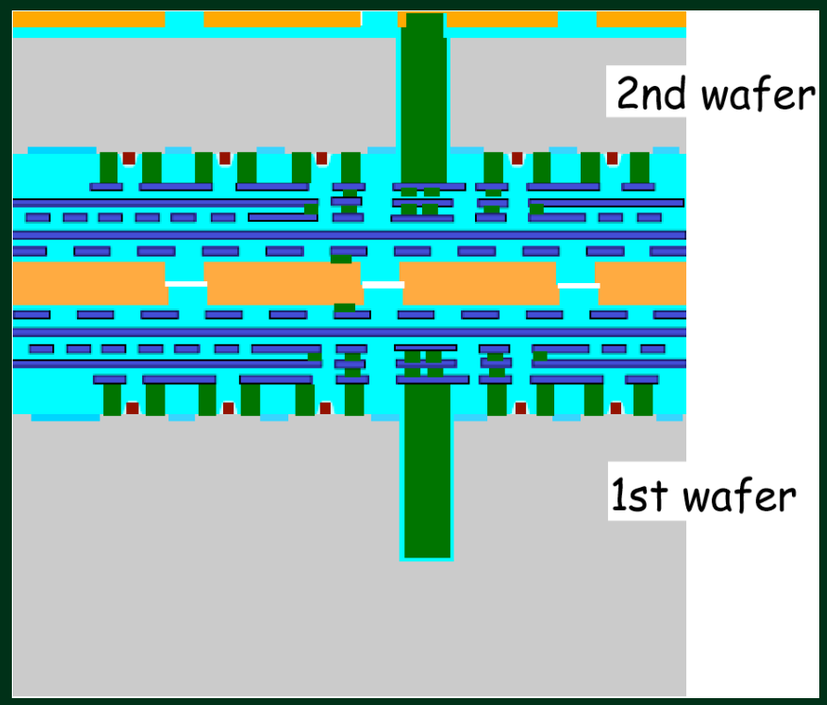
VIPII

- Work is proceeding on an improved version of VIP1 to be submitted to MIT LL at the end of September. The new chip is called VIP2b
  - Different power and grounding layout
  - Larger transistor sizes (0.18 > 0.5)
  - Larger pixels (30 x 30 microns)
  - Redundant vias and larger traces in critical paths
  - On chip ADC
  - More bits in digital time stamp (7 bits)
  - Redesign of current mirrors
  - Removal of dynamic logic due to leakage problems
- Very useful interaction with MIT-LL this week should improve overall quality of the design

VIPIIb

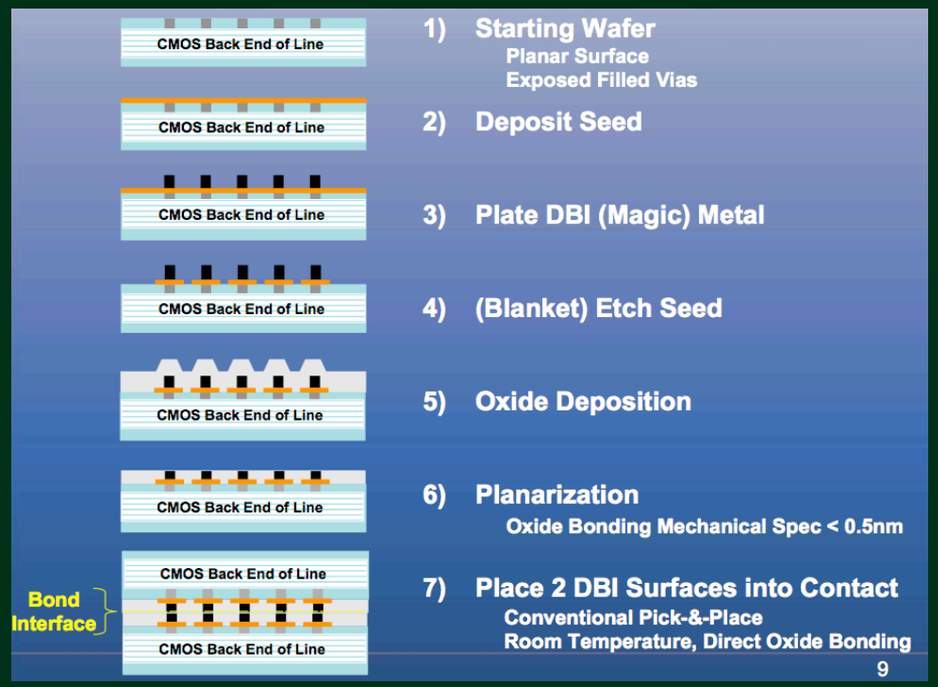
- Tezzaron (Chartered) has made their 3D 0.13 micron process available to Fermilab
- Uses cu-cu bonding to interconnect wafers fabricated with in silicon tungsten plugs
- Fermilab is organizing a multiproject run which will include a two tier version of the VIP
- Labs with NDAs:
  - Fermilab, Batavia
  - University at Bergamo (3D MAPs)
  - University at Pavia
  - University at Perugia
  - INFN Bologna
  - INFN at Pisa
  - INFN at Rome
  - CPPM, Marseilles
  - IPHC, Strasbourg
  - IRFU Saclay
  - LAL, Orsay
  - LPNHE, Paris
  - CMP, Grenoble
- VIP2 in *standard commercial CMOS*, more dependable models, better rad hardness, faster turn-around, availability of full wafers for sensor integration, less wasted area
  expect much better performance

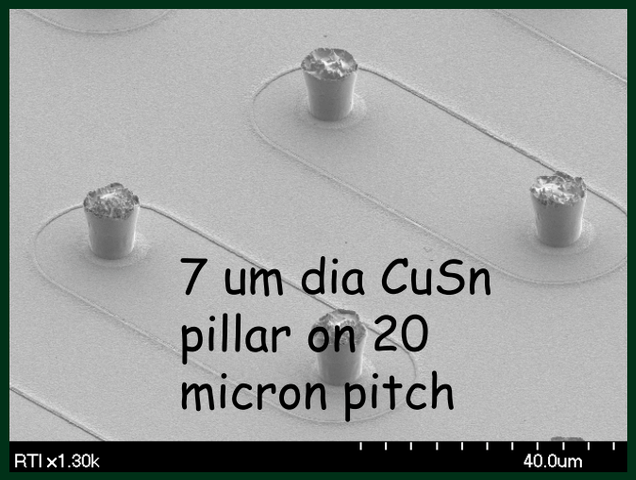


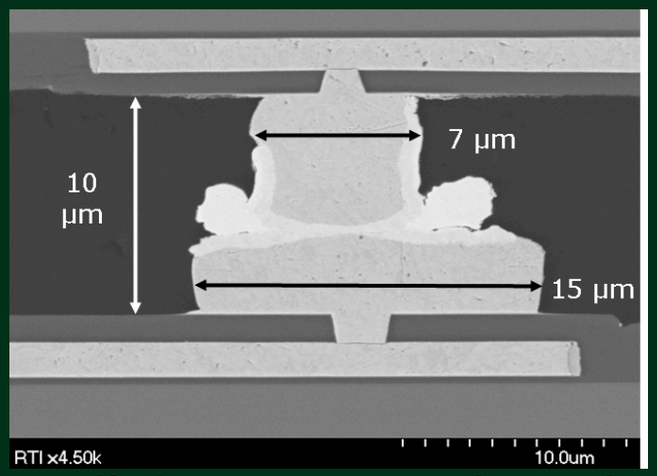


Sensor Integration

- 3D techniques can also be applied to sensor integration with readout
- We have tried two techniques: Cu-Sn and DBI oxide bonding
- DBI provides a robust bond with low capacitance and very fine pitch

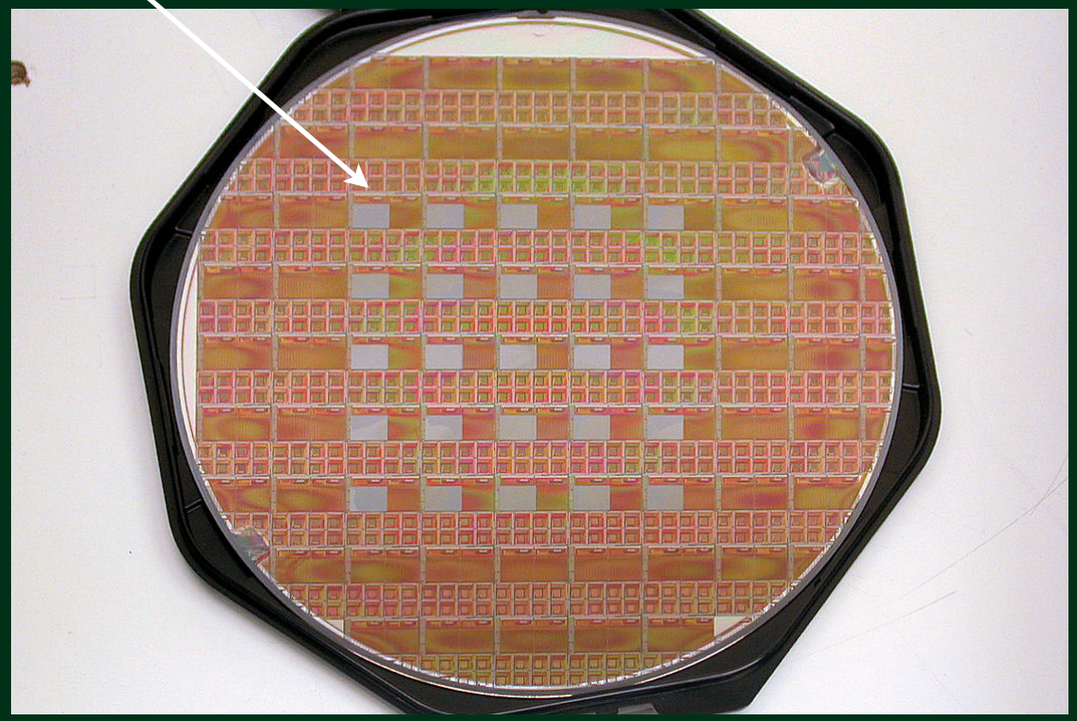






CuSn bond cross section

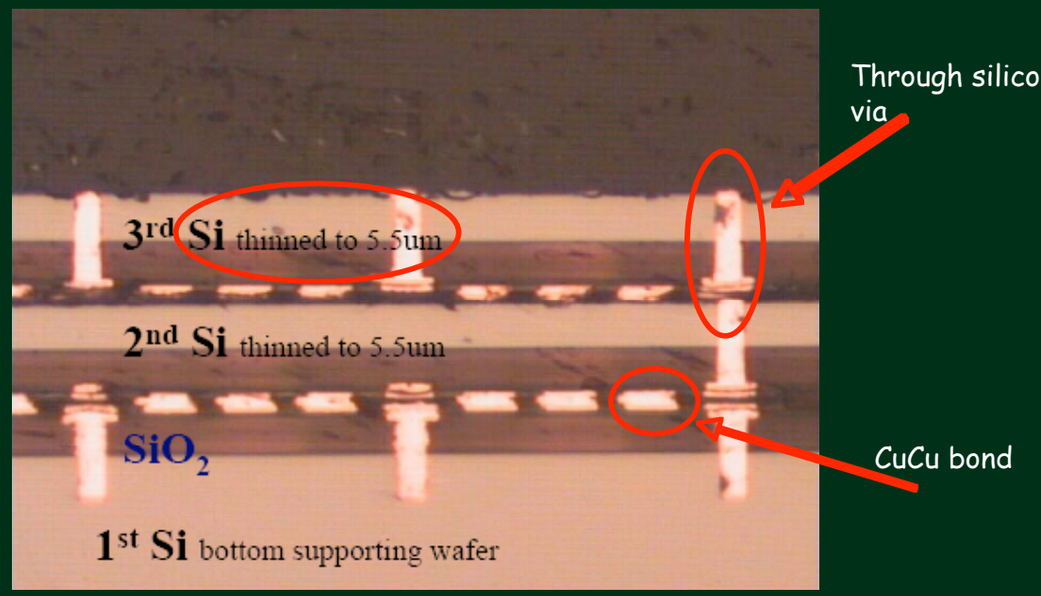
Fermilab sponsored study of sparse Cu-Sn bonding by RTI



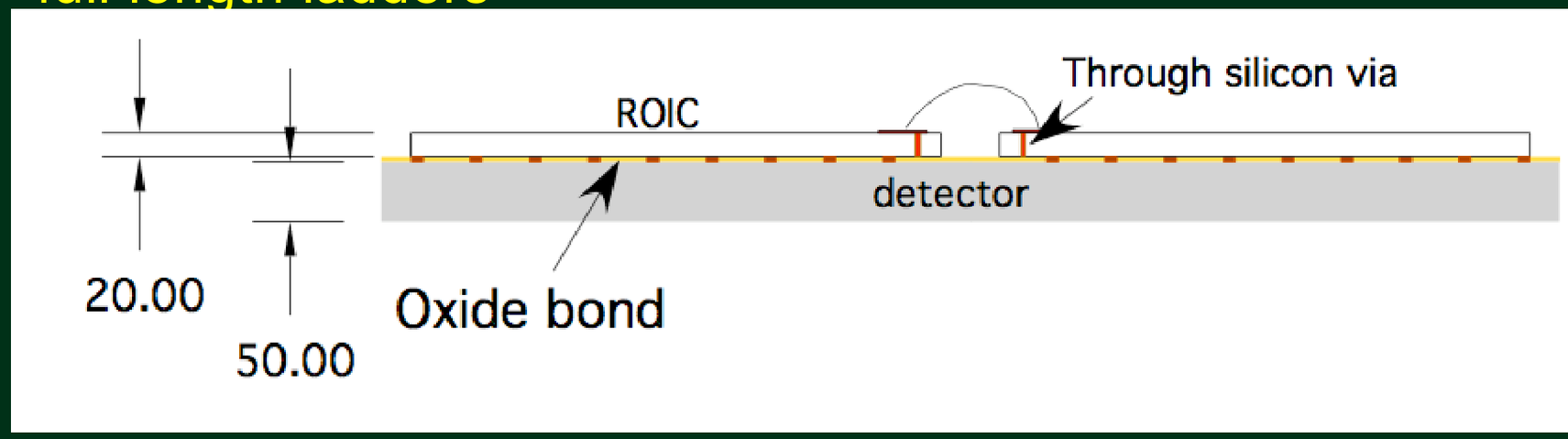
MIT-LL BTeV sensors bonded to FPIX2 wafer, tinned to 100 microns after bonding (would be better to bond ROIC to sensor)

Possible Layout

- A bonded Tezzaron wafer provides “supercontacts” above and below the substrate
  - Produce sensor wafer thinned and bonded to silicon substrate (MPI process)
  - DBI bond ROIC to sensor wafer using top supervias to contact sensor pixels to ROIC
  - After bonding to sensor grind to ~ 24 microns to reveal top super vias
  - Contacts to readout are made by lithography to top pads
  - Remove bottom side handle wafer to produced thinned ladder



- Alternative could use cu-cu bonds and polyimide bonded wafers - would allow all thinning on full wafers
- Use 6” sensor wafers - full length ladders
- no stitching
- some interconnect on sensor



Conclusions

- First 3D HEP chip (VIP) produced and tested
  - Functional, but low yield and high leakage current
  - Second version to be submitted this month
- Moving to commercial 3D technologies
  - VIP in two-tier 0.13 micron CMOS
- Developing sensor integration technologies
  - Received Direct bond Interconnect BTeV ICs bonded to thinned sensors
  - Shown robust fine pitch cu-sn bonding
- Conceptual design for a 3D integrated ladder
  We expect to have demonstrated a stacked, thinned ILC sensor/readout combination in 2009