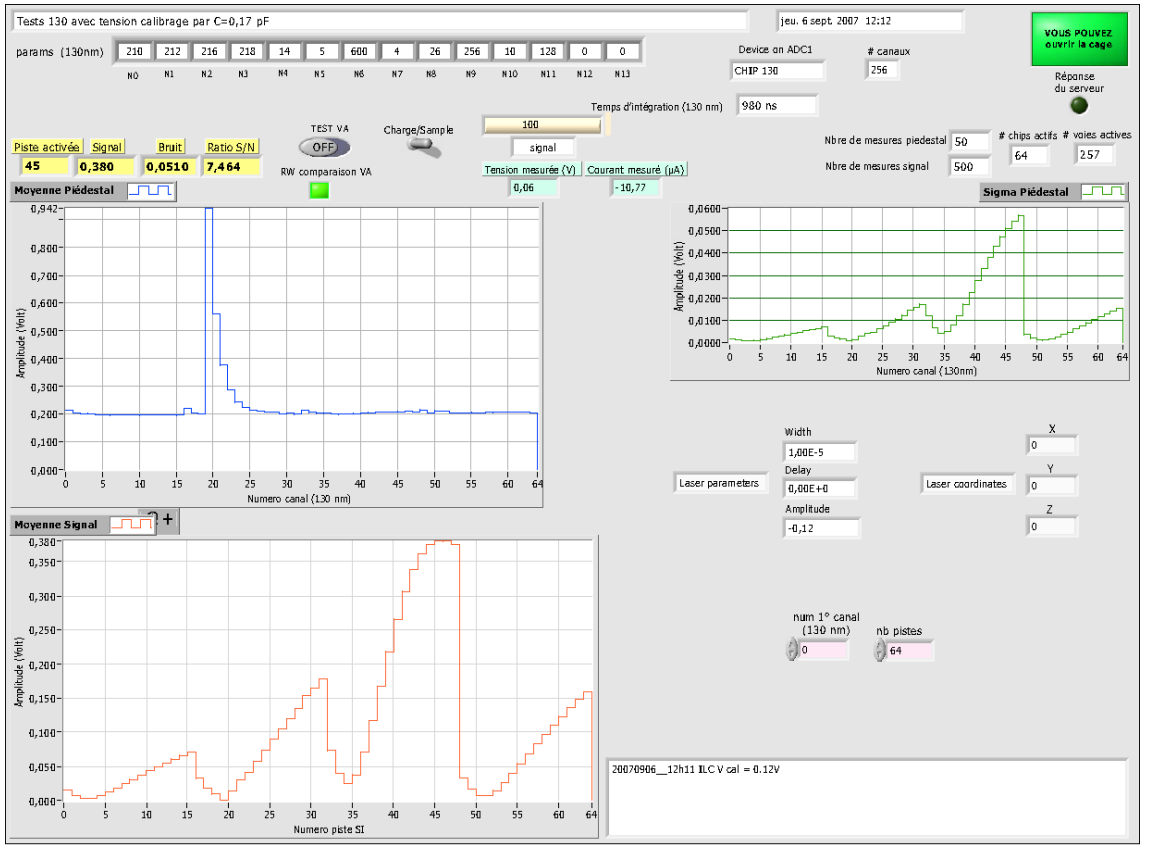
Paris Test Bench presentation

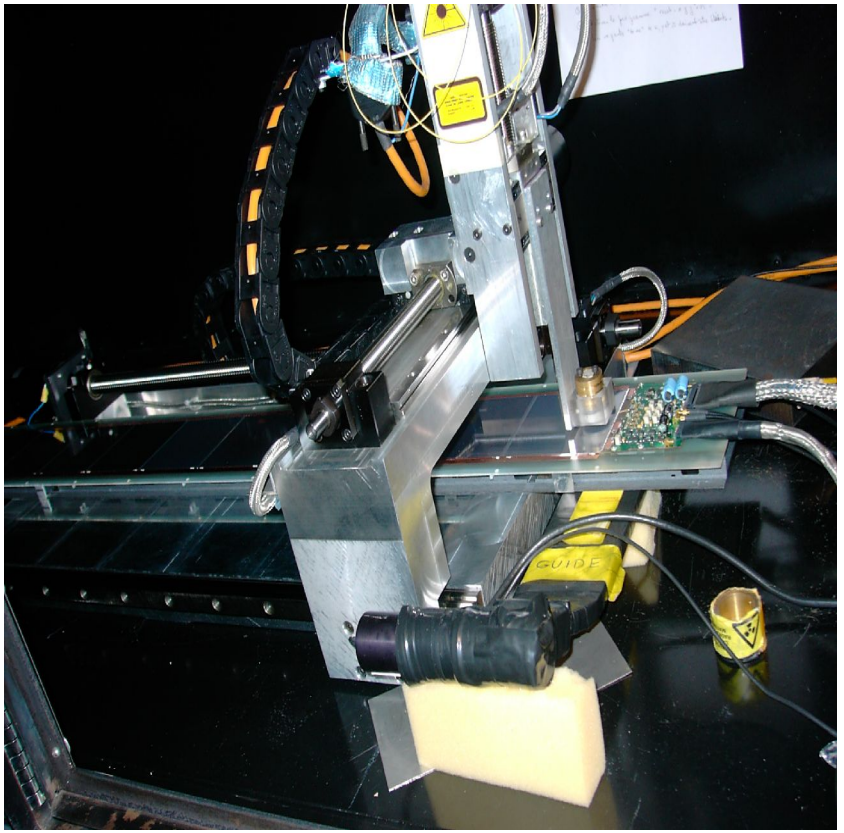


- C.Ciobanu, J. David, LPNHE, Paris
  - 7th SiLC meeting at CERN, July 2nd 2008

Contents

- Faraday cage containing
  - 3D table equiped with
    - Infrared laser
    - Radioactive source
  - PM + Scintillator for triggering

Faraday cage containing



- 3D table equiped with
  - Infrared laser
  - Radioactive source
- PM + Scintillator for triggering

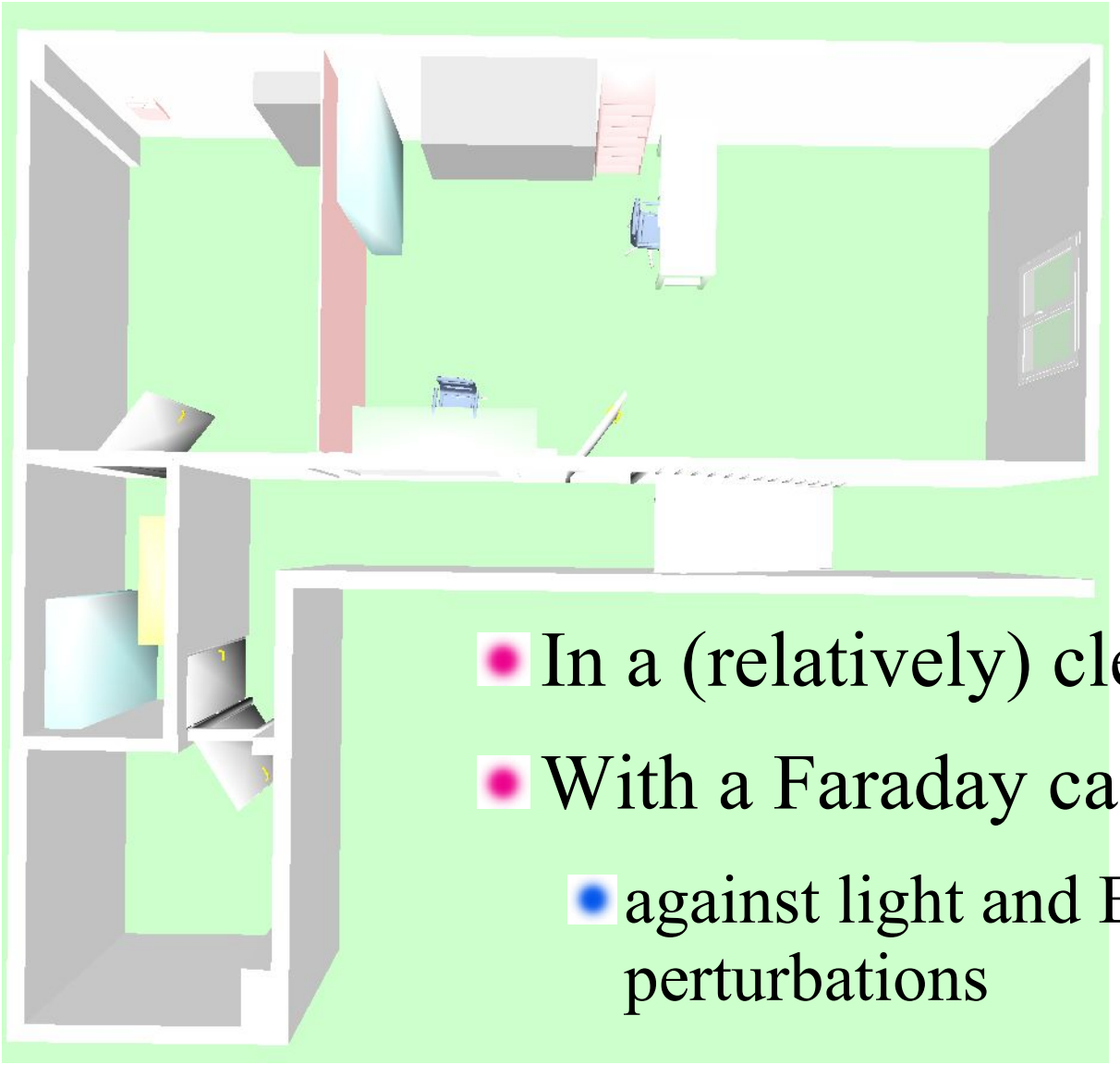
Contents

- PC under LabView controling
  - Polarization voltage source
  - Laser pulse height
  - Table 3D motorization
  - ADC of the output voltage of the VA1
- Miscellaneous devices
  - High voltage for the trigger PM
  - Discriminator

Contents:

- Trinocular (binocular with a camera)
  - For checking bonding etc.

Where:

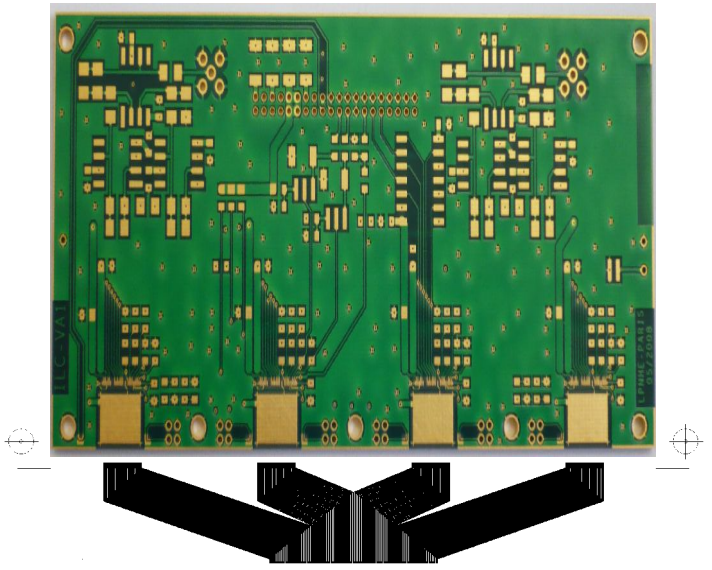


- In a (relatively) clean room
- With a Faraday cage
  - against light and EM perturbations

Status of the electronics:

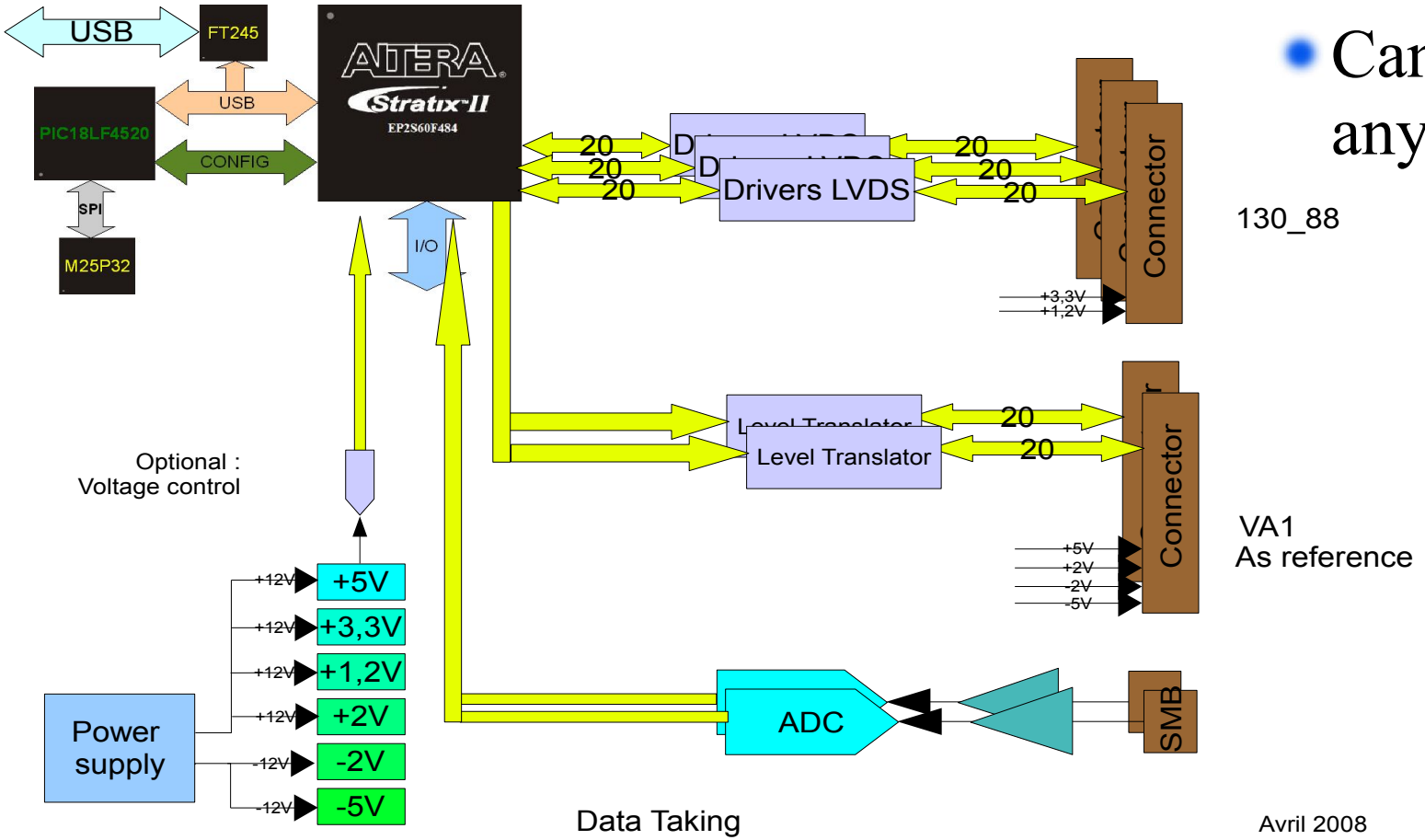
- VA1 (as reference)
  - Printed board done
  - Ready to be cabled (discrete componants)
  - Then, chips to be bonded (at bonding lab)
- Pitch adapters
  - To be delivered (mid-july)
- New chips 130
  - Sent to foundry
  - Return end september

- Daq card (called Altera card)
  - Printed board designed
  - Componants ready for cabling
  - VHDL programming in progress



(very) near future hardware:

- Whole system via USB links
  - Can be read via any computer



Future hardware:

- It's a step to an Ethernet link,
  - Avoid a PC in the experiment hall
  - Faster, more data
  - Upgradable to gigabit ethernet

Future software:

- Software
  - Under Linux
    - Easier to maintain
  - LabView just for some slow-controls
    - waiting a dedicated software (to be defined)
  - Quasi-online analysis via Root

Thank you