Discussion of the next steps on the SiLC Electronics R&D:

after the submission of the SiTR_130-88

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I.- Immediate steps: already ongoing

The chip SiTR_130-88 with the complete set of functions as described in T.H. Pham's presentation was sent to foundry on June 24th.

On July 1st was held a meeting between LPNHE and B.U. to discuss some of the next steps, concerning the tests and the next version of the SiTR series.

Let's present hereafter these next steps; they are subdivided in immediate, medium term and longer term developments.

I.1. The preparation for the tests in functionality of the SiTR-130-88

To be achieved now:

- Write-up of the user Manual: a detailed version by iterative steps (B.U.+ LPNHE)
- Sending the layout pins I/O of the SiTR_130-88 to HPK (bump bonding preparation)
- Also to the designers of the FE boards to host these chips and for the DAQ designers

These last 2 points are to be provided by LPNHE

In progress: the preparation of the FE boards (LPNHE)

Two types of FE boards are in preparation to host the new SiTR_130-88:

- The FE that will host 4 naked SiTR_130-88 chips that will serve to read out modules. Six such boards are starting to be prepared (design by LPNHE, cabling at CERN)
- The FE that will host one packaged SiTR_130-88 (standard package, not all channels will be read out in this chip and it will only serve for a full test of functionality on 20 chips (design LPNHE, fabrication SPC firm).

I.2. The functionality tests of the SiTR-130-88

As soon as the chips come back from foundry: second half of September or first half of October: preliminary tests on functionality at LPNHE and B.U. test benches
These first stage tests are foreseen to proceed over 3 months i.e. end of 2008.

Next stage of steps includes the tests with the hybrids connected to modules and tested with a radioactive source and the complete DAQ set-up before going to test beam. This should cover the first trimester of 2009.
The new DAQ hardware and software is under development (see J.David presentation) and should be achieved fall 2008 (at least the VA1 related part, for October test beam).

Test of the chips reading out the Si modules will be scheduled around April-May 2009 (see next section on medium term steps in slide 5)

I.3. Starting the design of the new version: preliminaries

First of all: why a new version?
This is requested by the EUDET project (a mini series to equip the prototypes on test beams in 2009 and 2010). This mini series should be available by the end of the EUDET project. It will be financed by the 4 EUDET partners with allocated EU funds.

I.3. Starting the design of the new version: preliminaries (cont'd)

This mini series will be produced in a min-wafer-production and not a multi project as the previous versions.

A preliminary discussion was held on July 1st between B.U. and LPNHE about the way to go for next version: main present conclusions

- Stay with IMEC and 130 nm UMC techno. But important to have an NdA with Faraday
- Revisit the present design and eventually correct remaining errors/pbs or add some modifications following what will be learnt from the test.
- Include a multiplexing of 256:1 (we know how to build it)
- Work out further the bump bonding option of the chip onto the microstrips

The new ASIC should be sent by January 2009.

I.4. Preparing the bump bonding of the chip onto the micro-strips

The SiTR_130-88 layout is being sent to HPK with needed specs (LPNHE) in order to allow HPK to prepare the masks of the sensors used for the direct chip bump bonding. Once the new untested chips are delivered from foundry, some of them will be sent to HPK (MTA) to allow HPK testing the bump bonding on the prepared micro-strips sensors

II.- Medium term steps

II.1. Dedicated test beam for measuring the SiTR_130-88 performances

The dedicated test beams for testing the full SiTR-130-88 performances are scheduled at DESY in the second trimester of 2009 (April or May).
There should be a request for test beam tentatively at this period of time (cf Zdenek).

II.2. Developing and testing the direct connection of the chip on the micro-strips

Once the chips are proven to work, there will be a dedicated effort to test the full performances of the chip-onto-the-sensor module with the traditional case, i.e. the chip on an hybrid board connected to the Silicon module by wire bonding.If everything goes fine this should occur over the first half of 2009 and even later in the year 2009.

II.3. Tests of the SiTR chips, cont'd

The tests of the SiTR_130-88 will be pursued in details over at least the 6 first months of 2009 and eventually further on, for getting a deep knowledge of its functioning over a large statistics (we have 20 packaged chips that means 1760 channels). This will also be useful in terms of yield and of uniformity in response. Important to share these tests among several of us (please volunteer) and we should sign an MoA or also NdA among us.
(Remind: the PRC-DESY requests a written report on the SiTR performances)

III .- Longer term steps

III.1. New technological developments on the SiTR chips

The first attempts on the SiTR_90 version should be started as soon as there is available manpower in terms of ASIC designers and after studying the best technology option. This includes revisiting the question of the technology choice and to keep an opened eye on the availability of the 90nm CMOS technology among the various founders.

Likewise the first developments of the 3D vertical interconnect option.
This should start sometimes in 2009 (to be defined according manpower availabilities).

Further other modifications or novelties are foreseen (to be discussed), including also the developments of the associated cabling and higher stages in the DAQ, higher multiplexing and more….

Plans to pursue further are now well defined but were not the object of this present discussion