Integrated pixel readout for a TPC at NIKHEF

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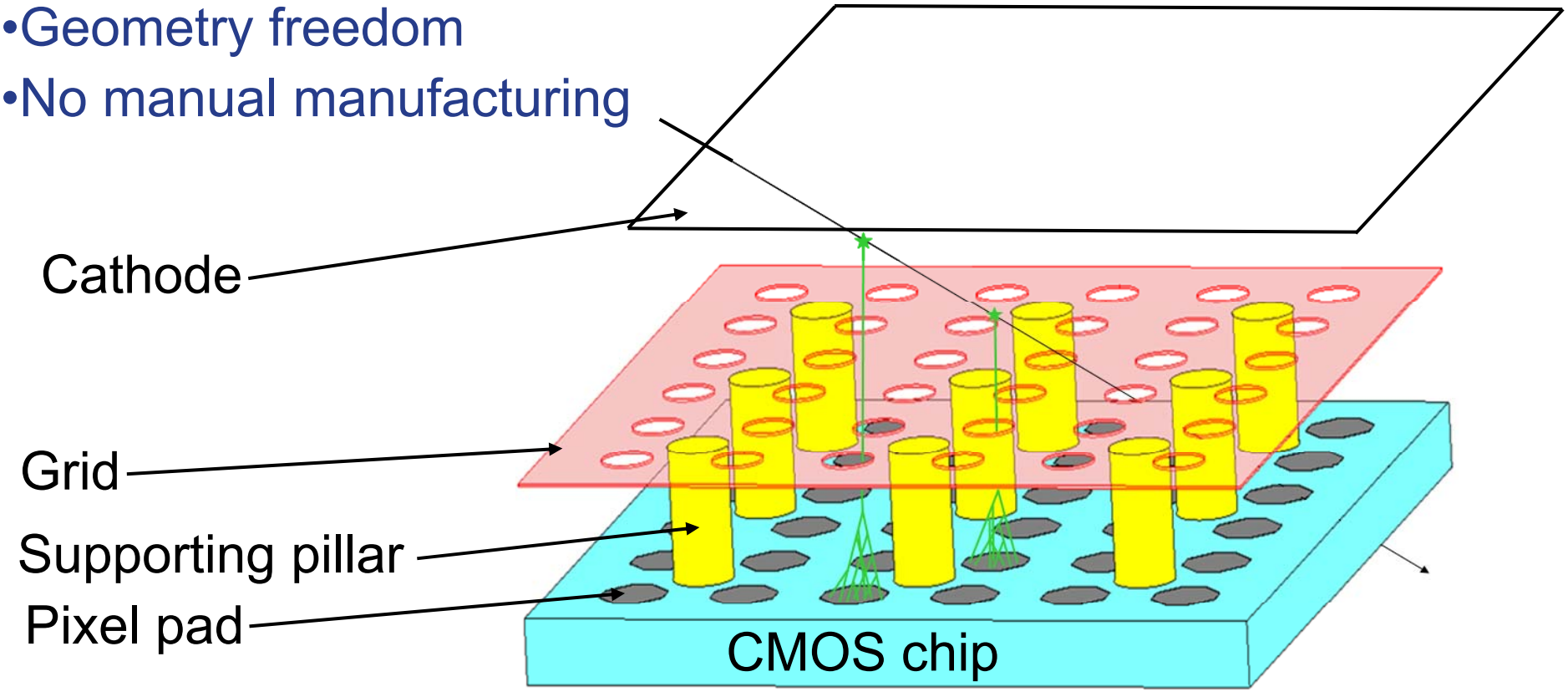
Overview

- Wafer post-processing concept
- InGrid production
- Tests
- New devices
- Future plans and conclusions

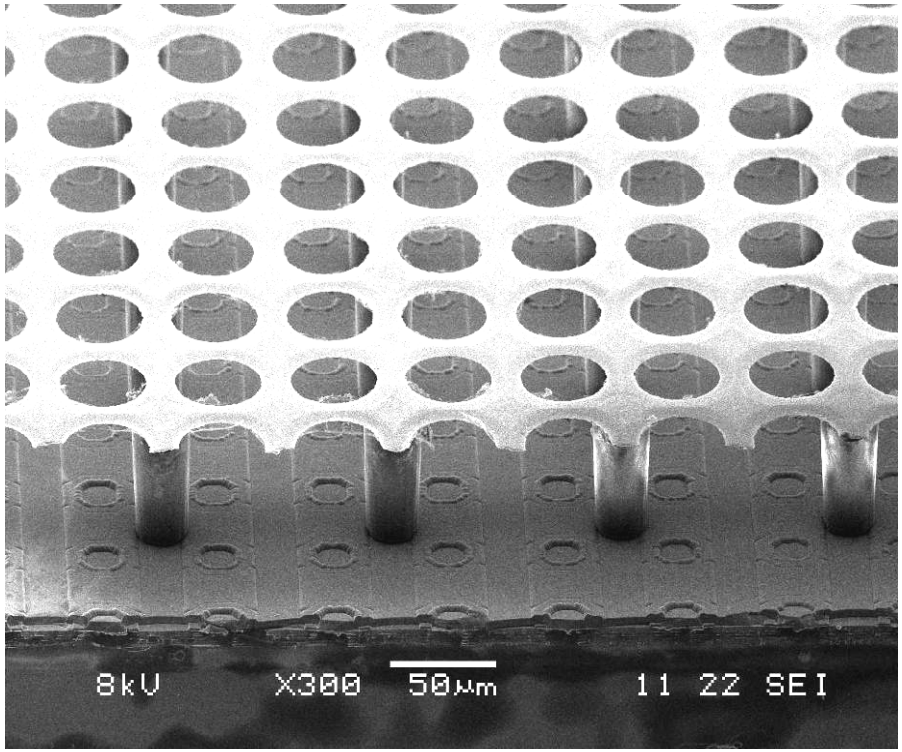
Wafer (or chip) post-processing

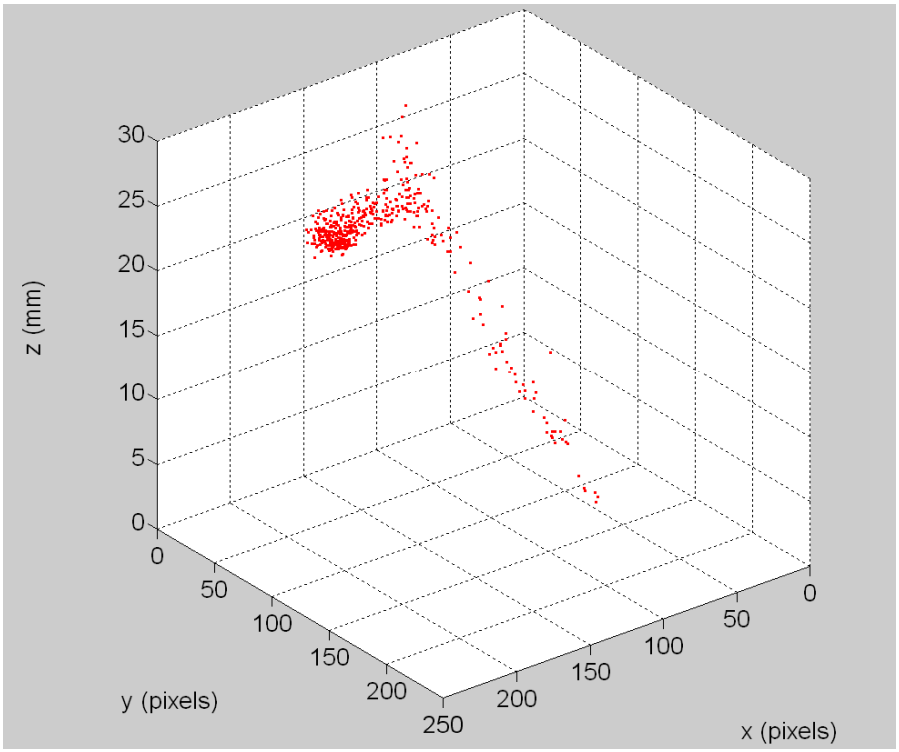
- Use the chip as electronics
- Perfect alignment holes to pixels
- No dead areas
- Geometry freedom
- No manual manufacturing



Standard device

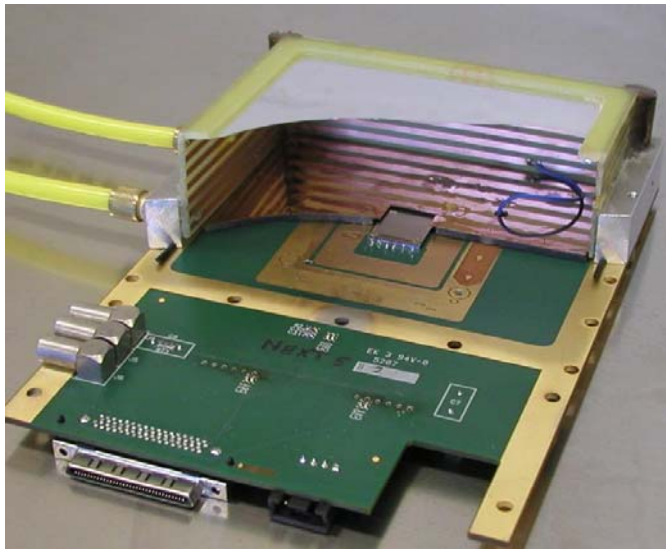
- Readout chip + anti spark layer + InGrid
- 3 dimensional track reconstruction
- Single electron detection with high efficiency

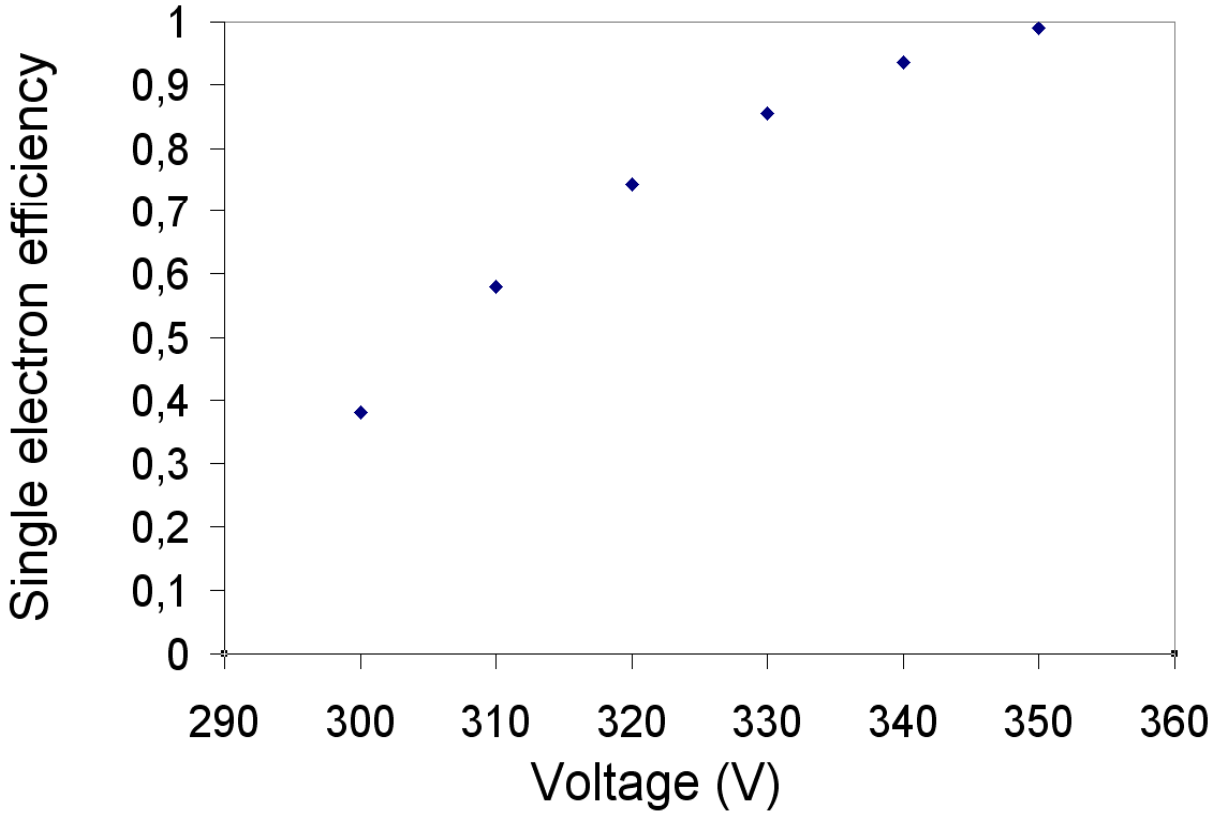




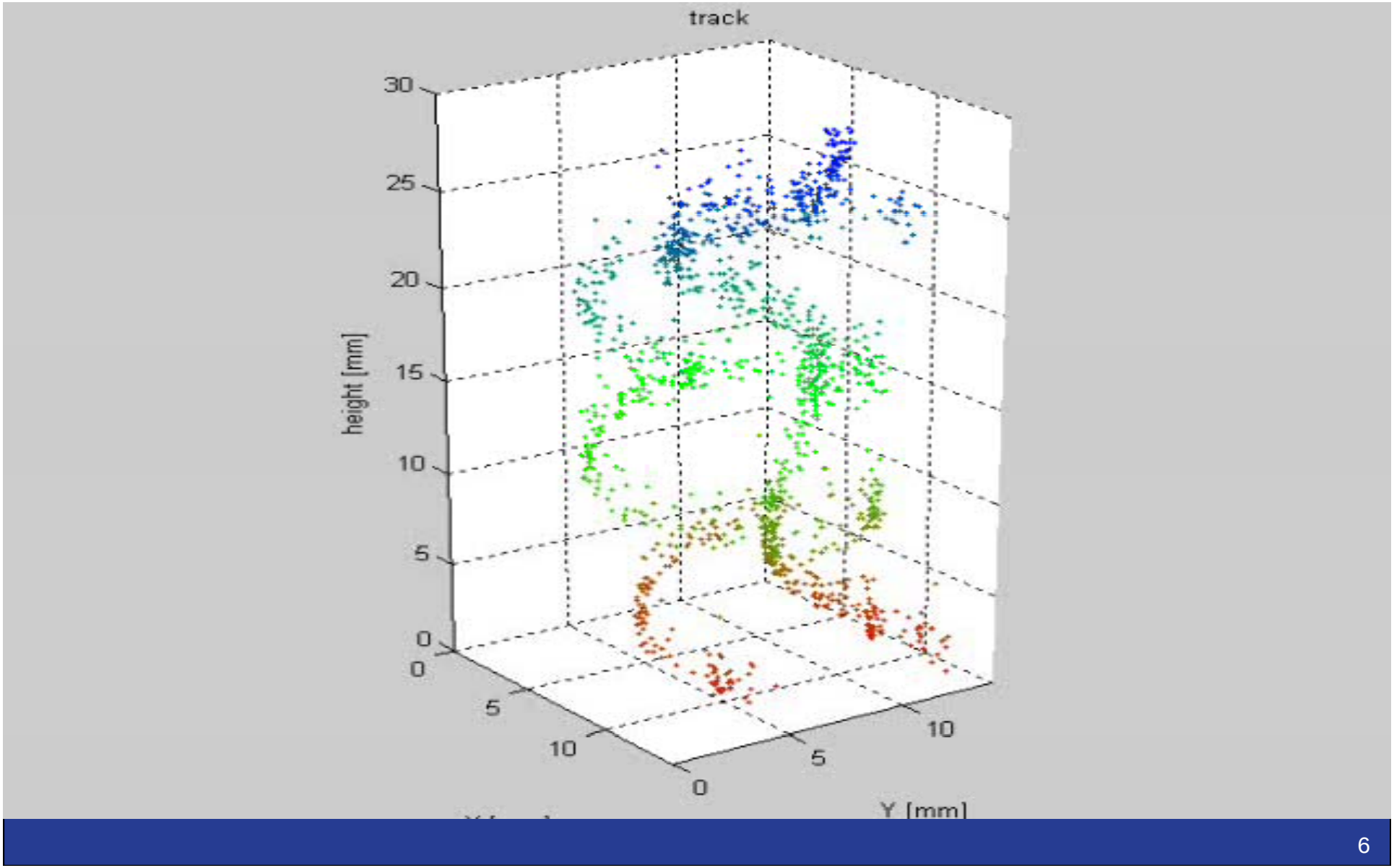
Single electron counting possible

- Charge spread over chip area with 10cm drifter in Ar/Iso (95/5)
- ^{55}Fe spectrum reconstructed from single electron counting



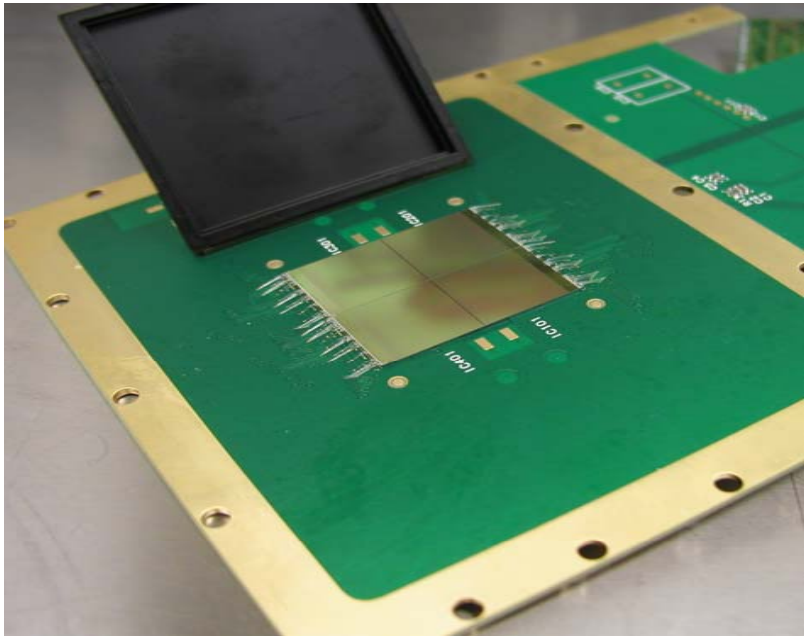


Beautiful ^{90}Sr tracks



Towards mass production

- Need of many post-processed chips for Next-quad and Next-64
- Yevgen is producing InGrids in single chips
  - About three chips per week
- Chip squares containing 3x3 chips will be processed at once
- IZM Berlin and SMC interested in production
  - 8 inches wafer facilities



Beam test results

- Beam test at the PS/T9 line at CERN

- Up to 10GeV pions and electrons

-2 Timepix+InGrid working for long time at NIKHEF

-Measurements with four different gas mixtures

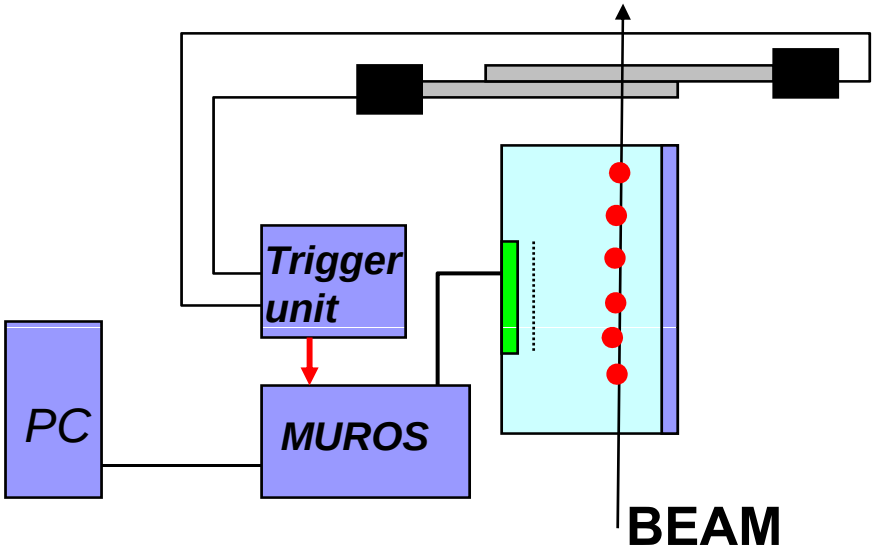
Xe/CO_2, He/Iso, Ar/CO_2, Ar/CF_4/Iso

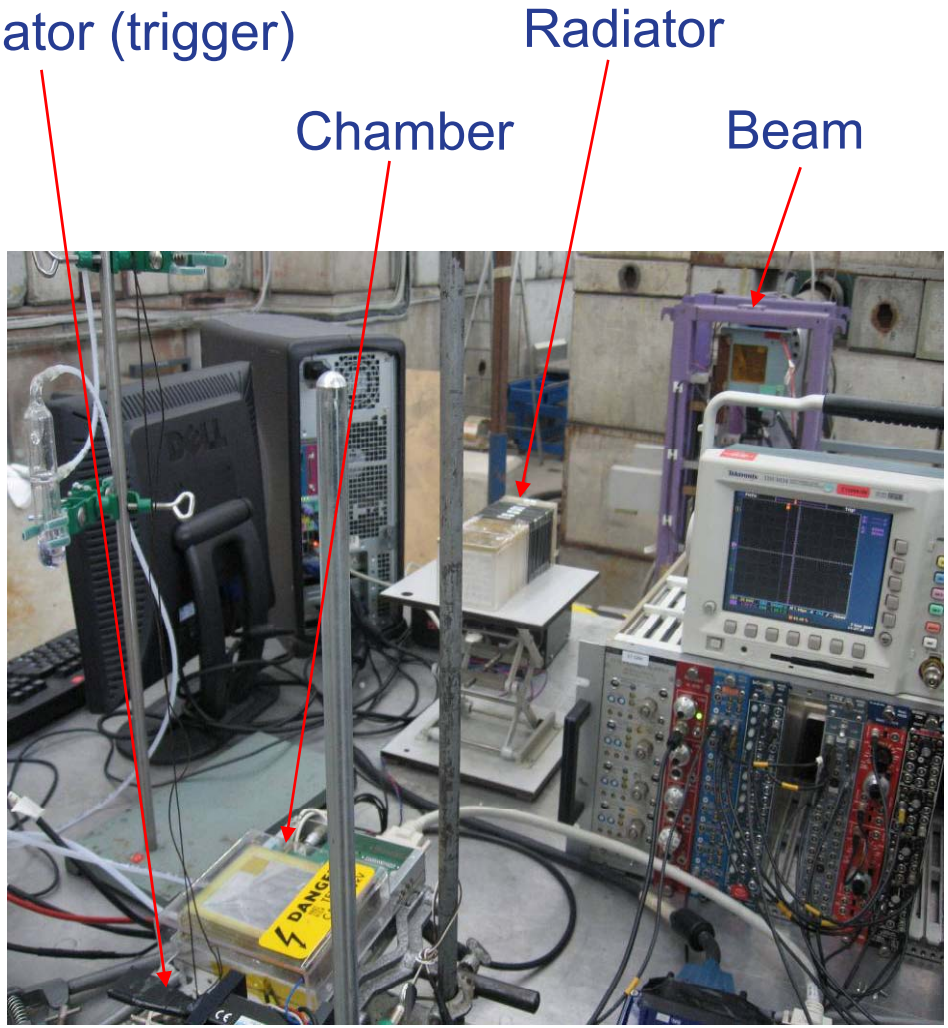
- One chip died in Xe/CO_2 at -490V (only 15µm a-Si)

-Rest of the measurements using a chip with 20µm a-Si

-Device can be used as a Transition Radiation Tracker

Beam test setup

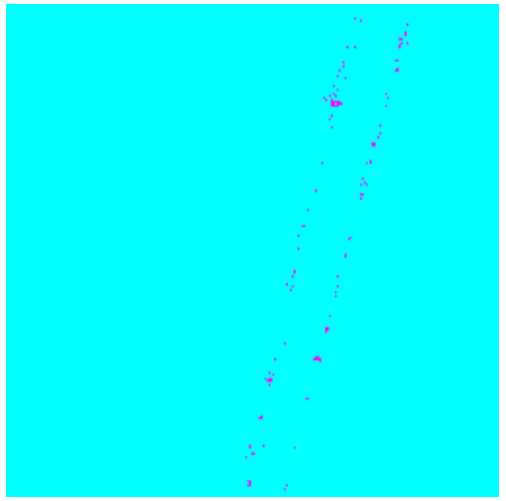




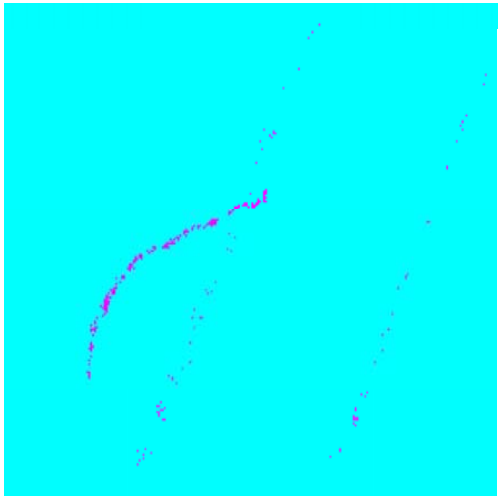
Tracks in different gases

Xe/CO2

He/Iso



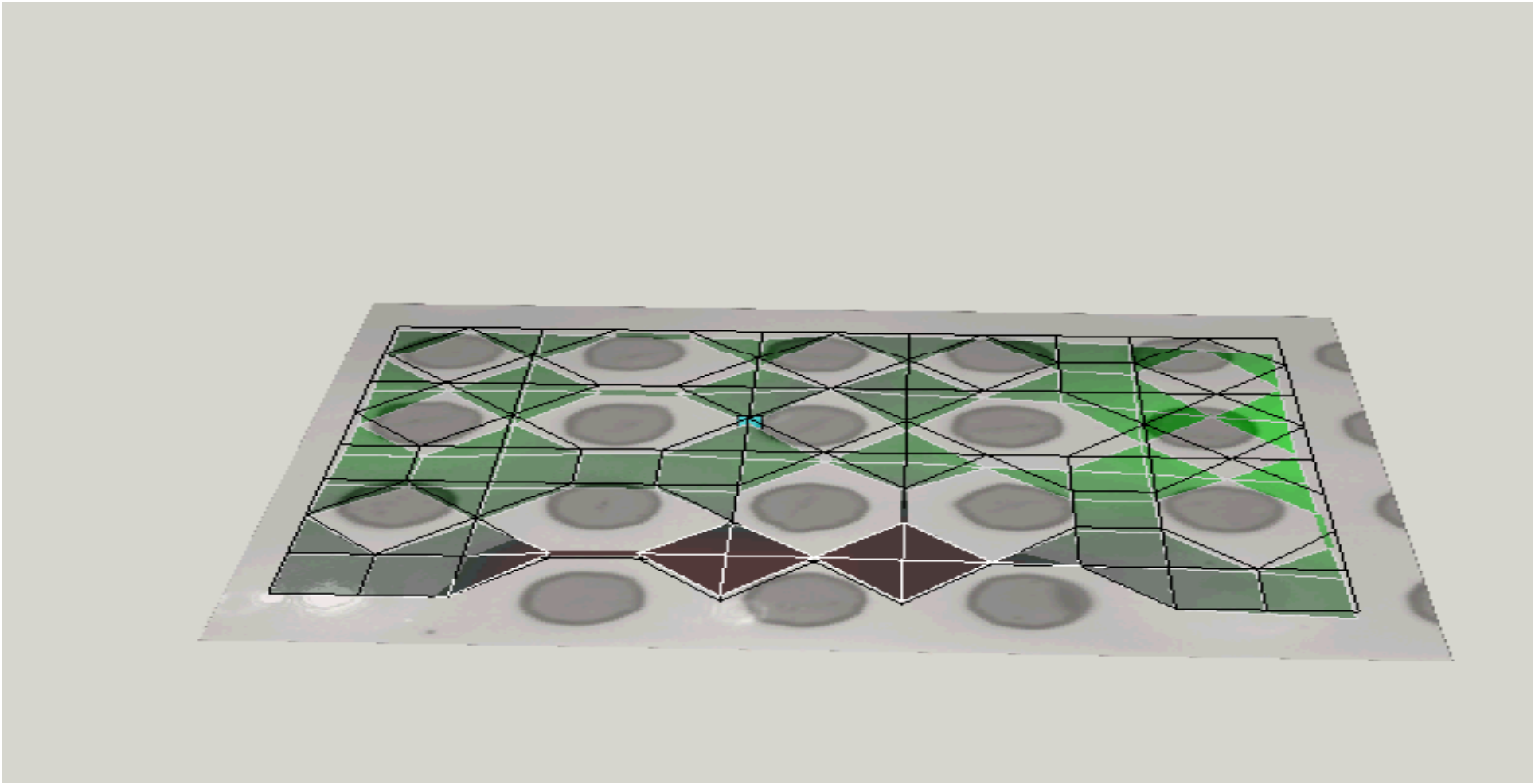
Ar/CO2



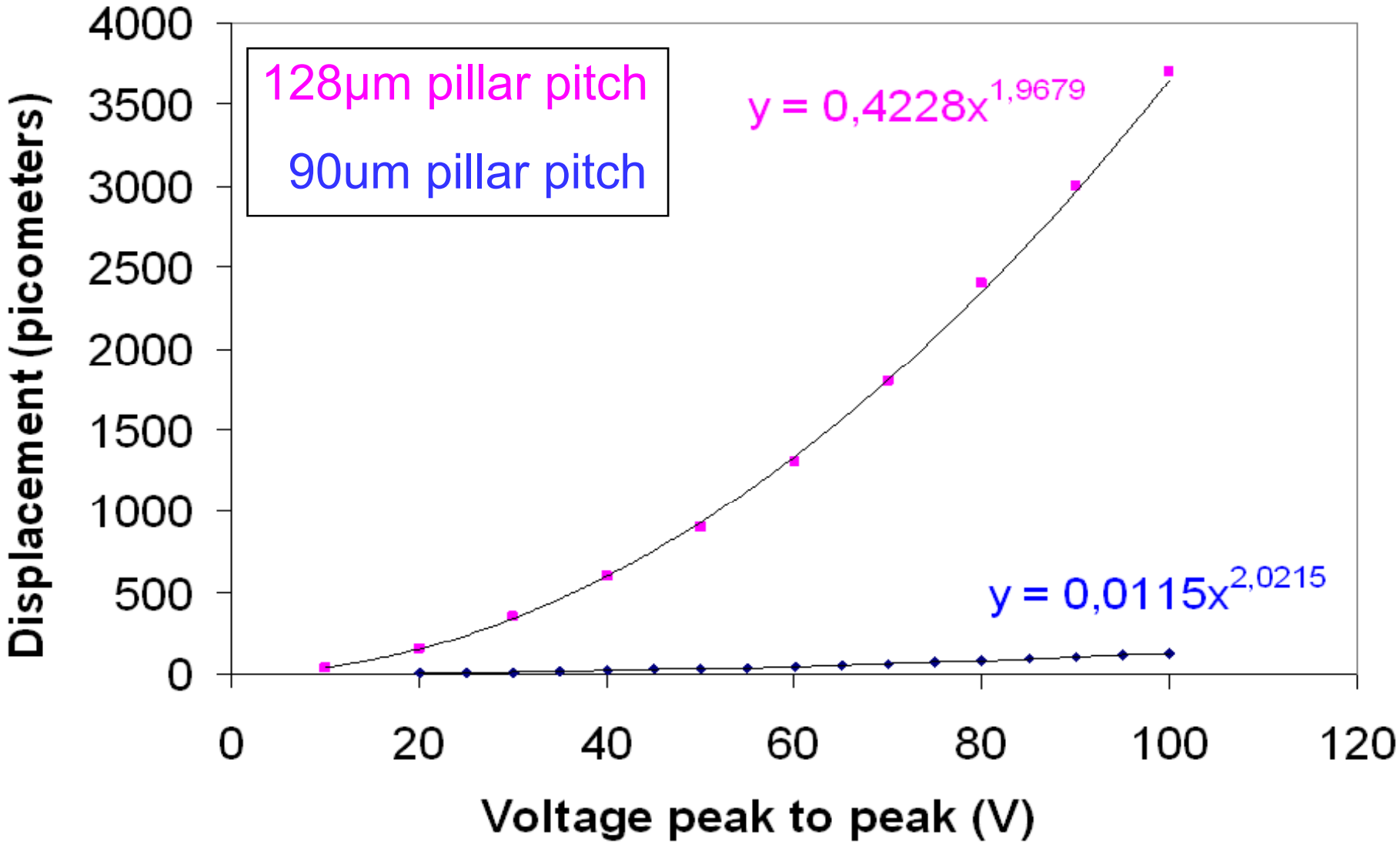
Ar/CF4/Iso

A mechanical curiosity

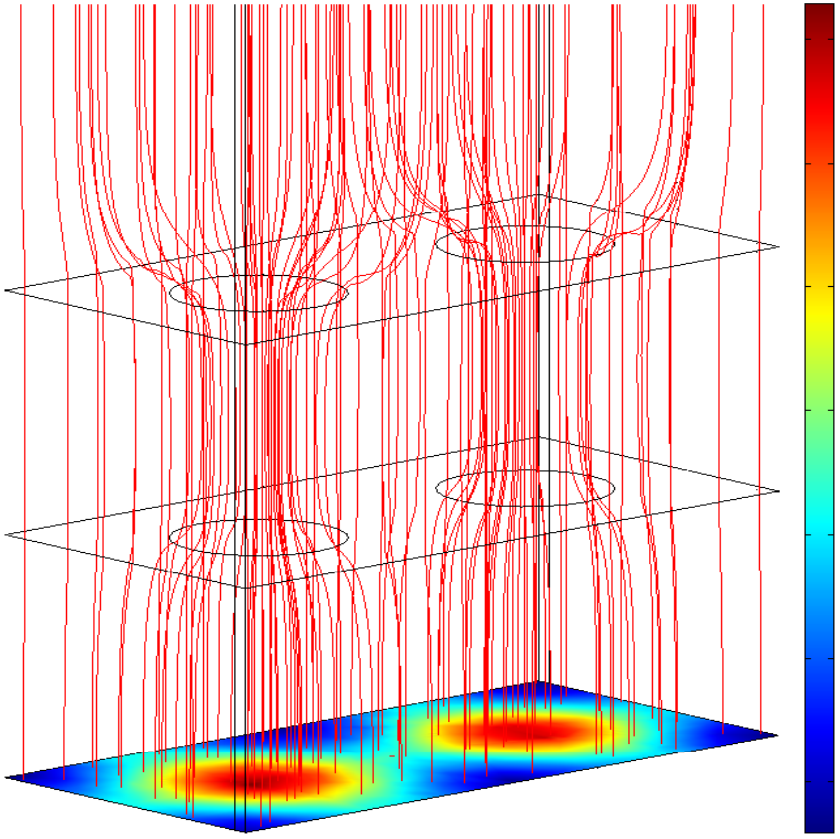
- Micromegas is sucked by the electric force
- InGrid is already fixed by the pillars
- How much does it move between pillars at 100KHz?

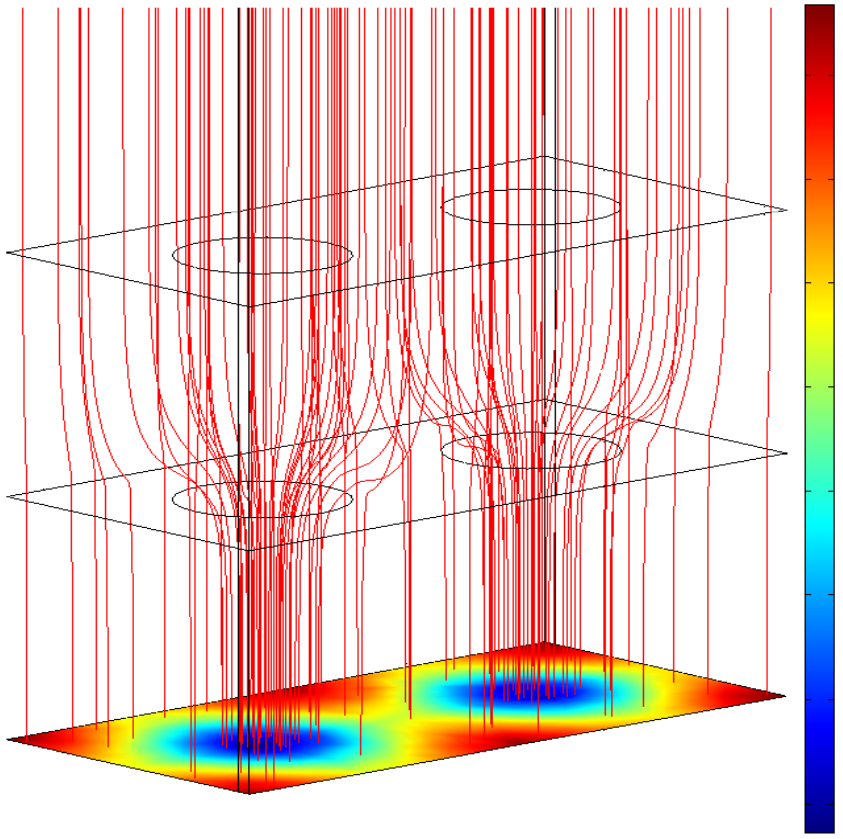


Vibrometer measurements



Simulated Twingrid electric field





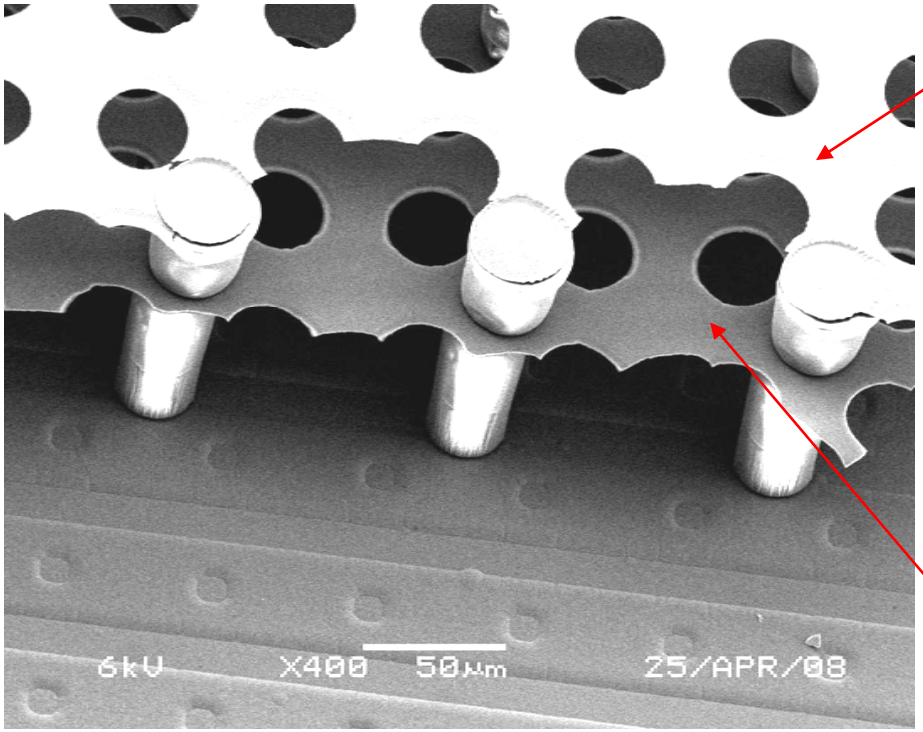
V_{bottom}=-100V

ΔV_{grids}=-500V

$V_{bottomgrid}$=-500V

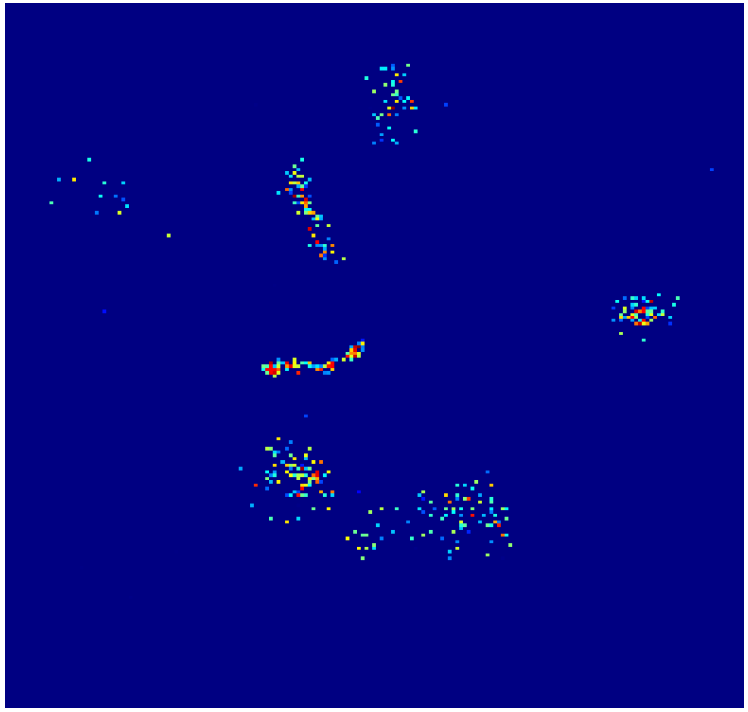
Twingrid operated for first time

- Double structure on a chip seems feasible
- No protection layer
- Chip survived ~5hours, protection layer needs to be added on next devices



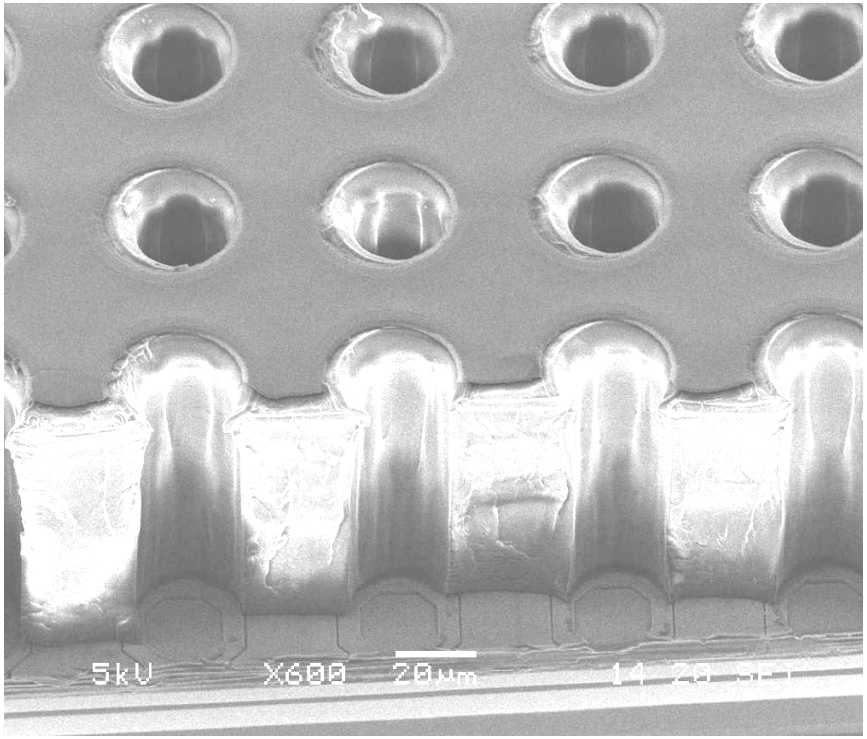
450V

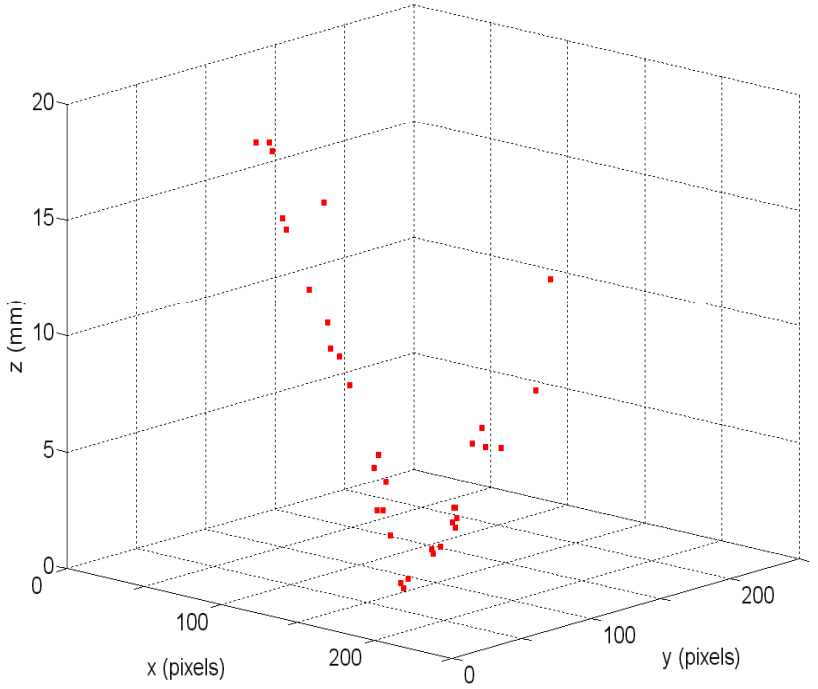
100V



GEMgrid

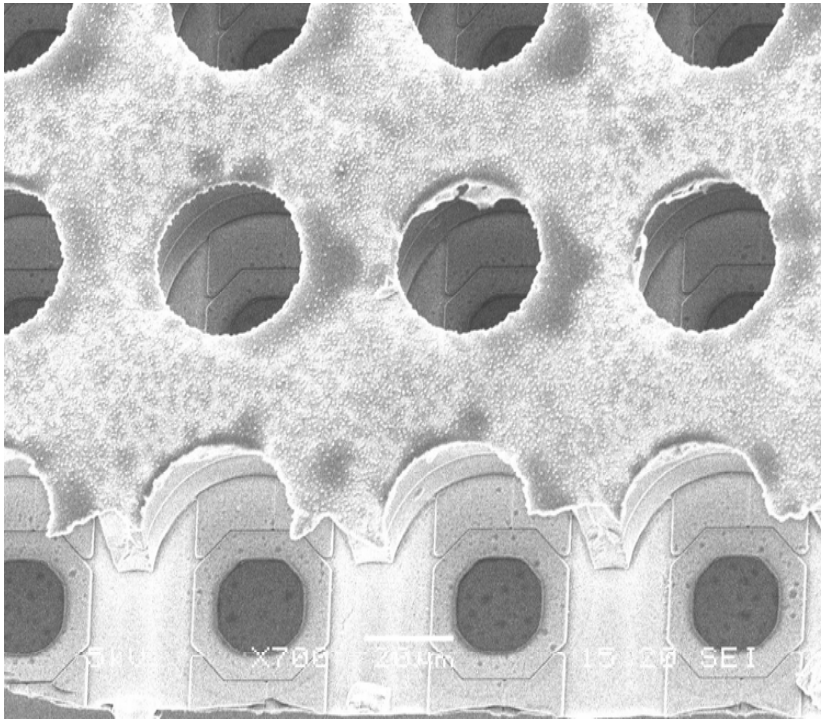
- Meant to resist drop ball test
- Similar to microbulk InGrid from Giomataris
- Low single electron efficiency, needs improved redesign

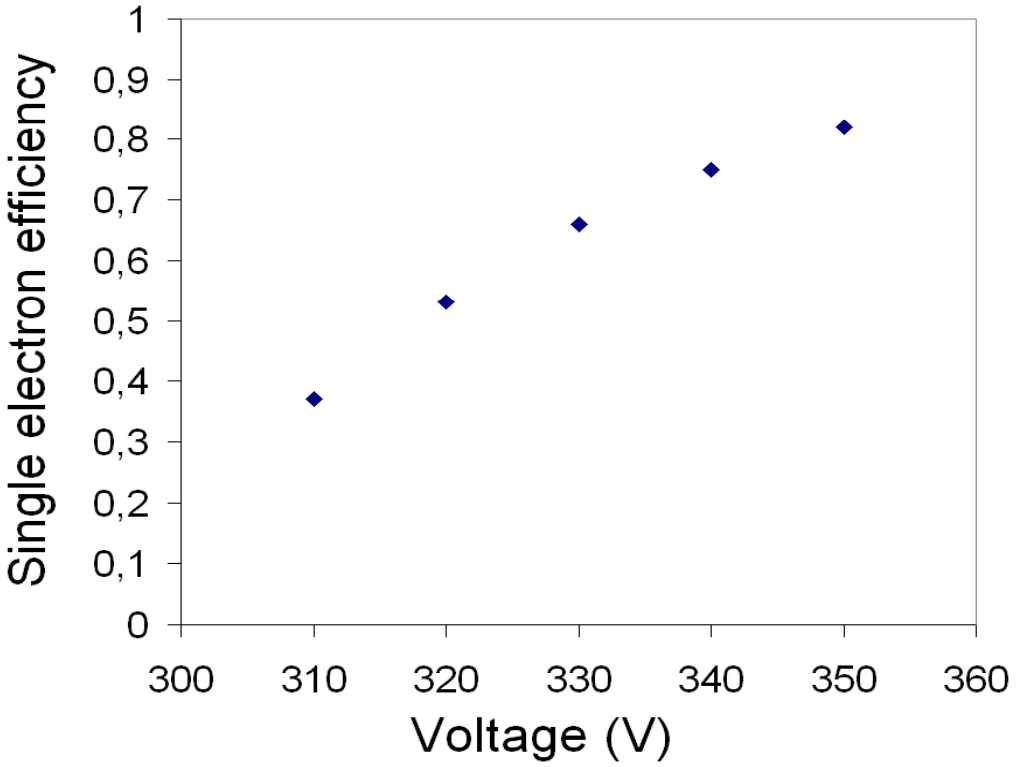




Improved GEMgrid with hanging metal

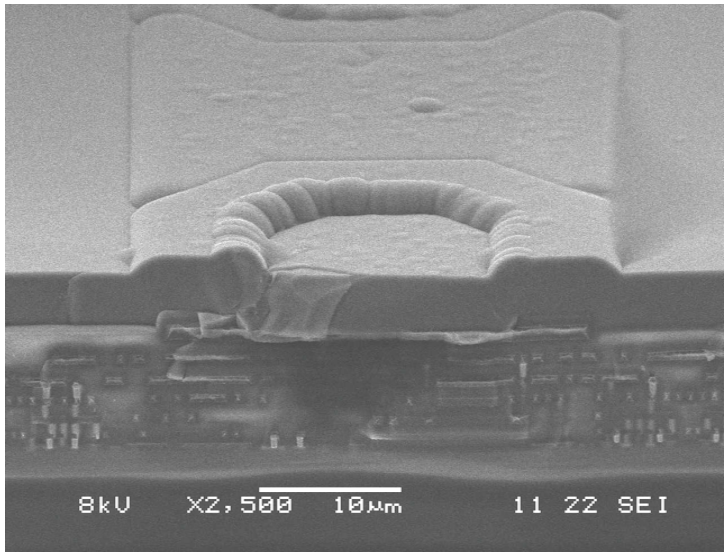
- Charge spread over chip area with 10cm drifter in Ar/Iso (95/5)
- ^{55}Fe spectrum reconstructed from single electron counting





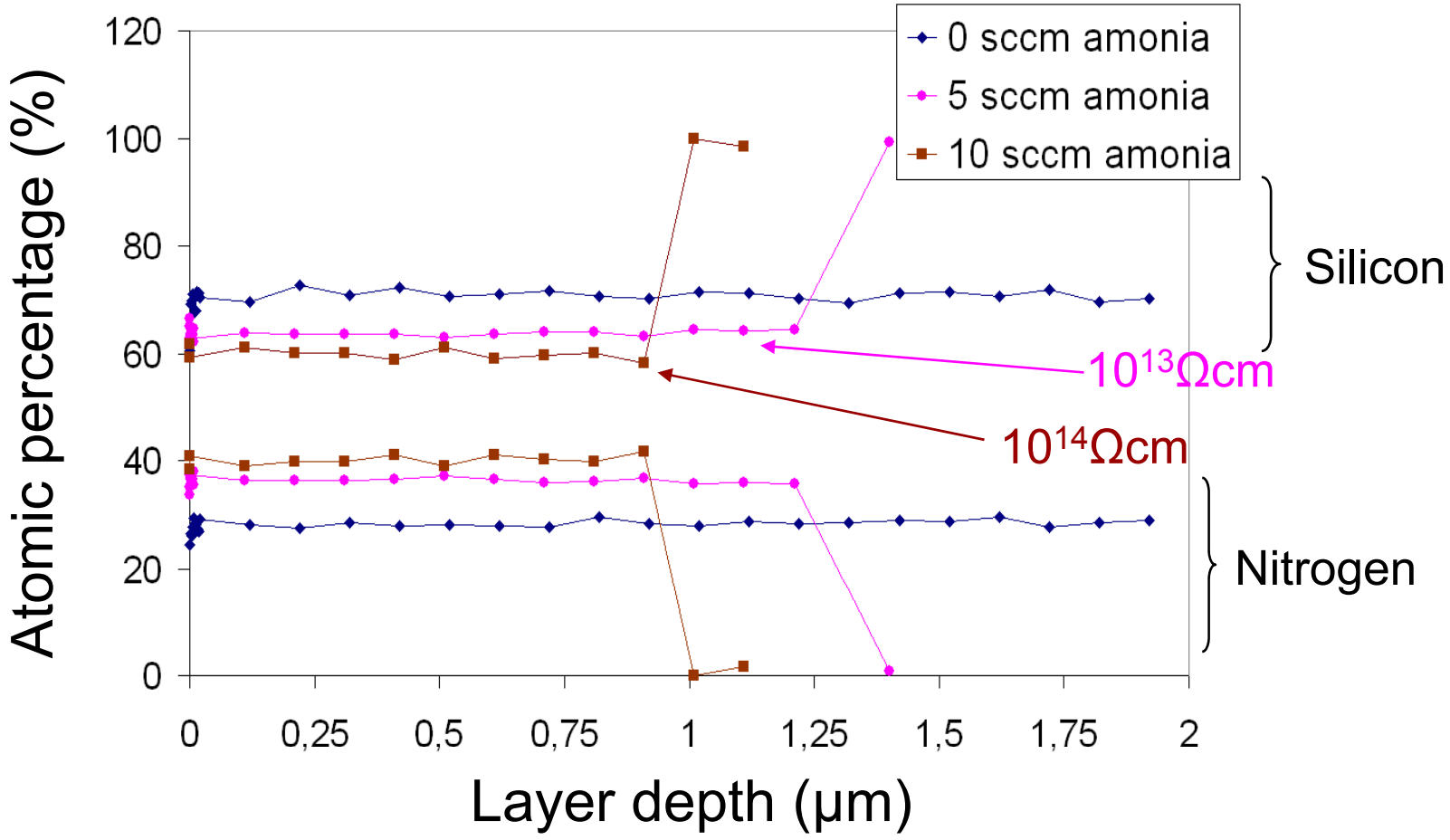
SiRN:New anti-spark material

- Si_3N_4 typical anti-scratch layer on CMOS
- Si-RichN, excess of Si makes it high resistive
- Deposited by PECVD at 300 °C or lower
- Any lab can do it !!



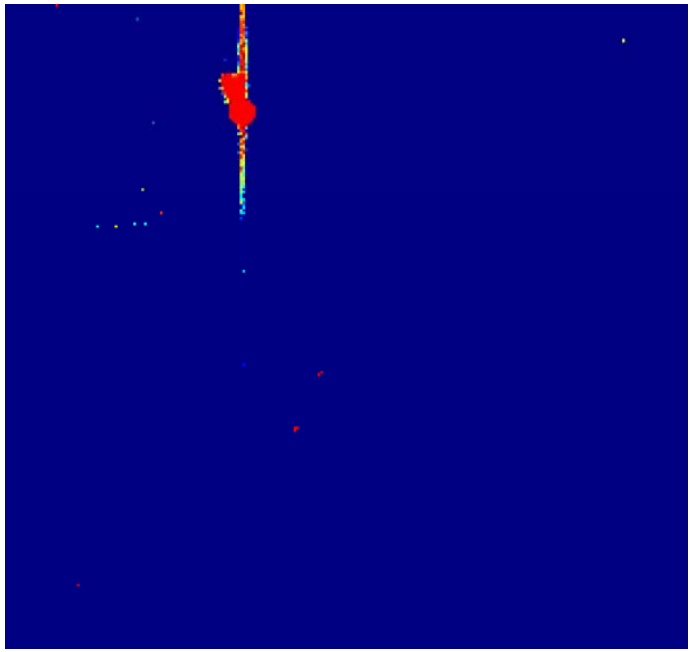
Resistivity vs ammonia flow

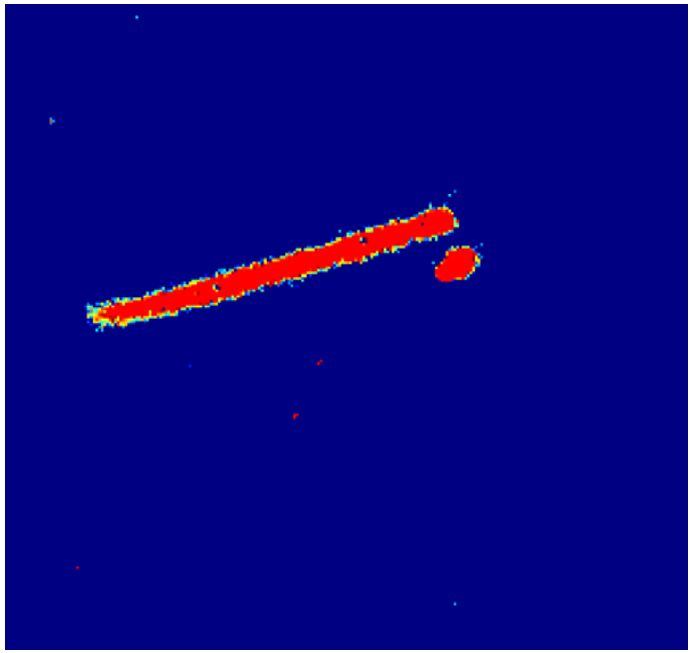
- Ammonia(NH_3)+silane (2 % SiH_4) diluted in N_2
- Ammonia/Silane ratio controls Si content and therefore resistivity



And it can withstand sparks

- Timepix covered with 7,2 μm SiRN
- Micromegas on top
- Ar/Iso 80/20, 520V on the grid and the chip does not want to die





Conclusions and future plans

- SiRN + InGrid close to become a standard
- GEMgrid = rock solid InGrid
- Next Quad can be done with InGrids
- Mass production

  -Chip squares will boost production

  -Collaborate with 8” wafer facilities

Thanks for your attention

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