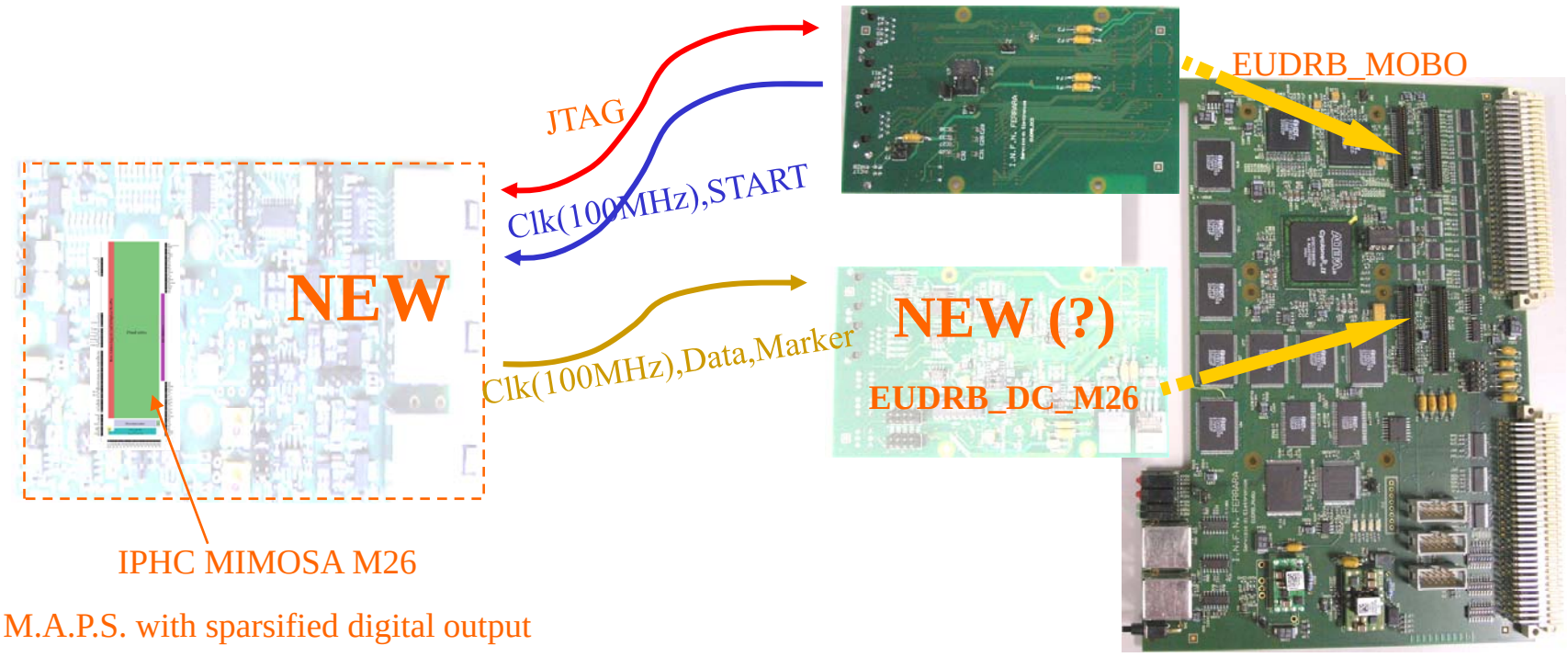


EUDRB: status report and plans for interfacing to the IPHC's M26

Summary:

- EUDRB developments in 2008
- Plans for interfacing the EUDRB to a new "proximity" card designed for the M26 sensor being developed at IPHC

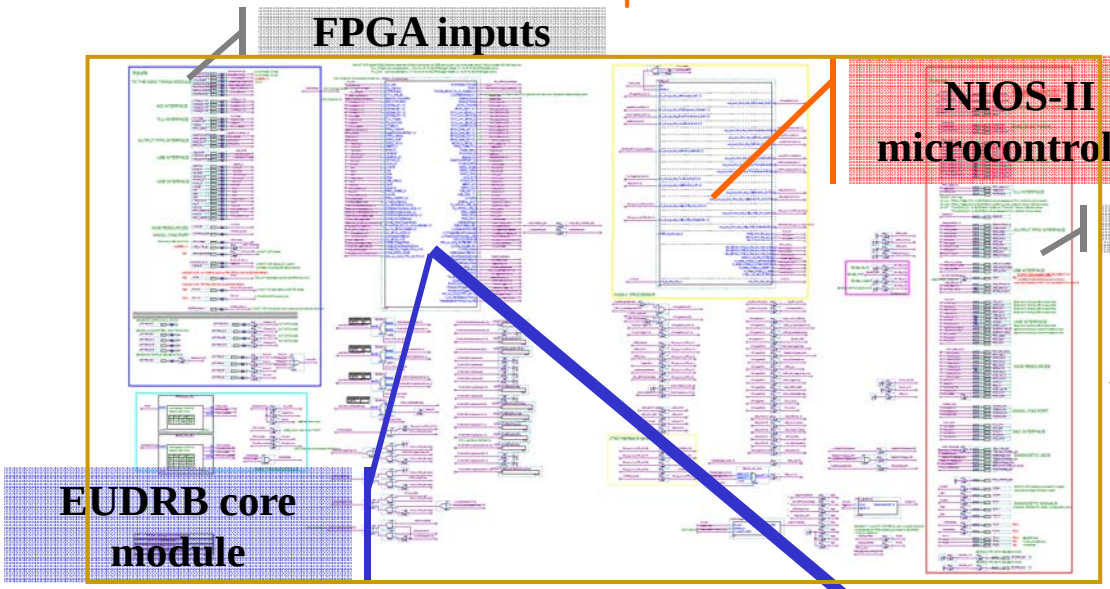
EUDRB developments in 2008: the EUDRB-MIMOx firmware

The "EUDRB-MIMOx" firmware was developed to:

- allow the EUDRB to read out the MIMOSA18 chip (256kpixels, high resolution sensor)
- allow full VME control of the parameters determining the sensor timing as well as the A/D converter timing and frame buffer size
- increase throughput by:
  - allowing overlapped readout and trigger processing operation of the EUDRB (capturing a new event can now start as soon as the previous event is stored in the output buffer)
  - implement a "rolling two frames" raw data format, to reduce the size of the non zero-suppressed events with respect to the previous "static three frames"
- re-style the FPGA design (VHDL and block diagram entries) to make it easier to read and maintain (as much as possible)

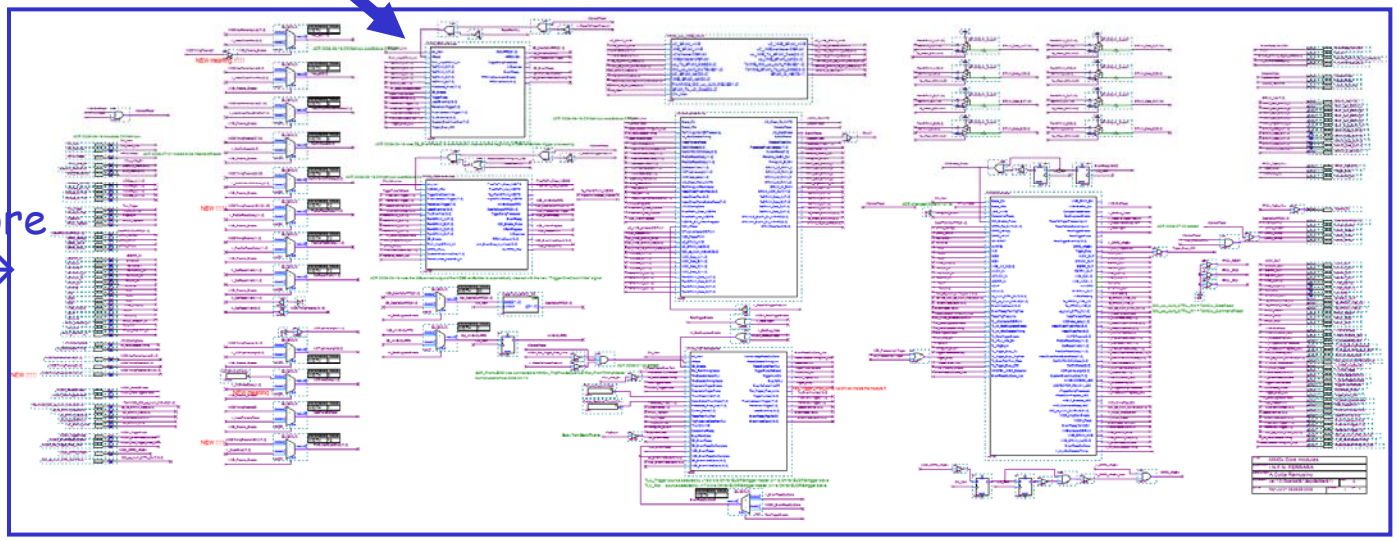
EUDRB: status report and plans for interfacing to the IPHC's M26

EUDRB developments in 2008: the EUDRB-MIMOx firmware



←EUDRB-MIMOx top level diagram

EUDRB-MIMOx core module diagram →



all lower levels of the "EUDRB-MIMOx core module" design are coded in VHDL

EUDRB: status report and plans for interfacing to the IPHC's M26

EUDRB developments in 2008: the EUDRB-MIMOx firmware

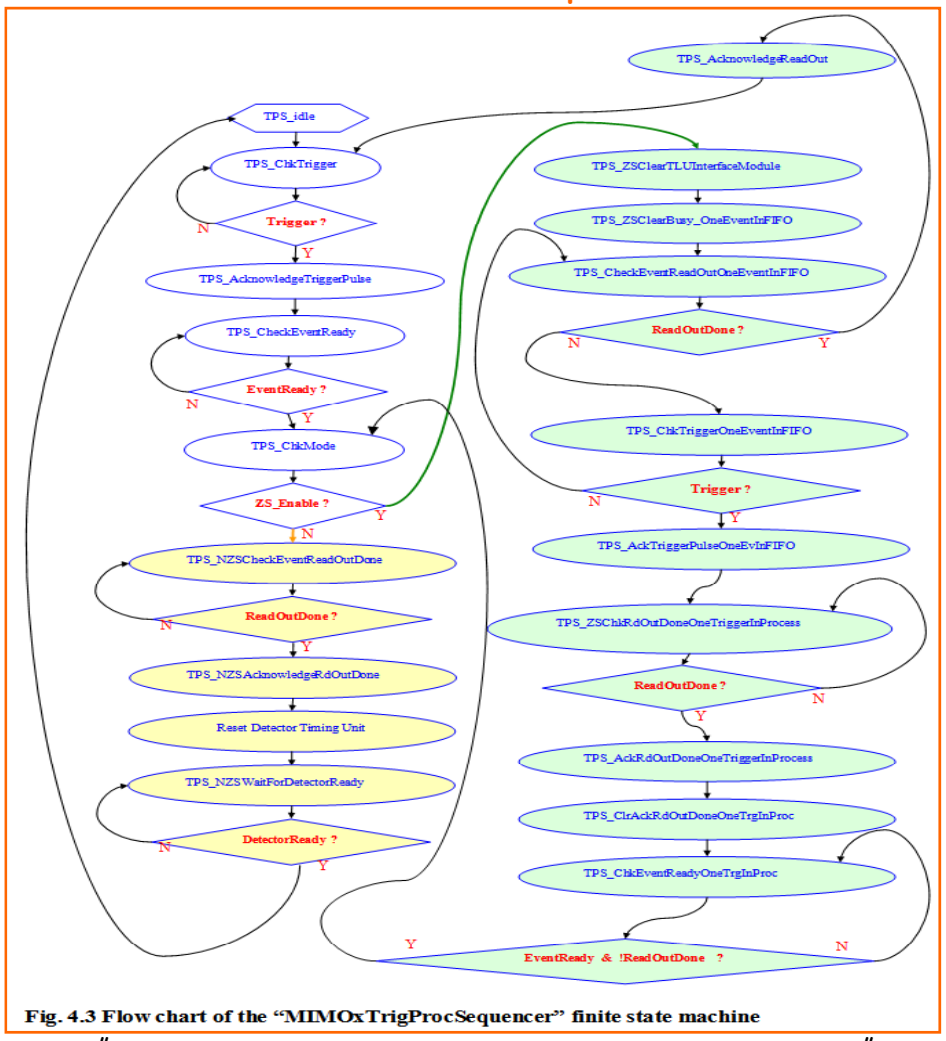


Fig. 4.3 Flow chart of the "MIMOxTrigProcSequencer" finite state machine

Source: "**The EUDET Data Reduction Board (EUDRB)** (firmware version EUDRB_MIMOx)" version 1.1 of Aug. 8th 2008, A. Cotta Ramusino INFN-FE

The "trigger processing sequencer" controls the overlapping of the sensor scan in response to a new trigger and the VME-MBLT readout of a previous event, both for Zero-Suppressed (green states) and Non Zero-Suppressed (yellow states) operation.

Decoupling the scan and the readout phase has allowed to achieve a trigger rate of about 100Hz in test beam operation with 6 boards in the crate.

While making the overlapped operation possible for EUDRB has improved things, the DAQ trigger rate is still below the goal ; the limitation is due to the idle time that the MVME6100 VME CPU spends while switching from MBLT to SINGLE CYCLE transfers (still under investigation)

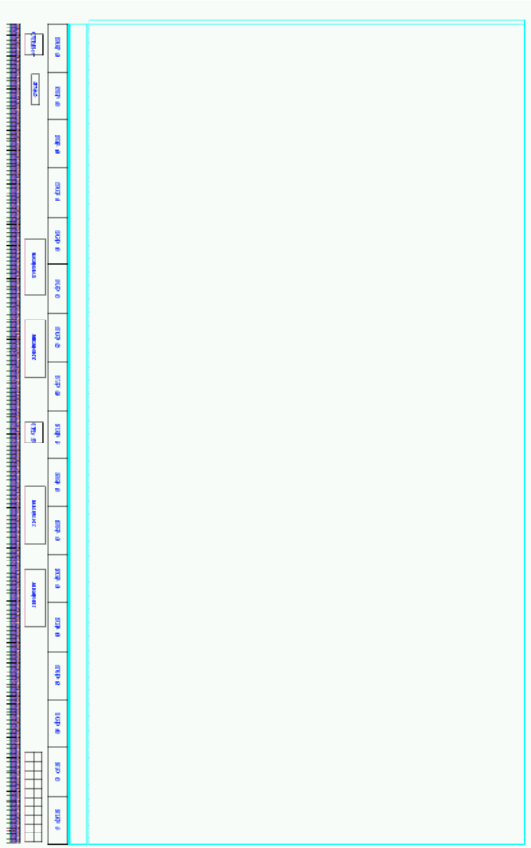
EUDRB: status report and plans for interfacing to the IPHC's M26

Plans for interfacing the EUDRB to the M26 sensor being developed at IPHC

MIMOSA 26 characteristics: summary

Autumn 2008 : fabrication of MIMOSA-26 = Final Sensor (TC)

- IDC/M-22 (binary outputs) complemented with ∅ (SDC-2/SUZE-01)
- best performing (rad. tol.) pixel architecture of IDC/M-22
  - ↪ wait for Octobre beam tests at CERN-SPS
- Active surface : 1152 columns of 576 pixels (21.2 x 10.6 mm^2)
- Pixel pitch : 18.4 μm ⟶ ∼ 0.7 million pixels
  - ↪ $\sigma_{sp} \gtrsim 3.5\ \mu m$ ⇛ pointing resolution $\lesssim 2\ \mu m$ on DUT surface
- Integration time ∼ 100 μs ⟶ ∼ 10^4 frames / second
- ∅ based on 18 groups of 64 columns and assuming ≤ 9 "clusters" per row
- Chip dimensions : ∼ 21 x 12 mm^2
- Data throughput: 1 output at ≥ 80 Mbits/s or 2 outputs at ≥ 40 Mbits/s
- Engineering run : 2 (+ ≤ 4) wafers of ≳ 30 chips expected (if yield ∼ 50 %)
- Design under way ⇛ planned submission date ≥ mid-November '08

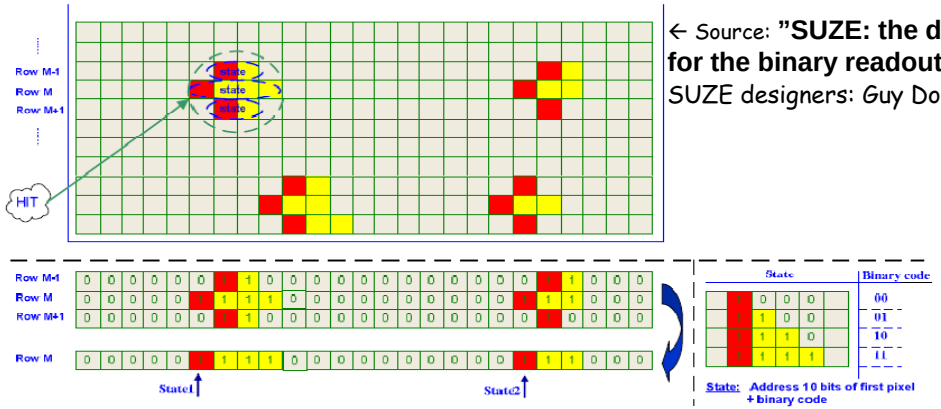


Source: " **Towards the Final Telescope Sensor:Status Report**", Marc Winter IPHC-Strasbourg, EUDET - JRA-1 – Final Telescope Sensor Progress Report, 1 September 2008

EUDRB: status report and plans for interfacing to the IPHC's M26

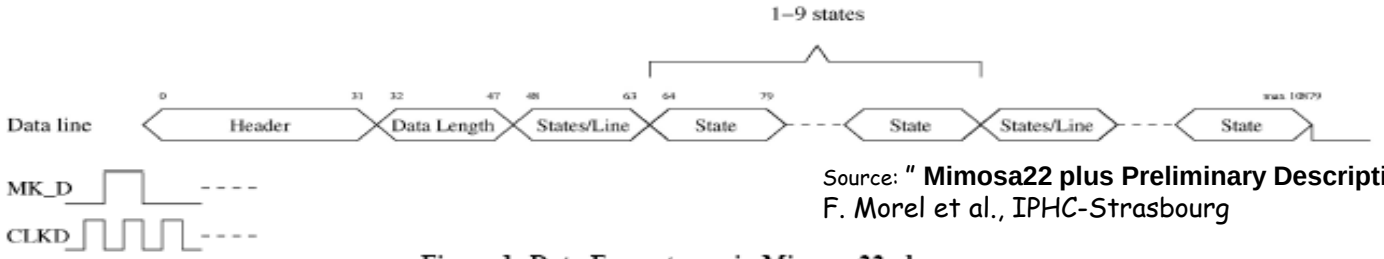
Plans for interfacing the EUDRB to the M26 sensor being developed at IPHC

MIMOSA 26 characteristics: PRELIMINARY output data format



← Source: **"SUZE: the demonstrator of data sparsification circuit for the binary readout MAPS",** Wojciech Dulinski on behalf of IPHC and SUZE designers: Guy Doziere and Abdelkader Himmi, IPHC-Strasbourg

Encoding of adjacent hit pixels in a row (up to four in one group) plus a common row address (if more than one state/row), means data compression but no real clustering.



Source: " **Mimosa22 plus Preliminary Description of the Serial Output** ", F. Morel et al., IPHC-Strasbourg

Figure 1: Data Format uses in Mimosa 22 plus

M26: 1152 columns of 576 pixels processed in groups of 18 columns

- data is sent at the beginning of each new frame, therefore the data frame is periodic.
- the different parts of the data frame are: Header (32bit), Data Length (16bit), States/Line (16bit), and State (16bit).
- the number of bits which could be sent between two headers is fixed; **the maximum number of bits sent after the next frame is 10880**

EUDRB: status report and plans for interfacing to the IPHC's M26

Plans for interfacing the EUDRB to the M26 sensor being developed at IPHC

HARDWARE PLAN (A):

• NO NEED TO BUILD A NEW DAUGHTER CARD:

! USE THE PRESENT J5 CONNECTOR ON THE EUDRB_DCD CARD which provides 4 spare LVDS inputs

CAVEATS of this solution:

• the outgoing LVDS signals 100MHz clock, and "Start" will be generated as single ended signals from the main FPGA and will have to cross the board-to-board connector to be converted into LVDS on the EUDRB_DCD digital daughter card

• the incoming LVDS signals 100MHz(50MHz) clock, 1 (2) data and "NewFrame" marker will be converted to single ended signals on the EUDRB_DCD card and will have to be transmitted as single ended signals to the main FPGA on the mother board: the reliability (concern with skewing) of this signal paths that cross the board-to-board connector between mother and daughter cards must be verified.

• only one MIMOSA26 sensor could be read by a EUDRB card

ADVANTAGES of this solution:

• cheaper (we have already enough EUDRBs to convert to MIMOSA26 readout and the conversion should involve only firmware changes)

• feasibility studies can start with the existent hardware

Plans for interfacing the EUDRB to the M26 sensor being developed at IPHC

ALTERNATIVELY: HARDWARE PLAN (B):

EUDRB_DC_M26 daughter card: in order to interface the EUDRB to the MIMOSA26 sensor it would be necessary to build a new daughter card to replace the present EUDRB_DCA analog daughter card.

The **EUDRB_DC_M26** will feature (in addition to the resources now present on the EUDRB_DCA to provide synchronous operation across the pool of EUDRBs in the DAQ system):

- LVDS receivers for the (100MHz / 50MHz) serial links (data lines and strobes) driven by the MIMOSA26
- a small, fast FPGA of the Cyclone III family, providing resources for:
  - de-serialization of the input stream(s) and temporary storage of the frame data received from the sensor pending the transfer to the mother board
  - transferring the data collected for each new frame to the main memory on the mother board (EUDRB_MOBO), using the parallel data path now used for the A/D converter data
  - diagnostics

ADVANTAGES of this solution:

→ **more sensors (possibly up to 3, due to space limitation at the front panel of EUDRB) could be read out by accessing a single EUDRB card.** A patch card would be needed to fanout the signals 100MHz clk and "START" to three detectors unless such "fanout" is already provided by the sensor developers

→ **higher efficiency in the VME readout due to the limited need of switching between burst read accesses and single cycle transfers**

EUDRB: status report and plans for interfacing to the IPHC's M26

Plans for interfacing the EUDRB to the M26 sensor being developed at IPHC

FIRMWARE UPGRADE PLAN:

The **EUDRB_MIMOx** firmware will need upgrading to account for the different data handling needed when reading out a MIMOSA26 sensor.

The new **EUDRB_M26_FW** firmware will:

- de-serialize the input data in case of adoption of hardware plan (A)
- provide temporary storage (on FIFO memories embedded in the FPGA) for at least two frames, pending the trigger request
- Build, in response to a trigger request, an event data packet with header and trailer (similar to the ones currently used)
- transfer the event in the output FIFO (external to the FPGA)
- control the transfer of the events buffered in the output FIFO over the VME backplane

EUDRB: status report and plans for interfacing to the IPHC's M26

Plans for interfacing the EUDRB to the M26 sensor being developed at IPHC

MILESTONES AND COSTS FOR UPGRADING THE EUDRB to readout the MIMOSA26 sensor:

Setting milestones for the upgrade would require the final information on the characteristics of the sensor proximity cards which are expected soon from the sensor developers at IPHC.

Such information would have bearing on schedule and costs because it would determine:

- whether or not "patch cards" are needed to adapt to the final choice of connectors / pinouts
- whether each EUDRB would have to individually clock each sensor proximity card or a "timing signal fanout" will be made available by the sensor designers

Milestones and cost estimates (based on current informations):

Assuming some passive patch card is needed but hardware plan (A) is followed::

- end Oct. 2008: reliability of 100MHz link from EUDRB_DCD (100Mhz clk+Start OUTPUT; 100MHz(50MHz) Clk, 1 (2) data, "NewFrame" marker INPUT) assessed
- end Feb. 2009: new **EUDRB_M26_FW** ready for field tests
- cost ≈ 3K€ for patch cards

Assuming hardware plan (B) is followed:

- end of Jan 2009: **EUDRB_M26_DC** ready for testing
- end of Apr 2009: new **EUDRB_M26_FW** ready for field tests
- cost ≈ 3K€ for patch cards needed for clock fanout
- cost ≈ 9K€ for **EUDRB_M26_DC** layout and production of 5 boards (capable of multiple sensor readout)