

Towards the Final Telescope Sensor

Progress Report

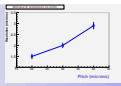
Marc Winter (IPHC-Strasbourg)

on behalf of IPHC and IRFU/Saclay

(contribution from A.Bulgheroni)

OUTLINE

- Strategy of the chip development (reminder)
- Col. // sensor prototyping : *Objectives of IDC/MIMOSA-22 prototyping – Lab & beam test results*
- The question of radiation tolerance
- Status of MIMOSA-22bis : *Differences with IDC/MIMOSA-22 – Preliminary test results*
- Final chip : status of design and plans
- Summary - Outlook

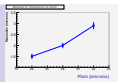


■ Specific goals of IDC/MIMOSA-22 :

- ⇒ *validate the fast read-out architecture developed in MIMOSA-16 (next slide) at **Real Scale***
- ⇒ *extract an optimal pixel design (sensing diode and signal processing μ .circuits)*
- ⇒ *improve the chip testability (JTAG, analog outputs, pads, ...)*

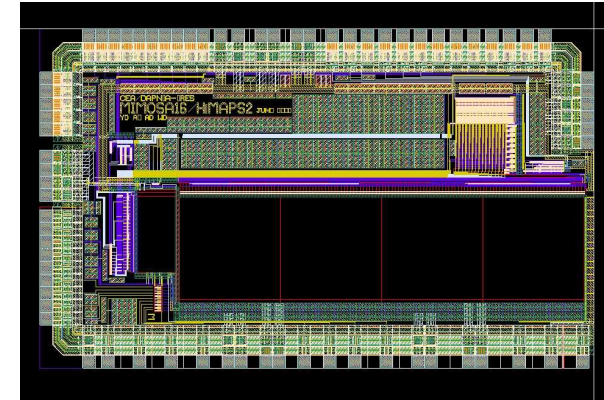
■ Objective beyond IDC/MIMOSA-22 :

- ⇒ *once validated, the IDC/MIMOSA-22 architecture will be merged with SDC-2/SUZE-01*
 - ⇒ *Final Sensor (TC/MIMOSA-26), to be sent for fabrication in Autumn*



Performances of a Small Prototype with Digitised Output

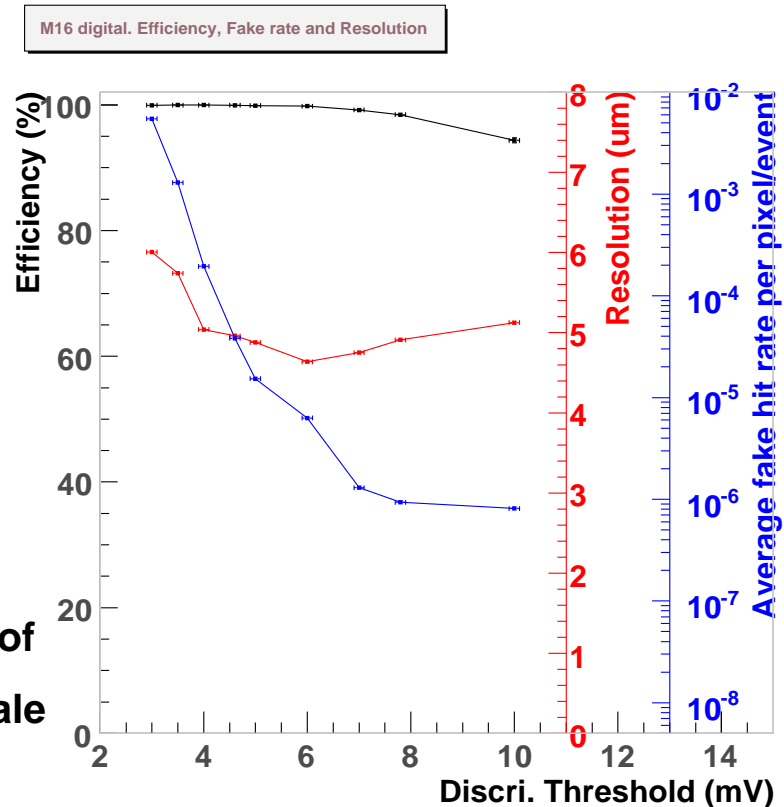
- MIMOSA-16 :
 - ◇ fabricated in 2006 (coll. with IRFU/Saclay)
 - ◇ 32 col. of 128 pixels (25 μm pitch, integrated CDS)
 - ◇ 24 col. ended with an integrated discriminator
 - ◇ 4 different pixels (i.e. 4 sub-arrays)



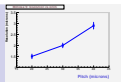
■ Tests at CERN-SPS ($\sim 180 \text{ GeV } \pi^-$) in Summer 2007

→ results of one sub-array (S4)

Discri. threshold	Detection eff.	Fake rate	Resolution
4 mV	$99.96 \pm 0.03 \text{ (stat) } \%$	$\sim 2 \cdot 10^{-4}$	$\sim 4.8 - 5.0 \mu m$
6 mV	$99.88 \pm 0.05 \text{ (stat) } \%$	$< 10^{-5}$	$\sim 4.6 \mu m$



▷▷▷ Architectures of pixel (integrated CDS) and of full chain made of "columns ended with integrated discri. " validated at small scale



■ Topics investigated :

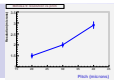
- ✧ *optimum between CCE (\Rightarrow large diode) and capacitive noise (\Rightarrow small diode)*
- ✧ *effective and robust pre-amplification scheme*
- ✧ *low noise (ionising) radiation tolerant design*
- ✧ *temperature dependence of performances*
- ✧ *performance uniformity over full active surface*
- ✧ *comparison with MIMOSA-16 performances (24 columns of 128 pixels)*

■ 5 pixel designs implemented, combining 2 reset & 2 ampli. variants (w/o rad. tol. diode, diff. diode sizes):

- ✧ *reset diode with (standard) common source amplifier : w/o improved gain*
- ✧ *self-biased feedback diode with common source amplifier with improved gain*
- ✧ *feedback reset diode with common source amplifier : w/o improved gain*

■ Status :

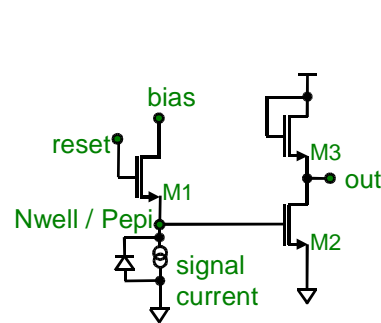
- ✧ *back from foundry since Feb.'08*
- ▷ *lab tests of analog and digital (discr.) outputs with ^{55}Fe source completed*
- ▷ *first beam tests (CERN-SPS / August '08) analysed*



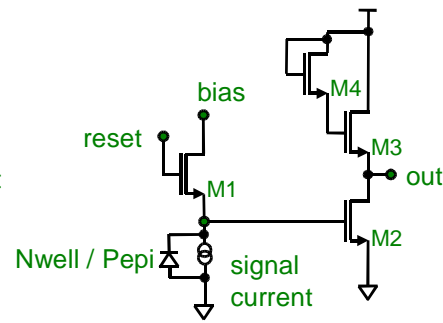
Various pixel designs (rad. tol. and standard) :

✧ *reset diode (improved gain)*

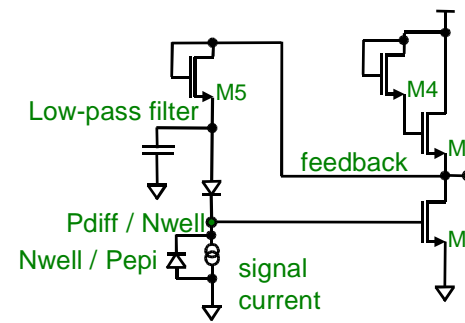
✧ *self-biased diode with feedback (improved gain)*



(S13)



(S10)



(S6)

Main results obtained with exposure to ^{55}Fe source ($t_{r.o.} = 92.5 \mu\text{s}$) :

✧ *Noise :*

≈ *Temporal (pixel) Noise* $\sim 0.5 - 0.7 \text{ mV}$ ($10 < N < 14 e^- \text{ ENC}$)

≈ *FPN* $\sim 0.25 \text{ mV}$

≈ *N (rad. tol. pixels)* $\sim N$ (*standard pixels*) $+ 1 e^- \text{ ENC}$

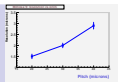
✧ *Cluster CCE :*

≈ *3x3 pixels* : 70 – 80 %

≈ *5x5 pixels* : 80 – 90 %

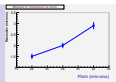
✧ *modest T dependence between* $\sim 10^\circ \text{C}$ *and* 35°C : $\lesssim 10\%$ *noise variation*

✧ *5 different chips characterised : identical performances within* $\pm 5\%$

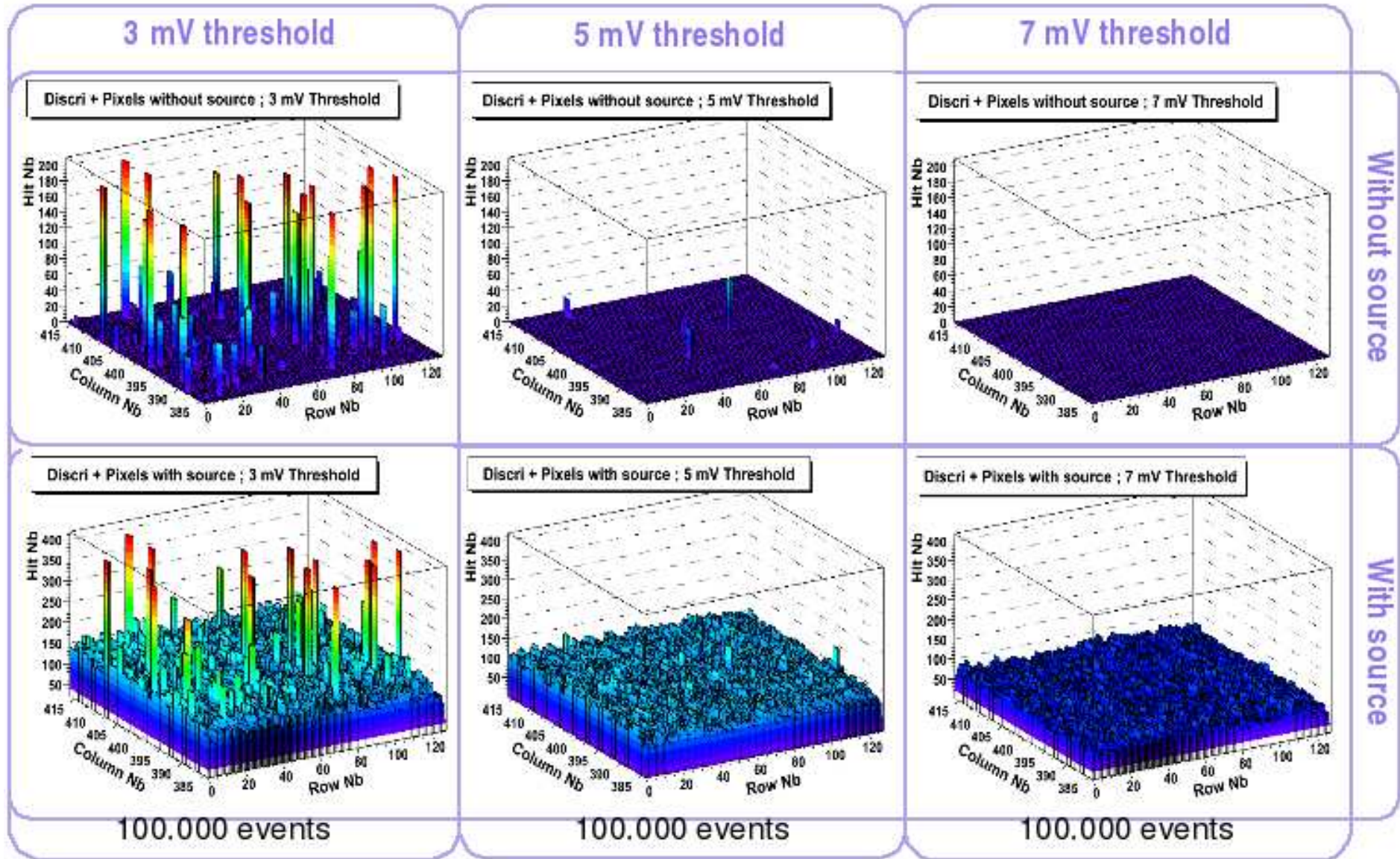


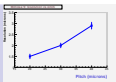
	S6		S7		S8		S9		S10	
	mV	e-	mV	e-	mV	e-	mV	e-	mV	e-
TN	0.612	11.5	0.601	10.7	0.615	11.3	0.595	10.0	0.639	11.6
FPN	0.250	4.7	0.263	4.6	0.254	4.4	0.273	4.6	0.222	4.0
	S12		S13		S15		S16		S17	
	mV	e-	mV	e-	mV	e-	mV	e-	mV	e-
TN	0.636	11.2	0.692	13.4	0.682	12.8	0.536	12.4	0.527	11.4
FPN	0.225	4.0	0.269	5.2	0.277	5.2	0.218	5.1	0.217	4.7

- Pixel Noise ~ 0.6mV
 - FPN ~ 0.25 mV
 - RadTol pixels (S6, S10, S13) Noise slightly higher than for standard pixels
- ⇒ Similar results than smaller prototype MIMOSA16 ones

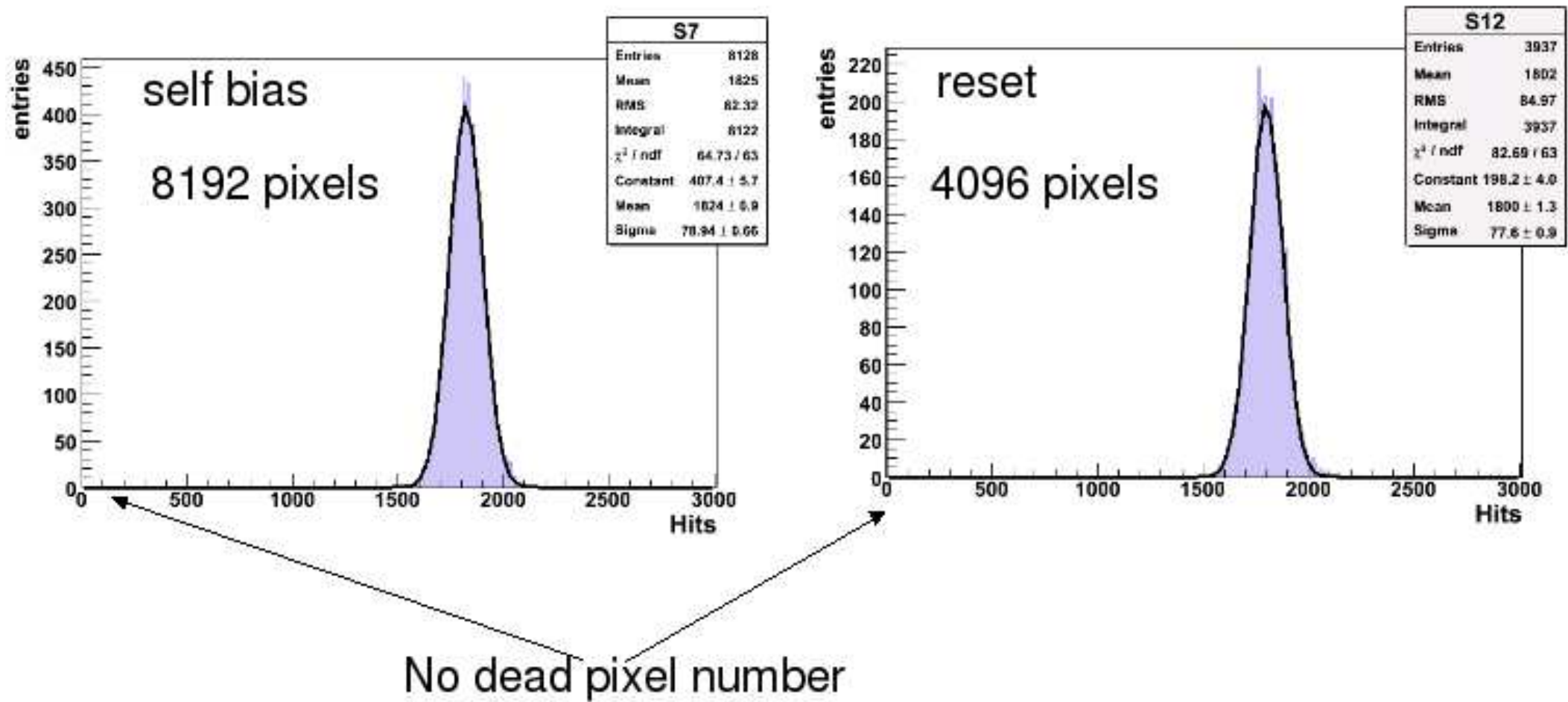


S12 response for 3, 5 and 7 mV threshold without and with ⁵⁵Fe source

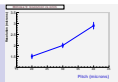




5 mV threshold with ^{55}Fe source



Good uniformity of discriminator response, within 4%



4 weeks of beam time at CERN-SPS :

- ▷ ~ 2 weeks in August with MIMOSA-22 (EUDET period)
- ▷ ~ 2 weeks in Sept.-Oct. with MIMOSA-22bis (SiLC period)

T4-H6 beam line : ~ 120 GeV π^- beam

▷▷▷▷

Chips mounted at center of Si-strip telescope

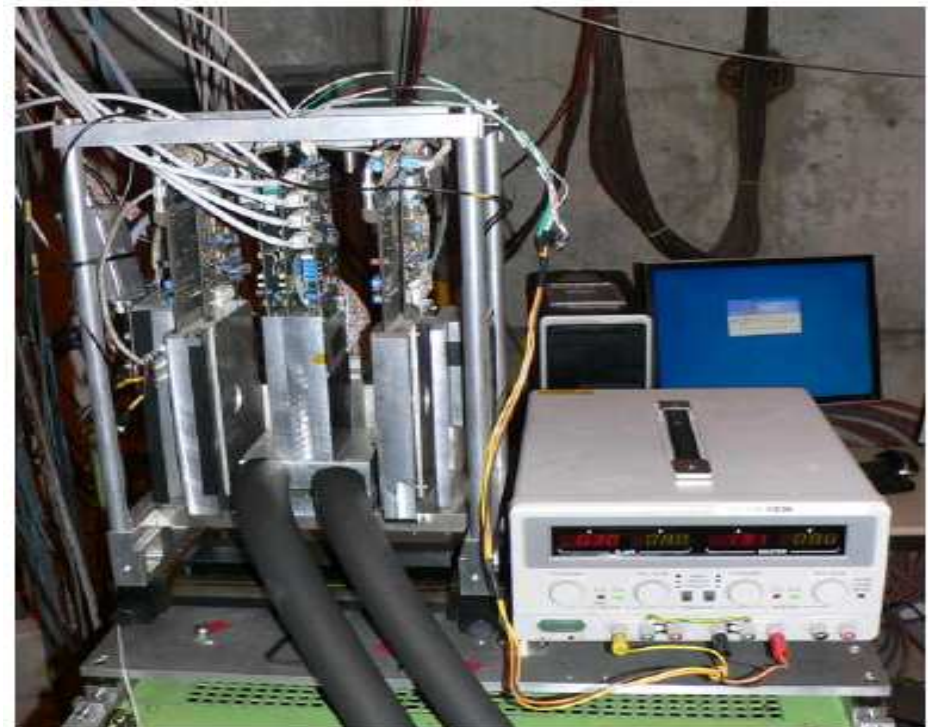
(4 pairs of orthogonal strips)

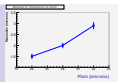
▷▷▷▷

6 chips tested at various discri. threshold values:

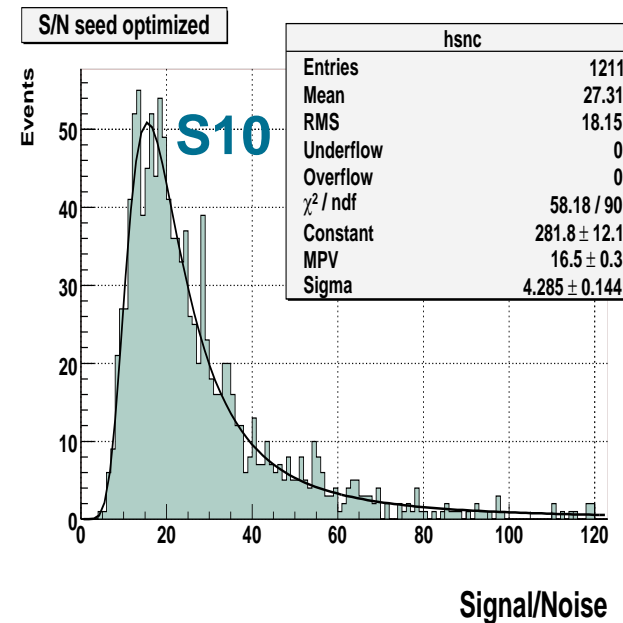
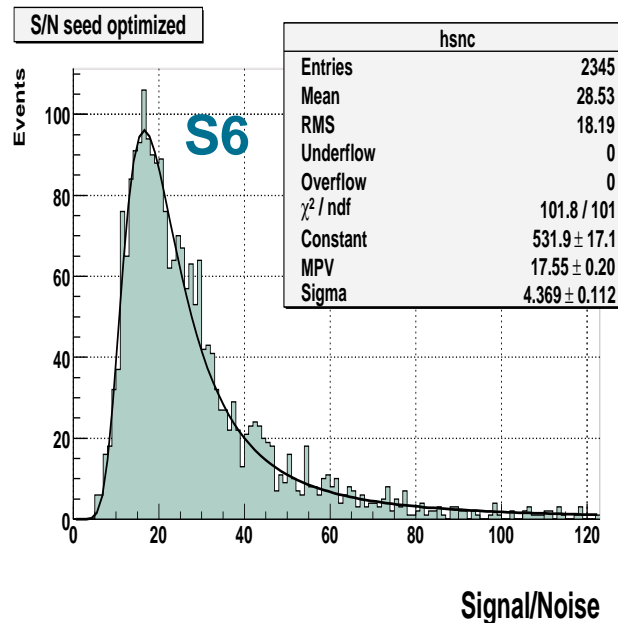
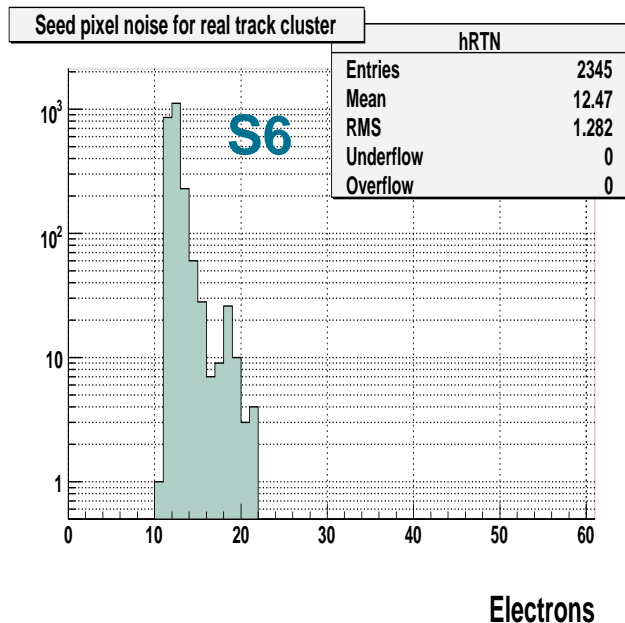
- ▷ 2 MIMOSA-22 : 0 & 150 kRad
- ▷ 4 MIMOSA-22bis : 0, 150 & 300 kRad, $6 \cdot 10^{12} n_{eq}/cm^2$

> 1 million tracks reconstructed in the sensors





Noise and S/N (seed pixel) distributions delivered by the 8 columns without discriminator

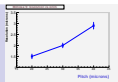


Detection performances (det. eff. , N and S/N for hits where the seed pixel exhibits $S/N > 4$) :

Sub-array	S6	S7	S8	S9	S10	S12	S13
Det. eff.	99.93 % ± 0.05 %	99.95 % ± 0.04 %	100.00 % +0/-0.30 %	100.00 % +0/-0.14 %	99.87 % ± 0.09 %	100.00 % +0/-0.08 %	100.00 % +0/-0.07 %
N (e^- ENC)	12.5 ± 0.1	11.6 ± 0.1	12.3 ± 0.1	10.6 ± 0.1	13.6 ± 0.1	12.1 ± 0.1	14.0 ± 0.1
S/N (seed, MPV)	17.6 ± 0.2	18.5 ± 0.2	20.9 ± 1.1	19.5 ± 0.5	16.5 ± 0.3	18.2 ± 0.3	16.0 ± 0.3

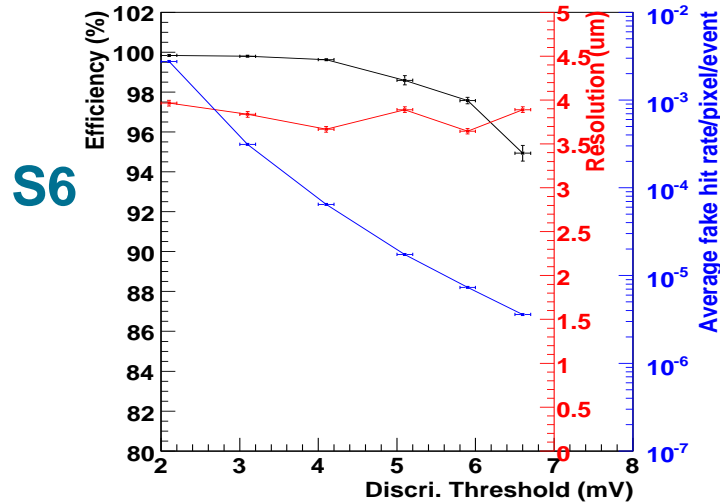
✳ very satisfactory performances (det. eff. ~ 99.9 % and single pt resolution $\lesssim 1.5 \mu m$)

⇒ pixel architecture (diode size, rad. tol. diode design, amplification scheme) validated

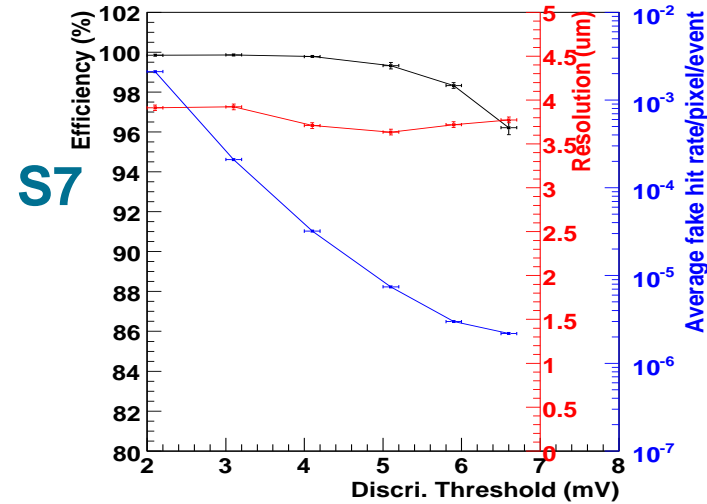


Det. efficiency, fake hit rate & single pt resolution for S6, S7, S12, S13 vs discri. threshold :

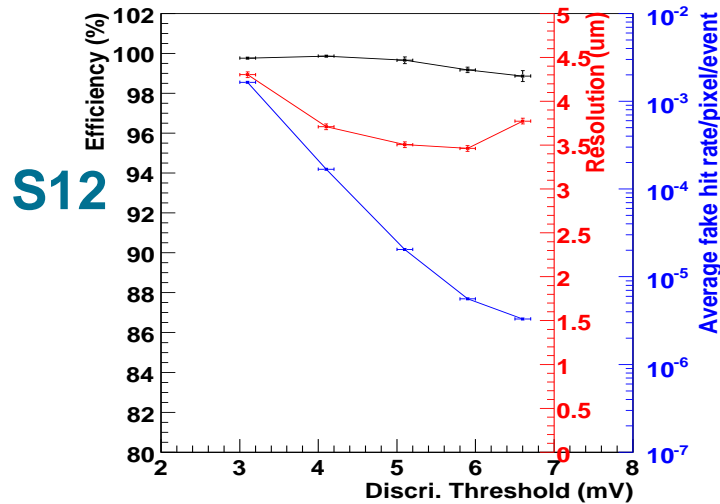
M22 digital S6. Efficiency, Fake rate and Resolution



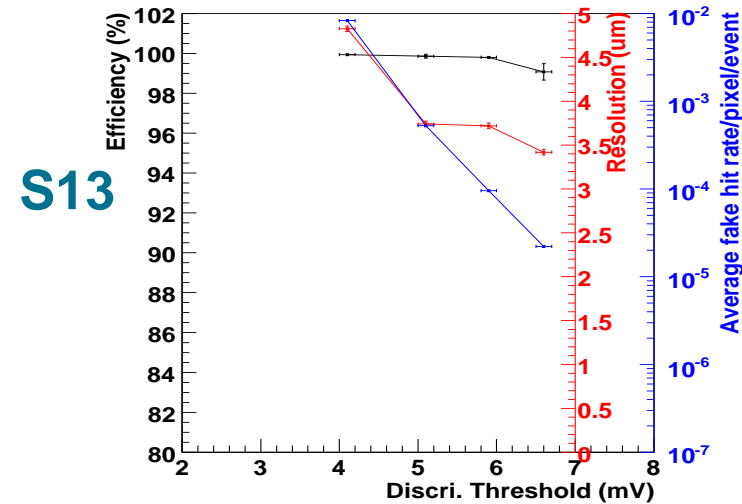
M22 digital S7. Efficiency, Fake rate and Resolution



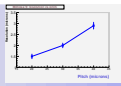
M22 digital S12. Efficiency, Fake rate and Resolution



M22 digital S13. Efficiency, Fake rate and Resolution

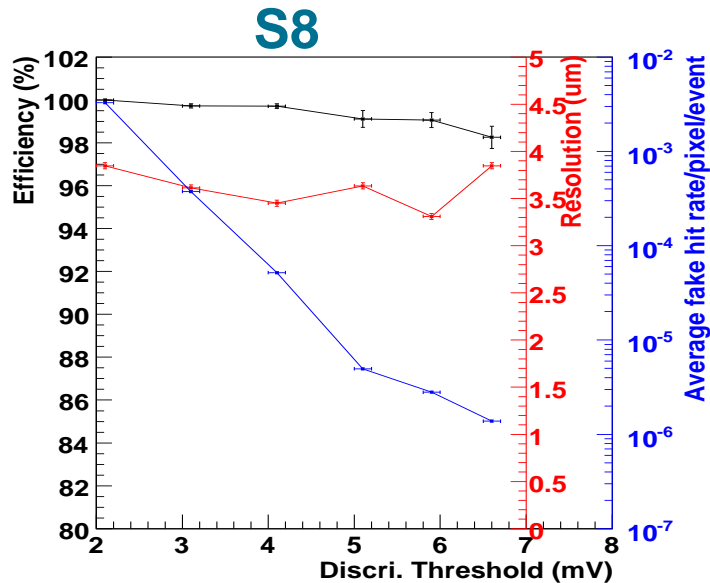


▷ ▷ ▷ Detection efficiency \gtrsim 99.8 % for all (rad. tol. and standard) pixel architectures !!!

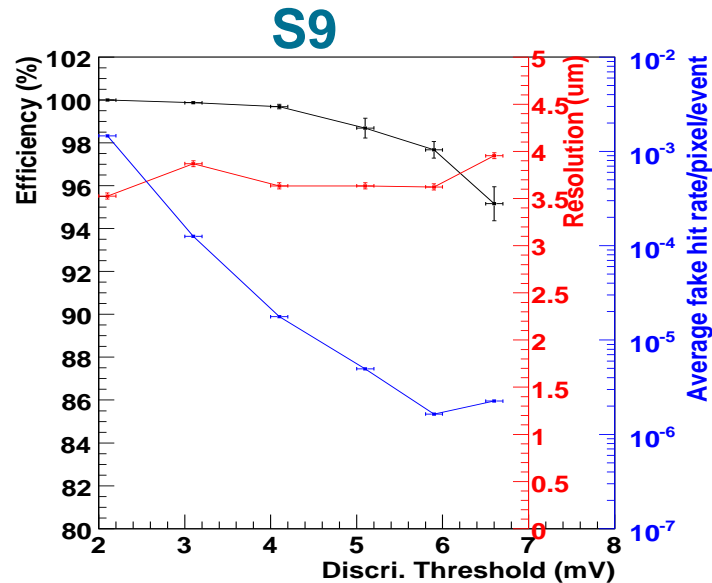


Detection efficiency, fake hit rate & single pt resolution for S8, S9, S10 vs discri. threshold :

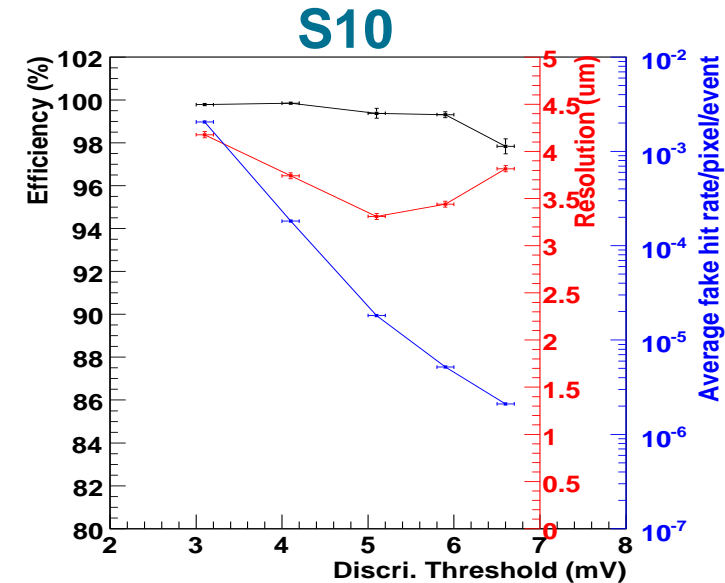
M22 digital S8. Efficiency, Fake rate and Resolution



M22 digital S9. Efficiency, Fake rate and Resolution

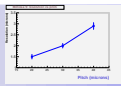


M22 digital S10. Efficiency, Fake rate and Resolution

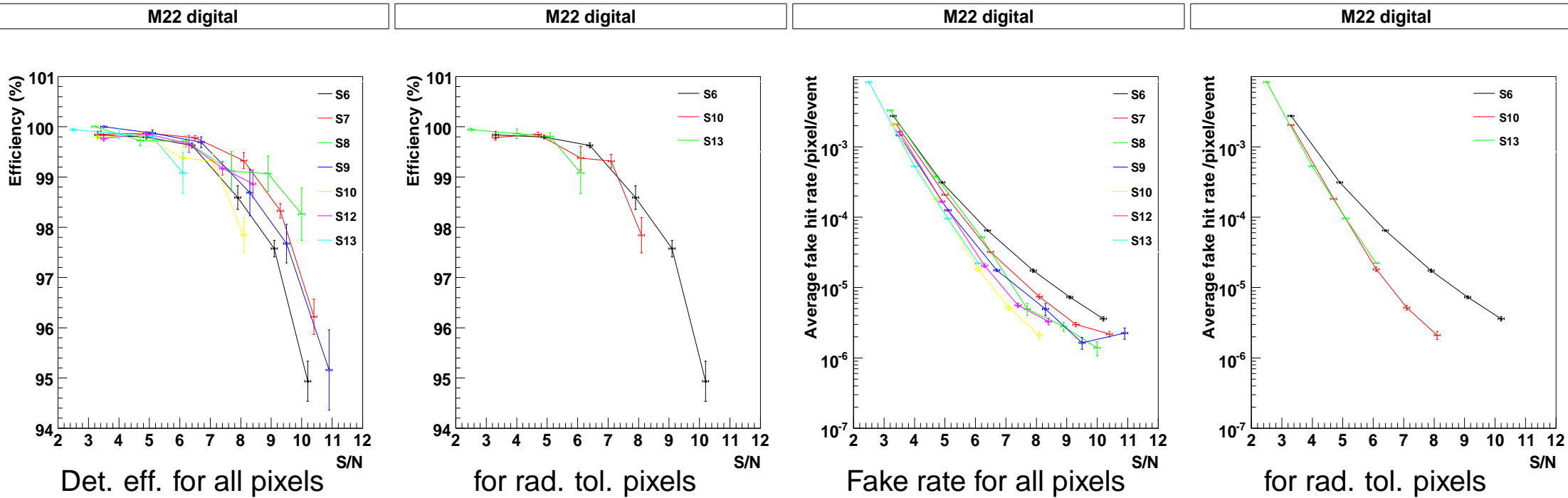


Main results:

- * rather marginal performance differences between the 7 sub-arrays (e.g. rad. tol. vs standard)
- * det. eff. of analog output $\sim 99.9\%$ for all sub-arrays \Rightarrow pixel architecture validated
- * det. eff. of digital output $\gtrsim 99.8\%$ for all 7 sub-arrays (agrees with MIMOSA-16)
- * fake hit rate seems larger than for MIMOSA-16 but acceptable : $O(10^{-4} - 10^{-5})$
- * single point resolution $\gtrsim 3.5 \mu\text{m}$ (as expected)
- * no performance non-uniformity observed over the chip surface \Rightarrow real scale check validated

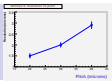


■ Comparison of det. efficiency & fake hit rate vs S/N for all sub-arrays (prelim.) :



▷ Observed performance differences (& analysis maturity) don't allow deciding for a given pixel archi.

- ⇒ Wait for :
- * more sensors tested
 - * MIMOSA-22bis performances
 - * more beam tests
 - * radiation tolerance studies



Why may radiation tolerance be a concern ?

- * max. annual doses at DESY $\lesssim 10^{11} e^-$ (few GeV)/yr $\Rightarrow \lesssim 3.5 \text{ kRad} \& 10^{10} n_{eq}/\text{cm}^2$
- * max. annual doses at CERN \lesssim several $10^{12} \pi^-$ (10^2 GeV)/yr $\Rightarrow \lesssim O(10^2) \text{ kRad} \& O(10^{12}) n_{eq}/\text{cm}^2$

Assessing radiation tolerance (10 keV X-Rays):

* Noise of IDC/M-22 (S6) at 20°C :

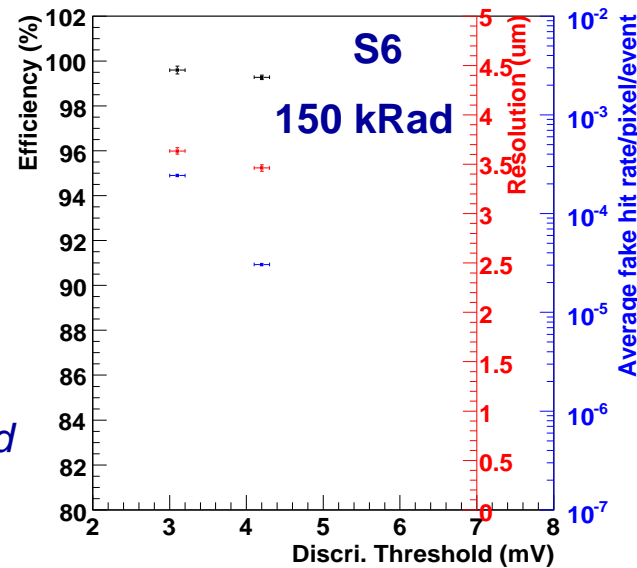
- $\sim 12.5 e^- \text{ ENC}$ before irradiation
- $\sim 16 e^- \text{ ENC}$ after 150 kRad \rightarrow
- $\sim 18 e^- \text{ ENC}$ after 300 kRad

- * New design (MIMOSA-22bis) fabricated
 ▷ tests in Sept.–Oct. (lab, SPS)

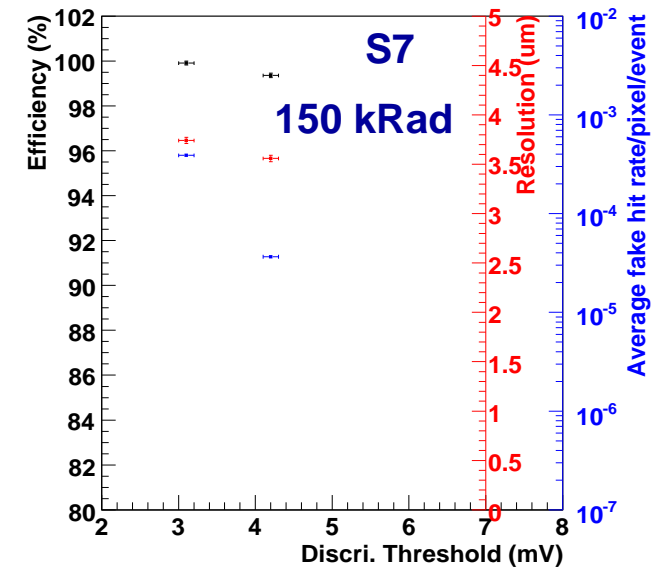
- * MIMOSA-22 non-ionising radiation tolerance assessment under way with fluences of $3 \& 6 \cdot 10^{12} n_{eq}/\text{cm}^2$

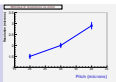
- * Latch-up tests of SDC-2/SUZE-01 foreseen in Octobre

M22 digital S6 (150kRad). Efficiency, Fake rate and Resolution



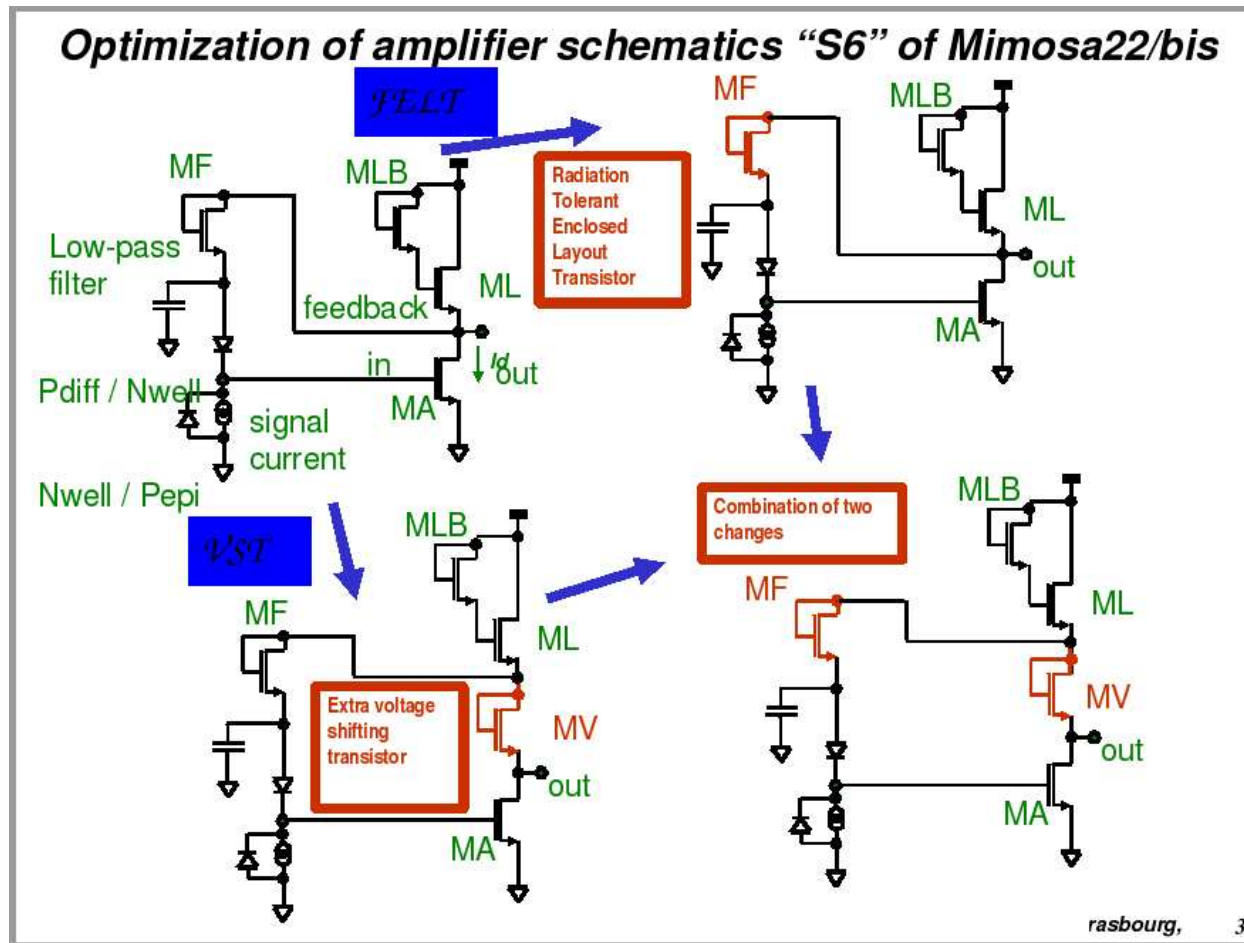
M22 digital S7 (150kRad). Efficiency, Fake rate and Resolution

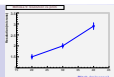




Main objectives of the MIMOSA-22bis prototype :

- ✧ check robustness of pixel operation against steering parameter values (e.g. T dimensions)
- ✧ optimise combination of parameters driving S/N value (e.g. coll. diode dimensions)
- ✧ optimise design against ionising radiation damage (e.g. enclosed T)





Lab test results :

▷ ex. of S6 (M22) variants at 20° C

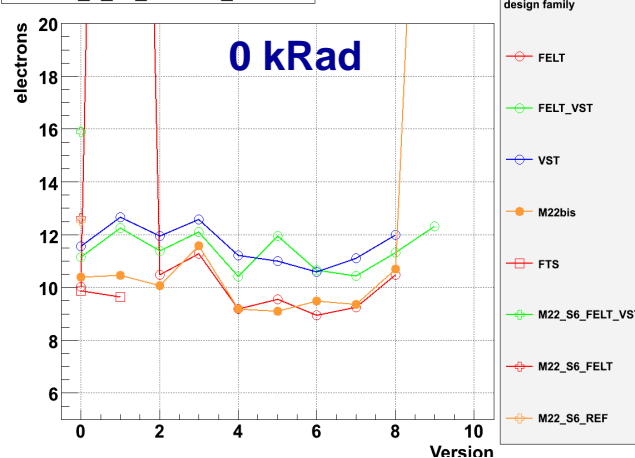
* before irradiation $\gtrsim 9.5 e^- ENC$

* after 50 kRad $\gtrsim 11 e^- ENC$

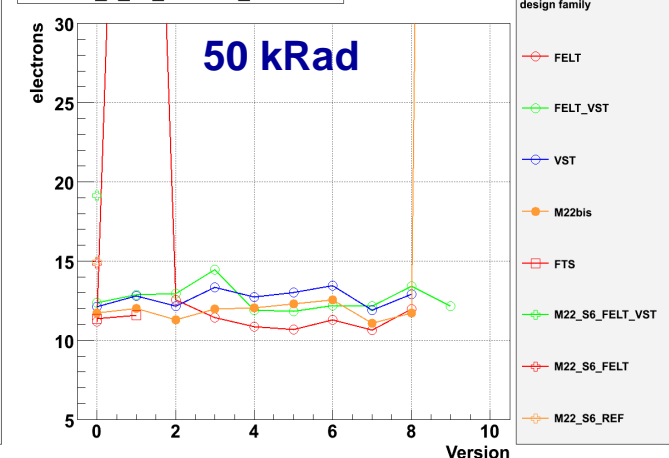
* after 150 kRad $\gtrsim 13 e^- ENC$

* after 300 kRad $\gtrsim 15 e^- ENC$

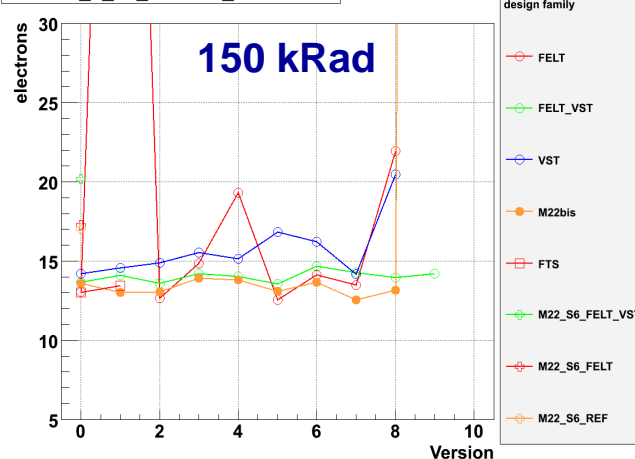
total_n_e_vs_Version_0kRad



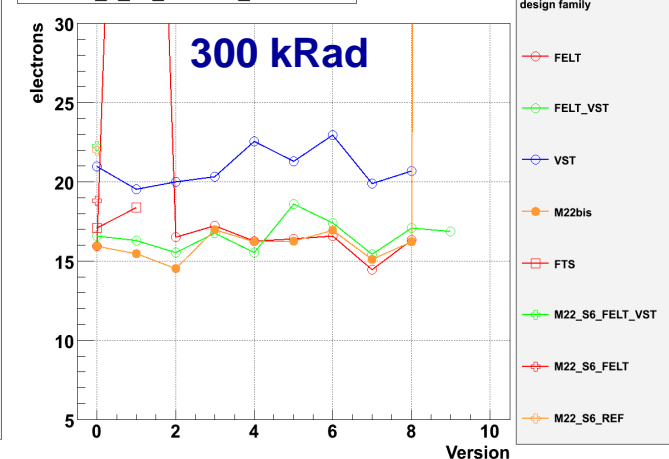
total_n_e_vs_Version_50kRad



total_n_e_vs_Version_150kRad



total_n_e_vs_Version_300kRad

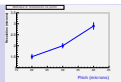


A. Dorokhov, IPHC, Strasbourg, 12

▷▷▷ Excellent stability of circuit behaviour against parameter variations

▷▷▷ Excellent noise performance

(... watch CCE ...)

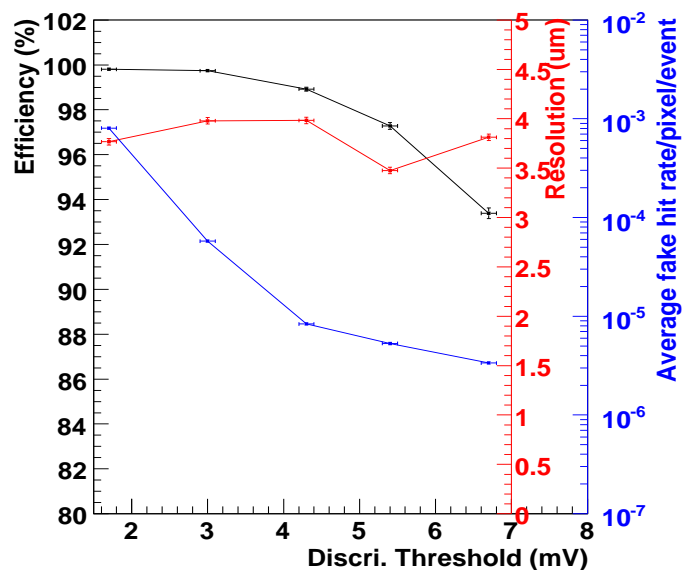


Data collected at CERN-SPS (T4–H6) during SiLC period (Sept. 24 – Oct. 6):

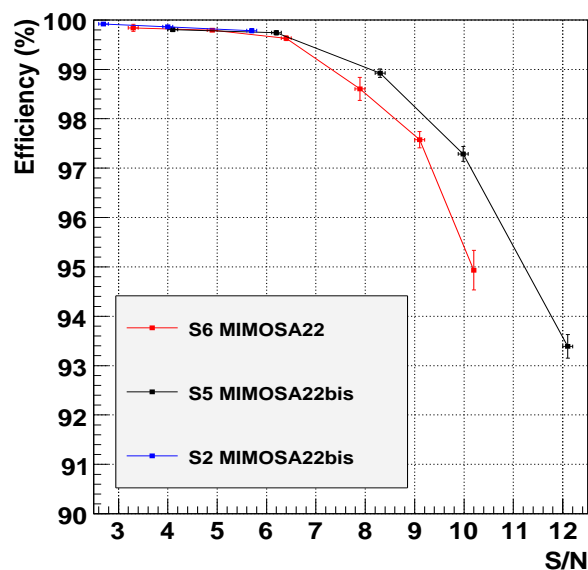
- ✧ 1 non-irradiated chip tested at 20° C
- ✧ 1 chip irradiated with 150 kRad tested at 20° C and 35° C
- ✧ 1 chip irradiated with 300 kRad tested at 20° C
- ✧ 1 chip irradiated with $6 \cdot 10^{12} n_{eq}/cm^2$ at 20° C

Beam test results (ex. of S6 (M22) variants):

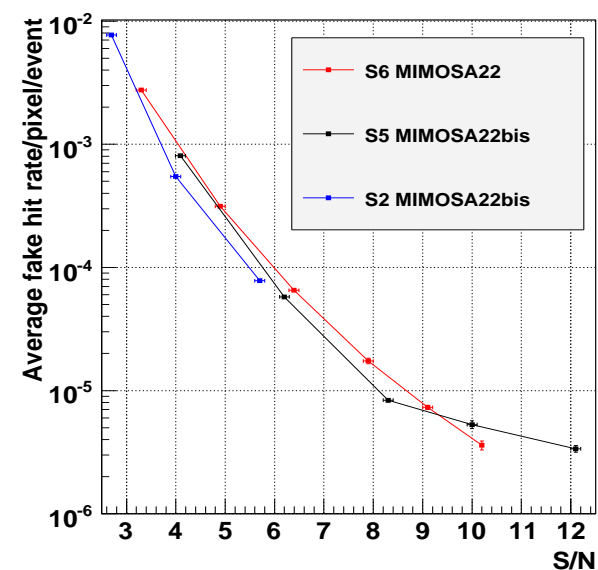
M22bis digital S5. Efficiency, Fake rate and Resolution



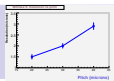
S6 M22, S5 M22bis & S2 M22bis digital Efficiency



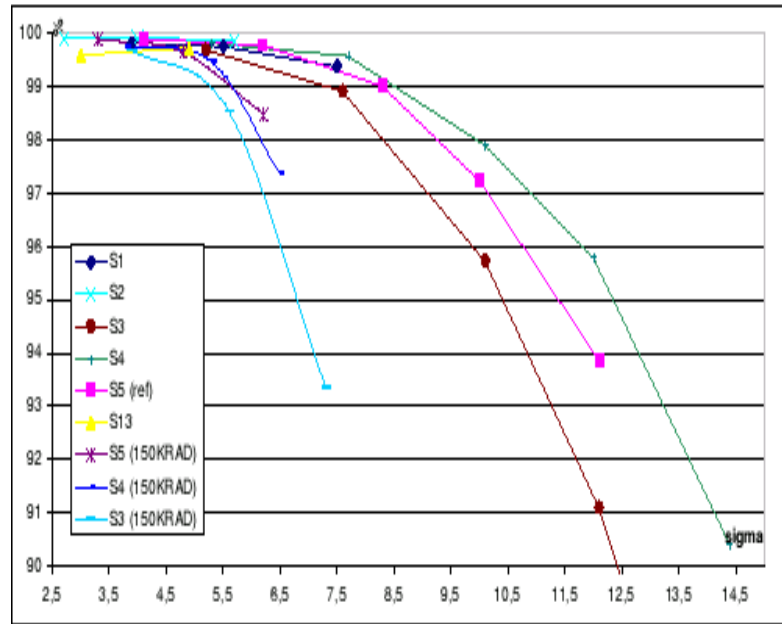
M22bis digital fake hit rate



▶▶▶ Performances of reference sub-array in MIMOSA-22 (S6) and -22bis (S5) are identical



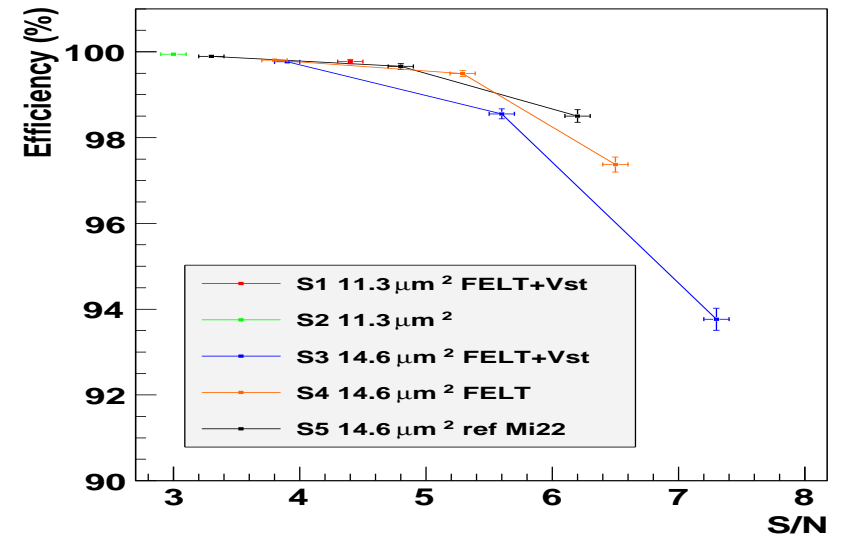
Beam test results with chips irradiated with 150 kRad :



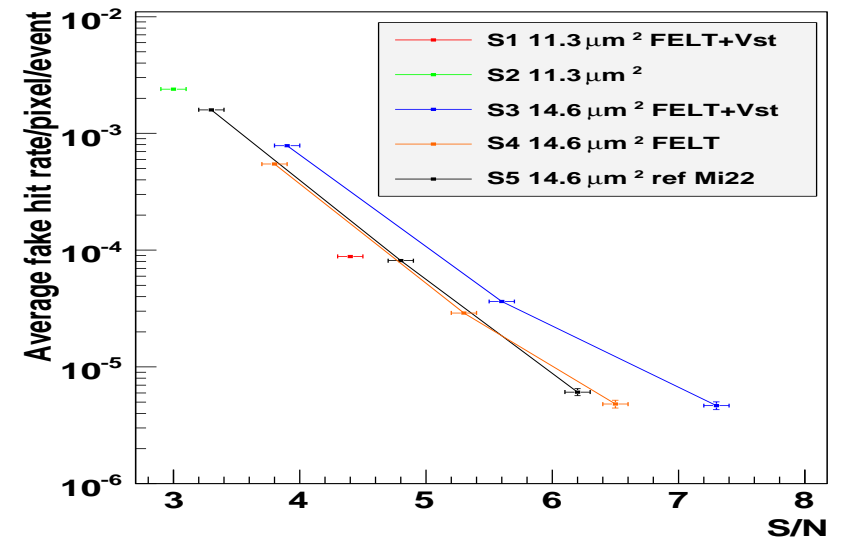
Det. eff. vs SNR before and after irradiation (150 kRad)

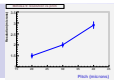
▶▶▶ Pixel & column parallel architecture
with integrated discriminators
Fully Validated !!!

M22bis digital Efficiency after 150kRad



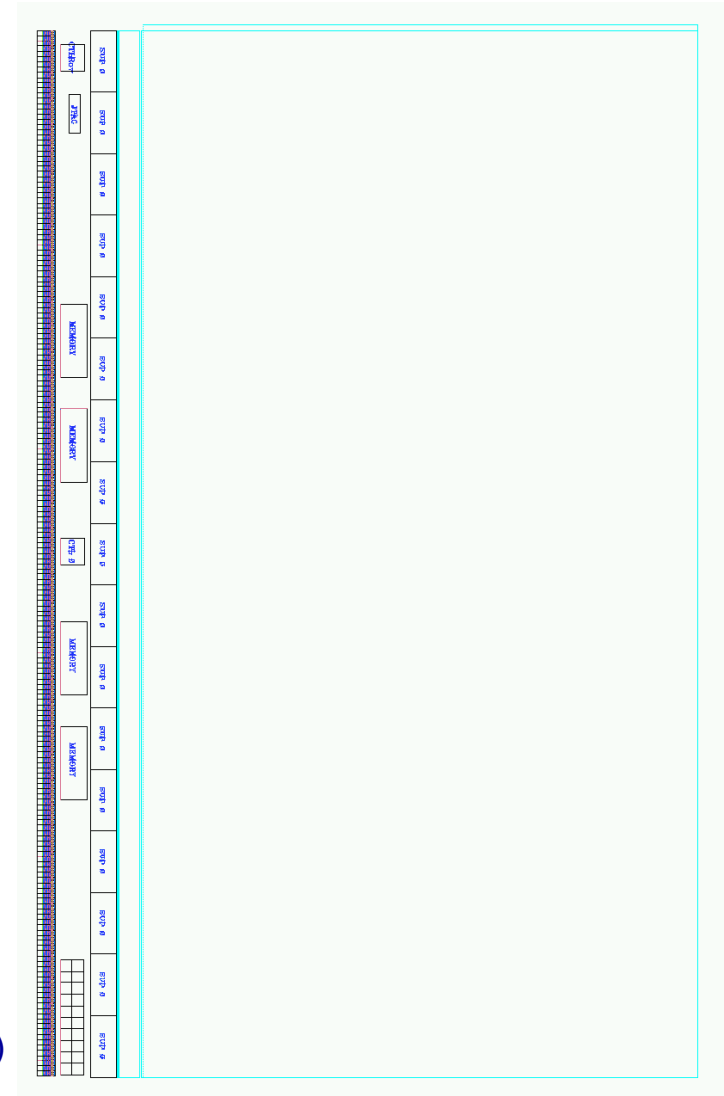
M22bis digital fake hit rate

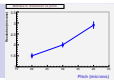




Autumn 2008 : fabrication of MIMOSA-26 = Final Sensor (TC)

- ✳ IDC/M-22 (binary outputs) complemented with \emptyset (SDC-2/SUZE-01)
- ✳ best performing (rad. tol.) pixel architecture of IDC/M-22(bis)
 - ↪ wait for Octobre beam test final results
- ✳ Active surface : 1152 columns of 576 pixels (21.2 x 10.6 mm²)
 - ↪ extension of IDC & SDC-2 from 128 col. to 9 x 128 col.
- ✳ Pixel pitch : 18.4 μm \rightarrow \sim 0.7 million pixels
 - ↪ $\sigma_{sp} \gtrsim 3.5 \mu m \Rightarrow$ pointing resolution $\sim 2 \mu m$ on DUT surface
- ✳ Integration time $\sim 110 \mu s \rightarrow \sim 10^4$ frames / second
- ✳ \emptyset based on 18 groups of 64 columns and assuming ≤ 9 "clusters" per row
- ✳ Chip dimensions : $\sim 21 \times 12$ mm²
- ✳ Data throughput: 1 output at ≥ 80 Mbits/s or 2 outputs at ≥ 40 Mbits/s
- ✳ Engineering run : 2 (+ ≤ 4) wafers of $\gtrsim 30$ chips expected (if yield ~ 50 %)
- ✳ Design under way \Rightarrow planned submission date \geq mid-November '08



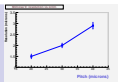


- Col. // architecture with discri. outputs validated for m.i.p. detection on real scale (128 col. of final length) :
 - ⇒ read-out frequency $\sim 10^4$ frames/s ✓
 - ⇒ pixel noise $\sim 10\text{--}13 e^- ENC \Rightarrow S/N \sim 17\text{--}22$ (MPV) ✓
 - ⇒ $\epsilon_{det} > 99.5\%$ with fake rate $\sim O(10^{-4} - 10^{-5})$, similar to MIMOSA-16 ✓
 - ⇒ $\sigma_{sp} \gtrsim 3.5 \mu m \Rightarrow$ resolution on impact position on DUT surface $\lesssim 2 \mu m$ ✓

- \emptyset μ -circuit with output buffers validated for 128 col. at read-out frequency $>$ nominal value ✓

- Radiation tolerance :
 - ⇒ achieved ionising radiation tolerance of pixel array sufficient for use of BT at CERN, FermiLab, ... ✓
(but source of noise increase still being investigated)
 - ⇒ non-ionising radiation tolerance may still be a concern once integrated particle flux $\gtrsim O(10^{12}) \pi^\pm / cm^2$
 - ⇒ latch-up tests of output memories in preparation (to be done in Octobre)

- ⇒ TC \equiv final sensor (combining col. // architecture with \emptyset μ -circuit) :
 - ⇒ design under way (crucial issues : extension from 128 to 1152 col. of IDC combined with SDC-2)
 - ⇒ in absence of unexpected pb, submission will occur \gtrsim mid-Novembre '08
 - ↪ TC sensor tests expected to start in January 2009

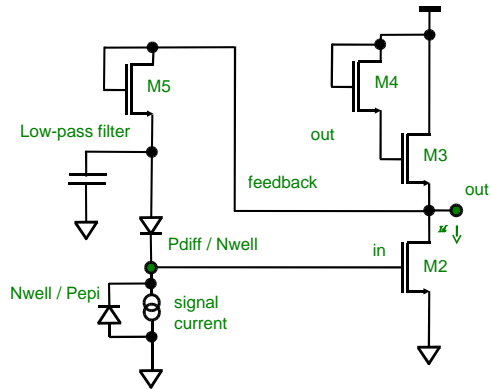


Best performing pixels (rad. tol. design) :

✧ *self-biased feedback diode (improved gain)*

✧ *reset diode (improved gain)*

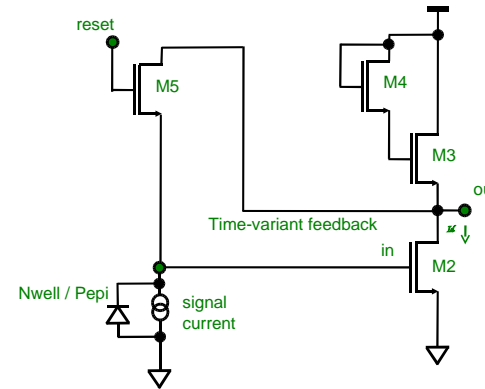
Amplifier schematics (3): improved common source + continuously biased from feedback (self-biased)



France

A. Dorokhov, IPHC, Strasbourg,

Amplifier schematics (4): improved common source + reset from feedback (time-variant feedback)



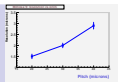
France

A. Dorokhov, IPHC, Strasbourg,

Main results obtained with exposure to ⁵⁵Fe source :

✧ *Chip-4 ; $F_{r.o.} = 100 \text{ MHz}$ ($t_{r.o.} = 92.5 \mu\text{s}$) ; $T \simeq 15^\circ \text{C}$ (coolant) / 20°C (chip) ;*

Pixel	diode	Noise (ENC)	CCE (4 pix)	CCE (9 pix)	CEE (25 pix)	comment
S6	$14.6 \mu\text{m}^2$	$12.4 e^-$	57 %	73 %	84 %	rad.tol. – self-bias – high gain
S7	$14.6 \mu\text{m}^2$	$11.4 e^-$	58 %	75 %	85 %	stand. – self-bias – high gain
S8	$19.4 \mu\text{m}^2$	$12.8 e^-$	65 %	82 %	90 %	stand. – self-bias – high gain
S9	$11.6 \mu\text{m}^2$	$10.5 e^-$	54 %	72 %	83 %	stand. – self-bias – high gain
S10	$15.2 \mu\text{m}^2$	$13.3 e^-$	60 %	77 %	86 %	rad.tol. – feedback reset – high gain
S12	$15.2 \mu\text{m}^2$	$11.8 e^-$	58 %	75 %	84 %	stand. – feedback reset – high gain



■ Dispersion between chips (rad. tol. pixels, with high gain) :

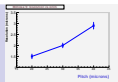
<i>Pixel</i>	<i>chip</i>	<i>Noise (ENC)</i>	<i>CCE (4 pix)</i>	<i>CCE (9 pix)</i>	<i>CEE (25 pix)</i>
S6	4	12.4 e ⁻	57 %	73 %	84 %
	3	12.7 e ⁻	59 %	76 %	86 %
	1	12.6 e ⁻	58 %	74 %	85 %
S10	4	13.3 e ⁻	60 %	77 %	86 %
	3	12.8 e ⁻	58 %	75 %	85 %
	1	13.5 e ⁻	59 %	76 %	86 %

■ Sensitivity to operating temperature (rad. tol. pixels, with high gain) :

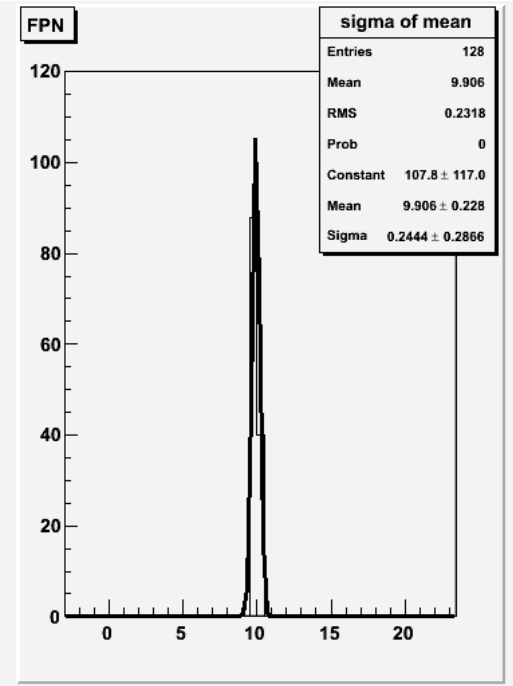
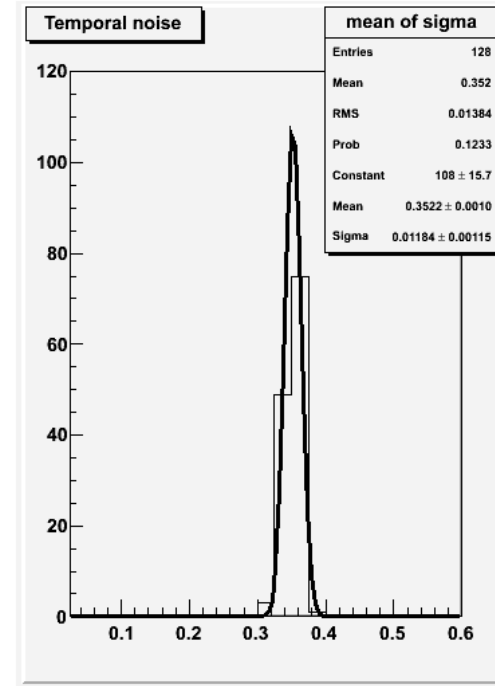
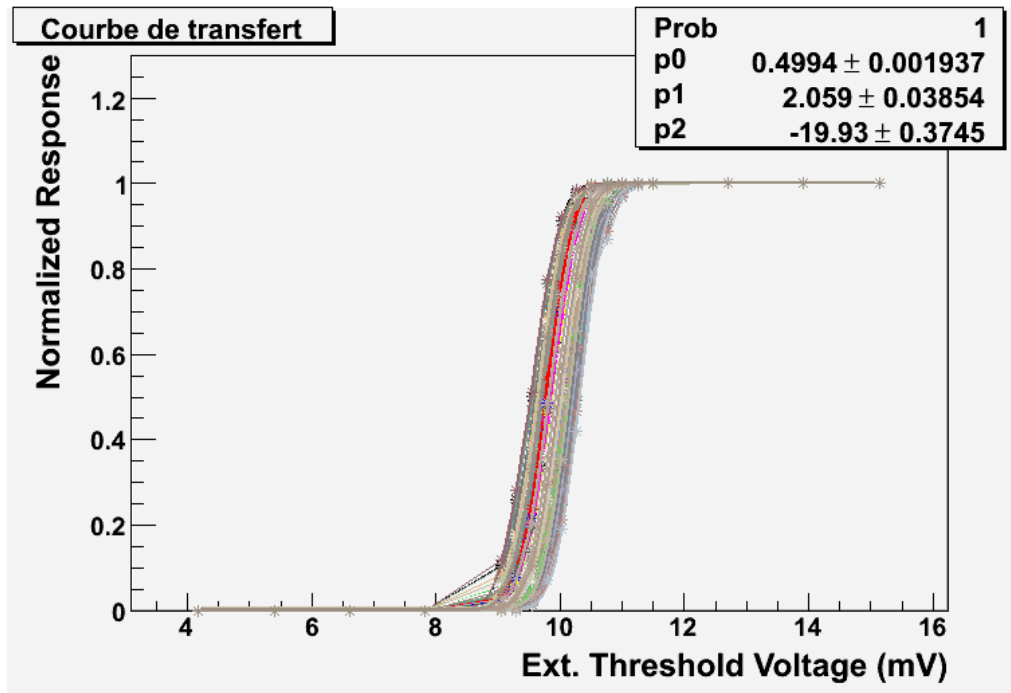
<i>Pixel</i>	<i>T (°C)</i>	<i>Noise (ENC)</i>	<i>CCE (4 pix)</i>	<i>CCE (9 pix)</i>	<i>CEE (25 pix)</i>
S6	0 / 10	12.5 e ⁻	58 %	75 %	85 %
	10 / 15	12.6 e ⁻	58 %	74%	85%
	30 / 35	13.0 e ⁻	59 %	76 %	80 %
S10	0 / 10	12.8 e ⁻	59 %	77 %	84 %
	10 / 15	13.5 e ⁻	59 %	76 %	86 %
	30 / 35	14.2 e ⁻	60 %	76 %	86 %

■ Conclusions :

- ✧ *Pixel array operationnal at nominal frequency and room temperature*
- ✧ *Rad. tol. pixel exhibits rather moderate noise (12.5–13.5 e⁻ ENC), ~ +1 e⁻ ENC w.r.t. standard diode*
- ✧ *Self-bias pixel seems slightly less noisy than reset pixel → assess ionising rad. tol. before chosing*



Uniform voltage (-10 mV \rightarrow 0 V) injected in discrim. \rightarrow transfer functions of all 128 discriminators :

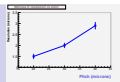


Noise performances for $F_{clock} = 100$ MHz, $T \sim 15 / 20^\circ\text{C}$

* *Temporal noise* $\simeq 0.35$ mV

* *Fixed Pattern Noise* $\simeq 0.25$ mV

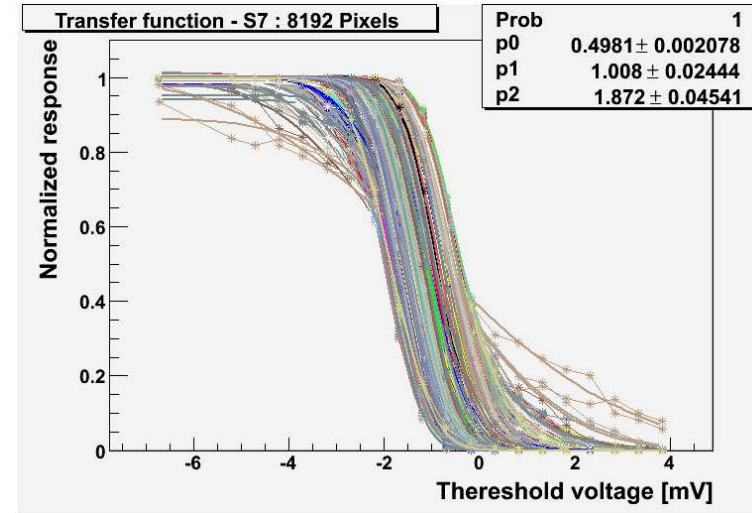
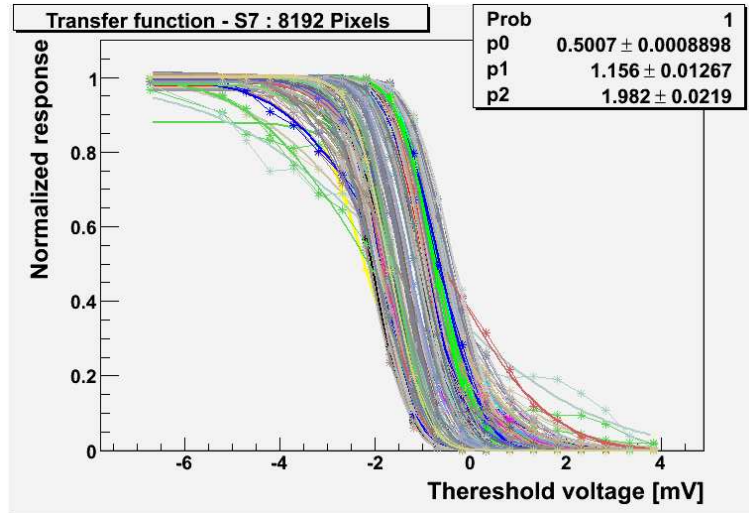
\Rightarrow Very satisfactory performances



Threshold scan of pixel noise from S6 & S7 (self-biased feedback with high gain) :

* rad. tol. diode (S6)

* standard diode (S7)



Noise derived from scan of S6 (CFC $\simeq 50 \mu V/e^-$)

- * Running conditions : 100 MHz, $T \sim 25^\circ C$
- * Pixel noise $\simeq 0.6 mV$
- * Fixed Pattern Noise $\simeq 0.3 mV (\equiv MIMOSA-16)$

⇒ Performances satisfy requirements

