DAQ Hardware Status

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DAQ architecture

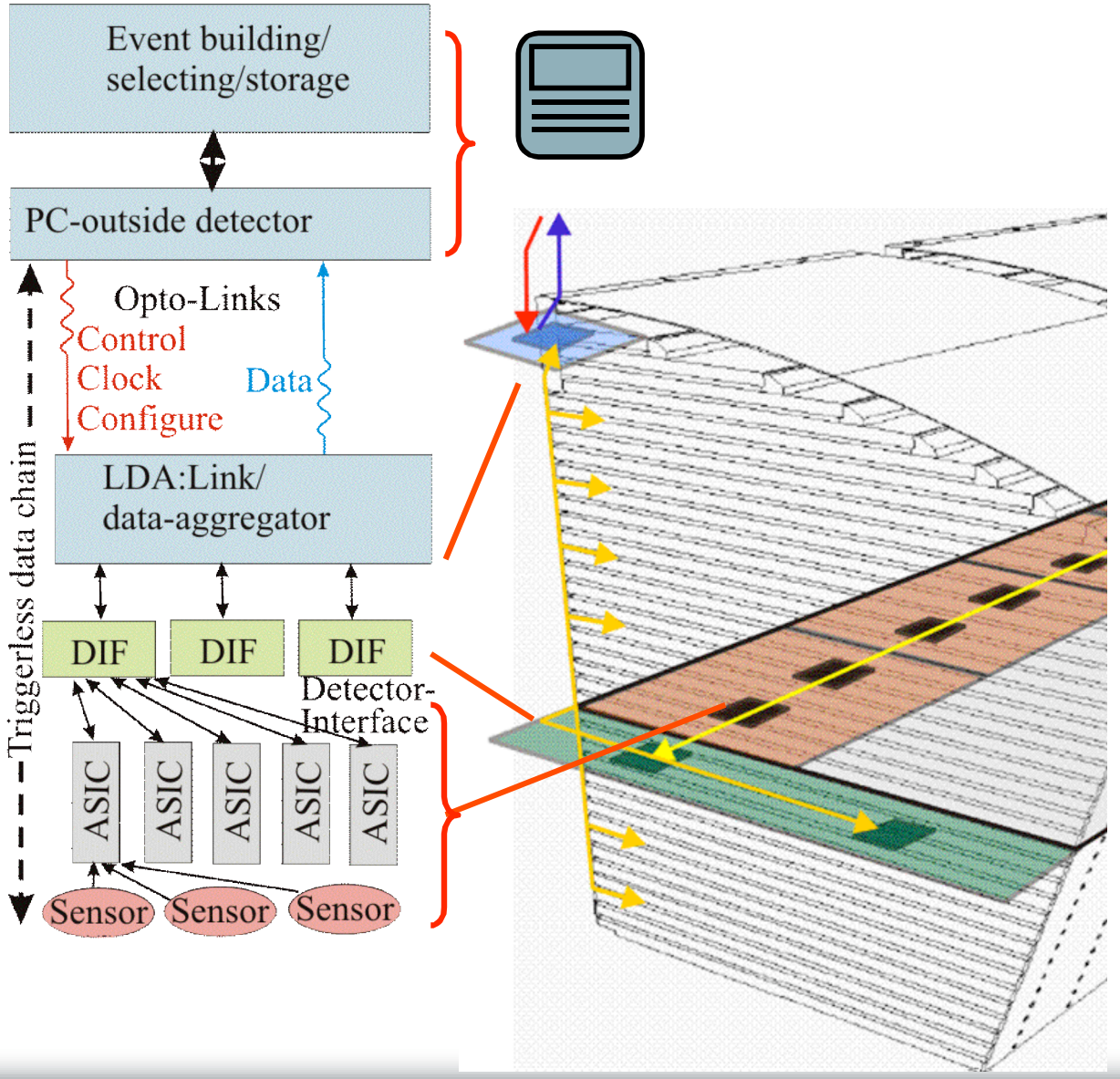
DAQ software

Off Detector Receiver (ODR)

Link Data Aggregator (LDA)

Detector Interface (DIF)

Detector Unit



DAQ architecture

Detector Unit: ASICs

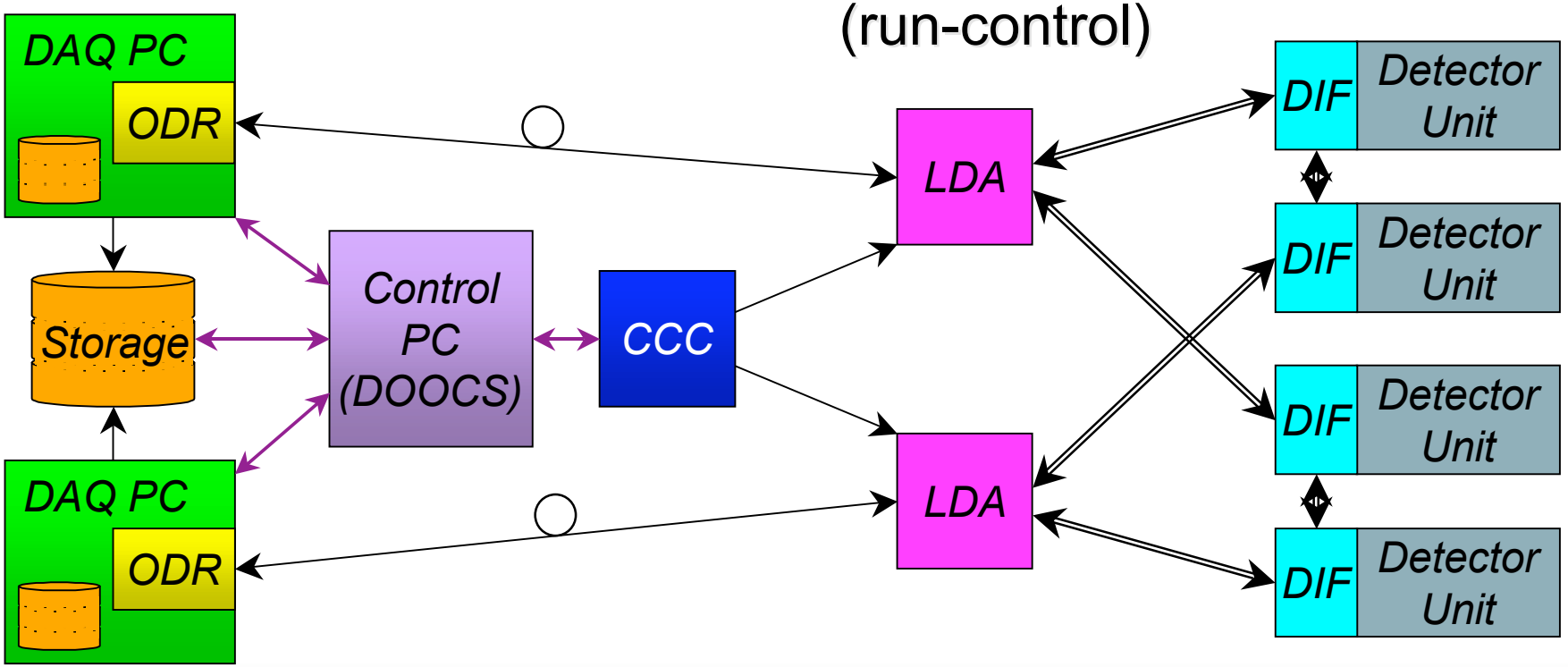
DIF: Detector InterFace connects Generic DAQ and services

LDA: Link/Data Aggregator – fanout/in DIFs and drives link to ODR

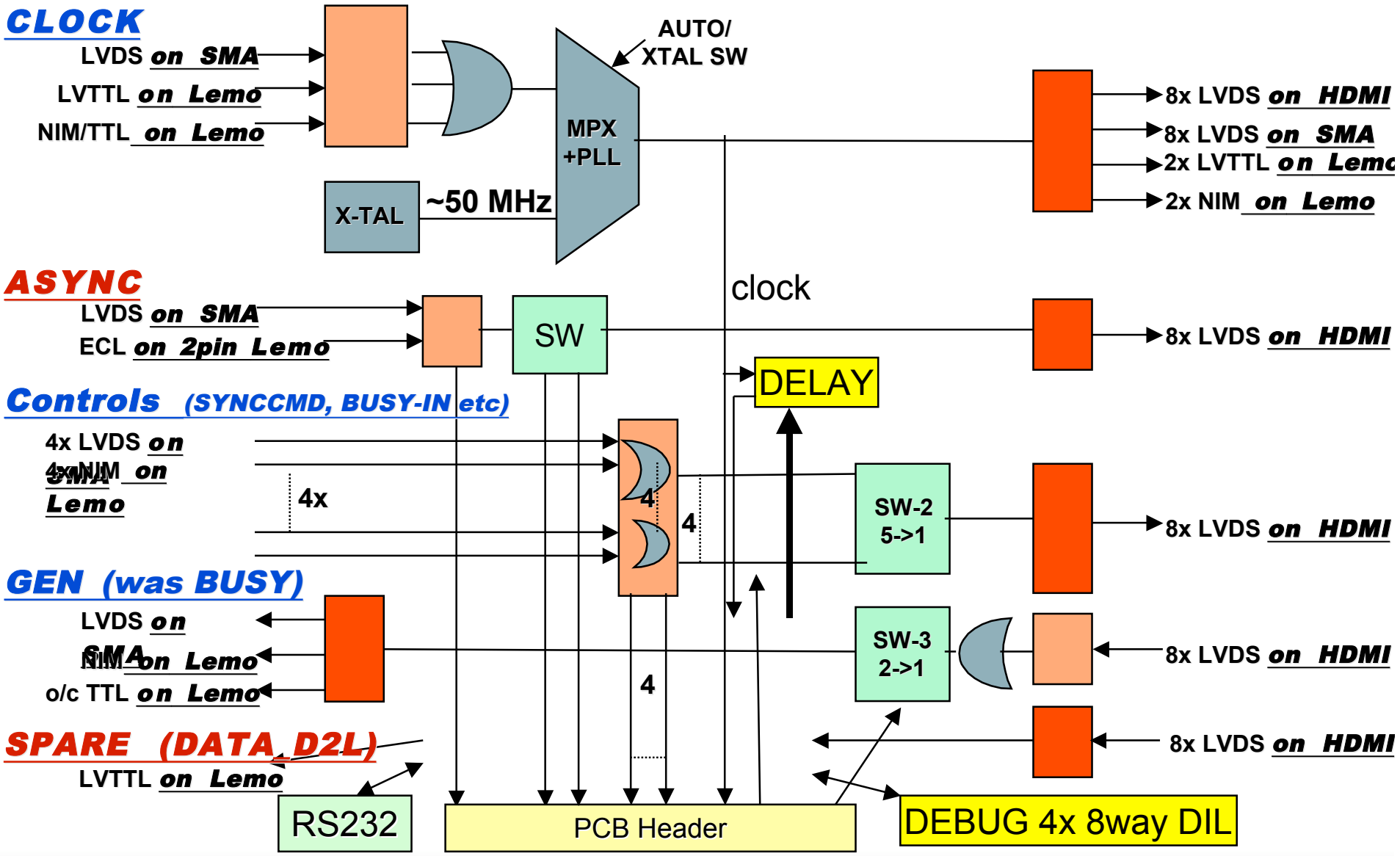
ODR: Off Detector Receiver – PC interface for system.

NEW! **CCC:** Clock & Control Card: Fanout to ODRs (or LDAs)

NEW! **CONTROL PC:** DOOCS GUI (run-control)



Clock: Detailed Overview Schematic



CCC Link Signals

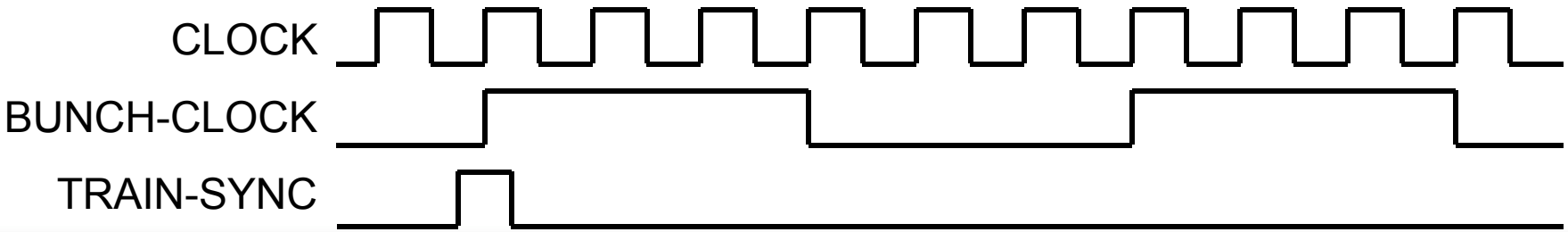
Uses same HDMI cable and signal types/direction

CCC HDMI Signals		
CLink Signal	*CCC Signal*	*Function*
CLOCK_L2D	CLOCK_OUT	Clock
DATA_L2D	TRAINSYNC_OUT	Trainsync signal output
DATA_D2L	Unused	Unused
ASYNC_L2D	FAST_OUT	Asynchronous signal
GEN_D2L	FAST_IN	Busy

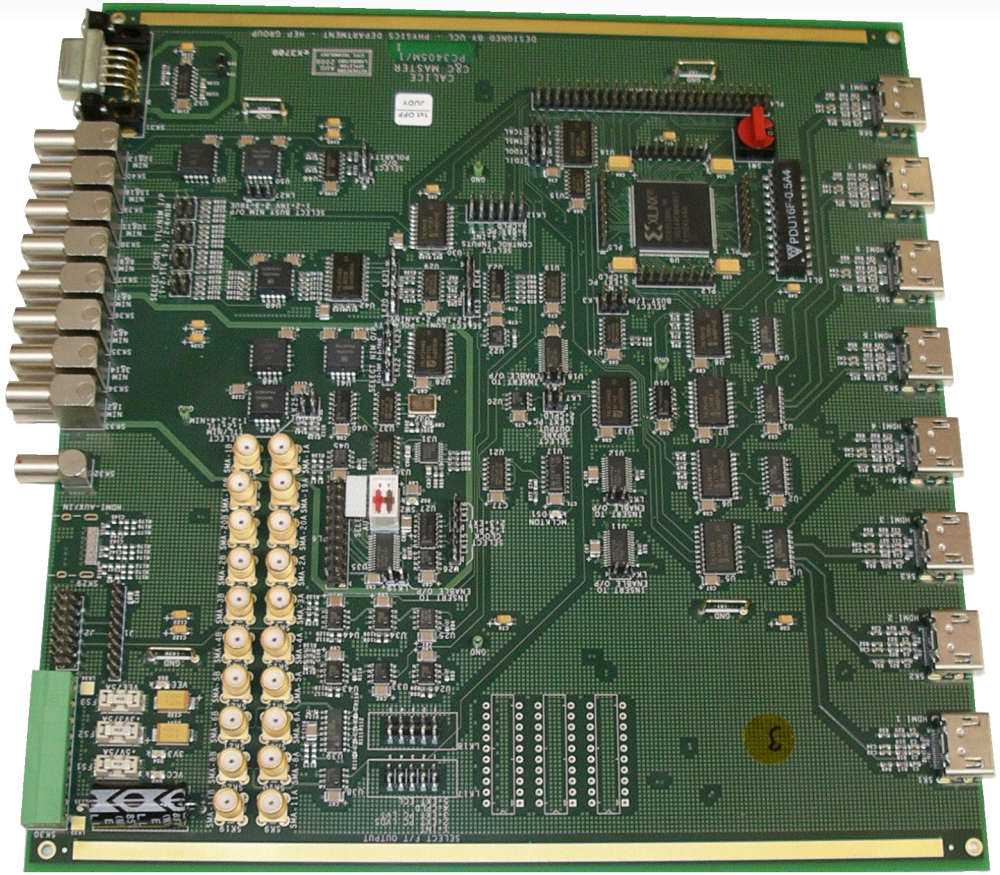
- **CLOCK**
  - Machine clock (50-100MHz)
- **TRAINSYNC_OUT**
  - Synchronisation of all the front-end slow clocks.
  - An external signal will be synchronized with/to CLOCK, phase adjusted and transmitted as a single clock-period wide pulse to the LDA.
  - To allow communicating with a stand-alone DIF, the CCC board can be configured to send the LDA 8b/10b serialised command for train-sync.
- **FAST_OUT**
  - Transfer asynchronous triggers as fast as possible.
  - In AUTO mode, used to Transfer BUSY to detector (toggle = level)
- **FAST_IN**
  - Used by DIFs (via LDA) signal to “stop acquisition” when needed.
  - Due to AC coupling the busy must asserted by constantly toggling this line.

Clock: Timing Overview

- Presume machine CLOCK period < bunch-period
  - Expected to be 50-100MHz, local or machine.
  - Common fanned-out to the detector
- BUNCH-CLOCK (slow clock) derived as CLOCK/n
  - Re-produced locally on DIF (with TRAINSYNC & counter)
- Start of train signal (TRAINSYNC) synchronises bunch-clocks on all DIFs.
  - Requires fixed-latency signal – a SYNCCMD.
  - TRAINSYNC "qualifies" CLOCK edge



Clock: Status/Schedule



- Schematic **DONE**
- Layout **DONE**
- Manufacture **DONE**
  - Testing to be started
  - Run of 2 with 8 more when satisfied working
- Firmware development: **TO BE STARTED**

DIF -LDA link testing

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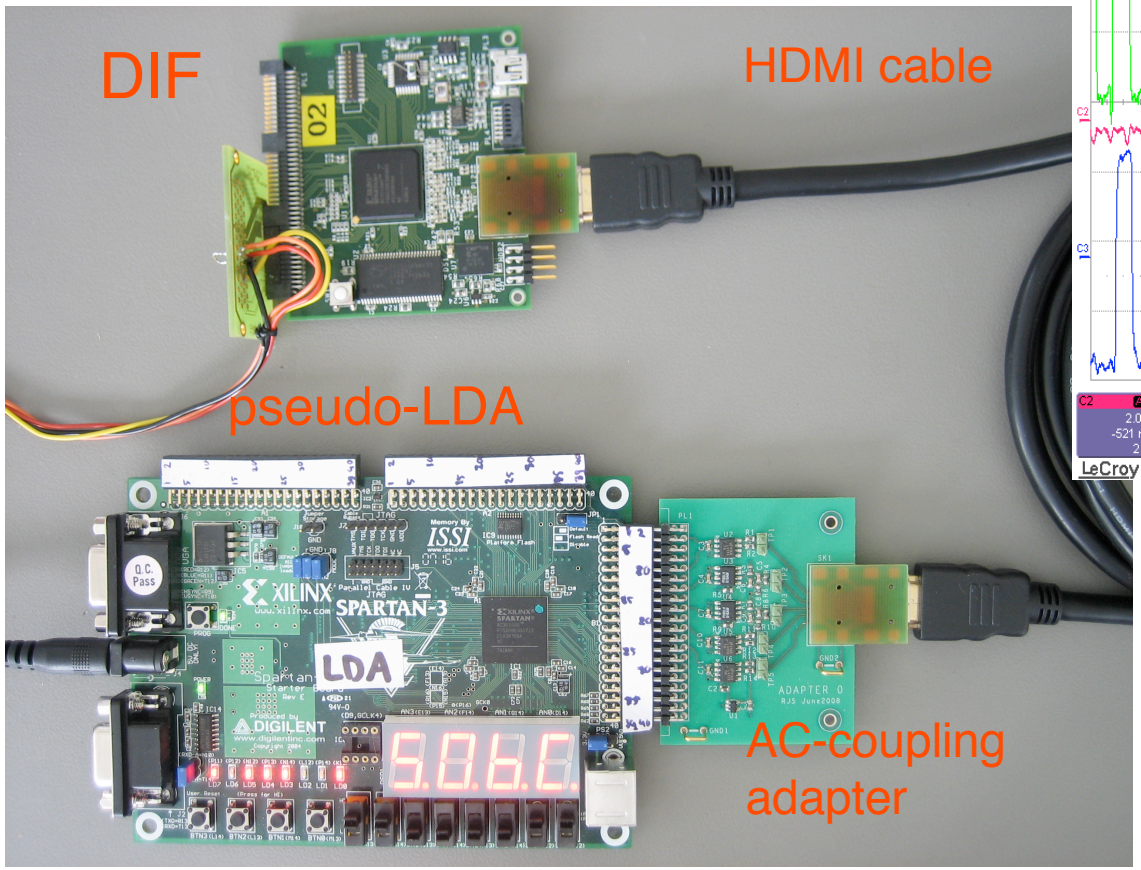
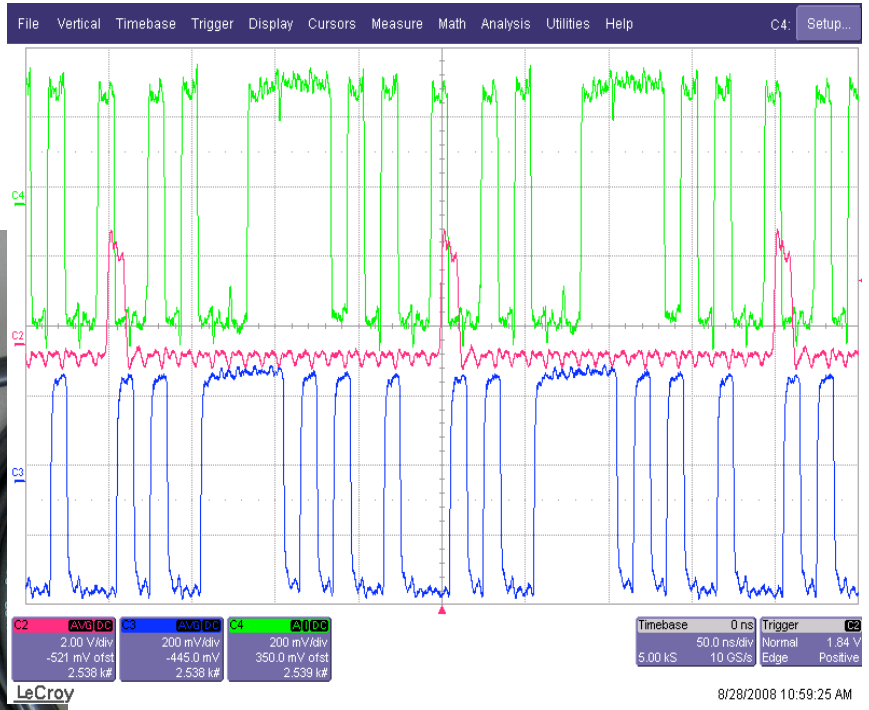
- Link shows signs of life.
  - pseudo-LDA sends CLK & 8B/10B data @ 100MHz over AC-coupled LVDS on HDMI cables





data loop-back in firmware stable

DIF: Status (generic) and Plans

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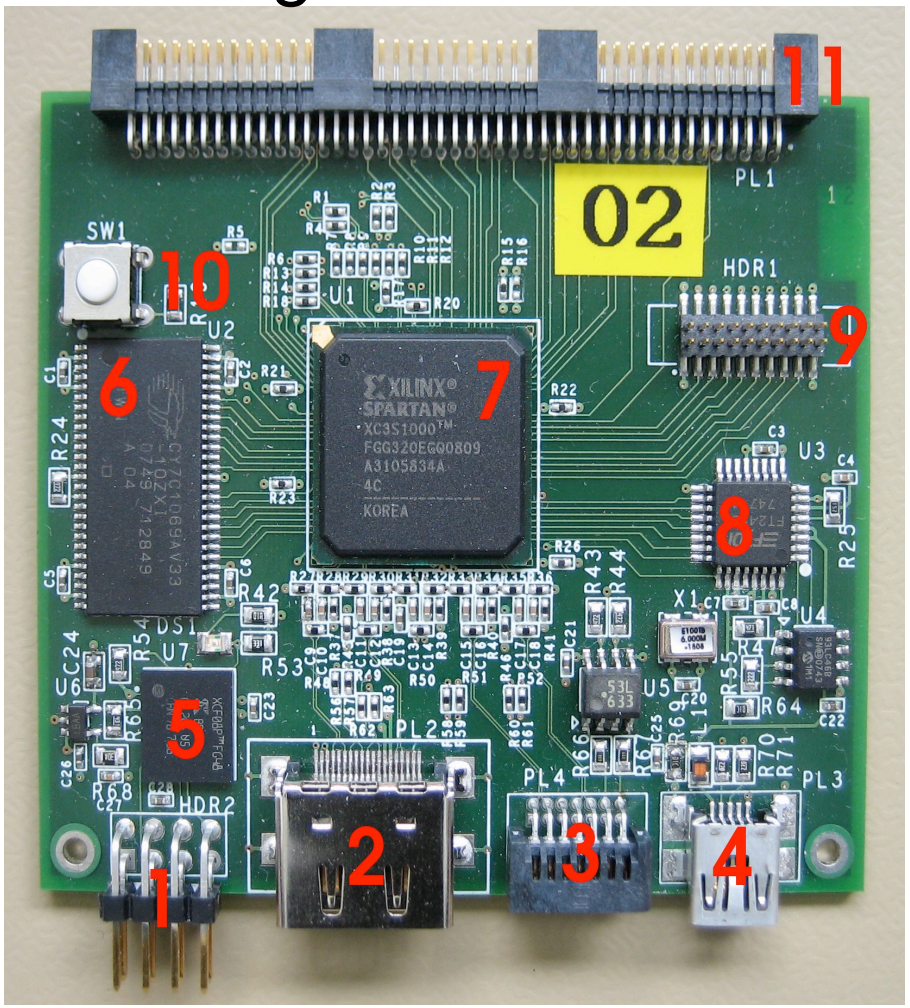
- Test hardware: **DONE**
- Firmware development: **STARTED**
  - LDA Link integration

ECAL DIF prototype:
65x72mm, 8 layers

1. JTAG programming header
2. LDA link HMDI connector
3. DIF link connector
4. mini-USB connector
5. Xilinx PROM
6. Cypress 2MB 10ns SRAM
7. Xilinx Spartan3-1000 FPGA
8. FDTI FT245R USB controller
9. 20p user header connector
10. reset pushbutton
11. 90pin SAMTEC IB connector

e.g: ECAL DIF

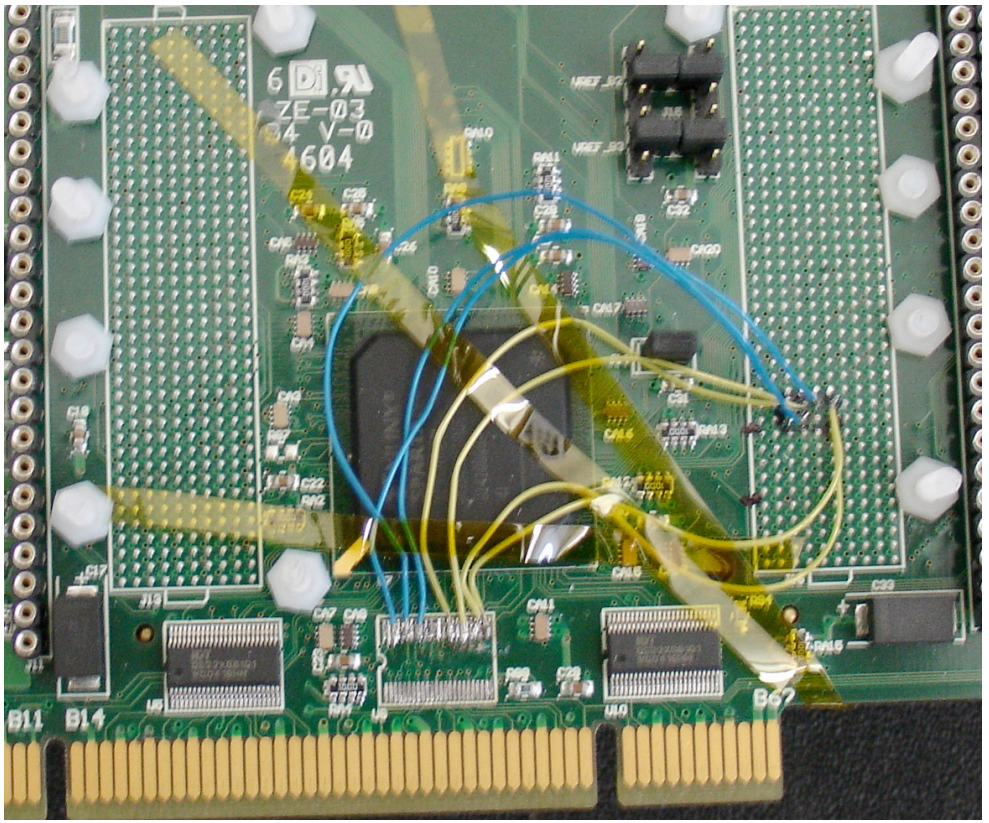


- 2 DIFs produced, parts available for 10 more.
- DIF hardware is (at least partly) functional

LDA-ODR Connectivity

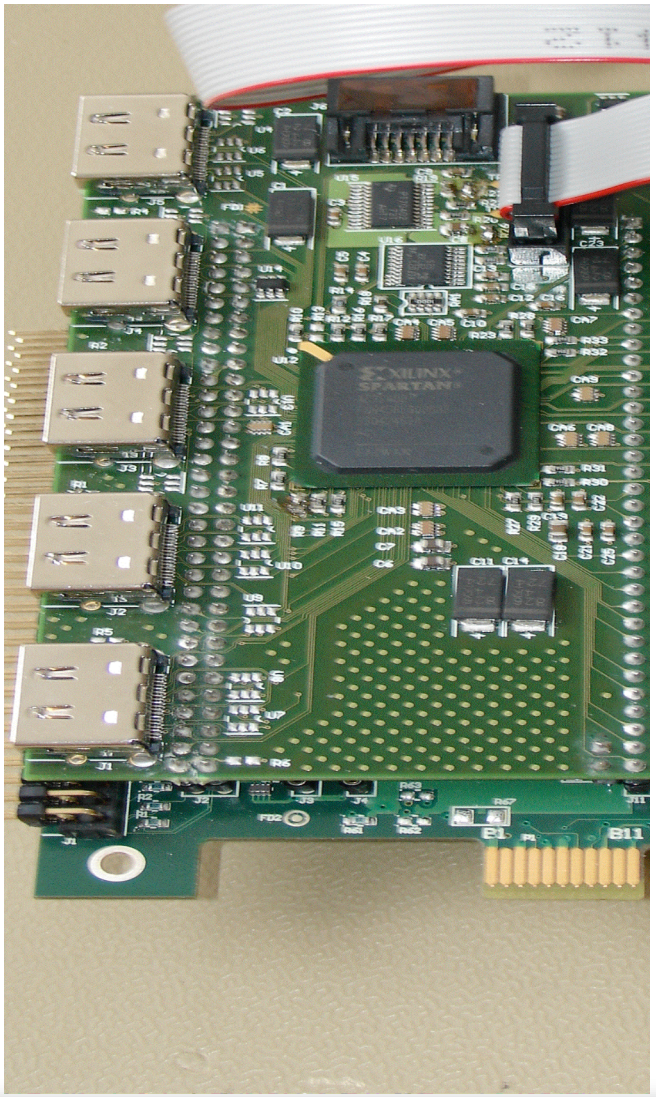
- Prototype LDA has hardware problems
  - Mainly incorrect signals routed on PCB to Eth add-on
  - LDA has been modified to attempt fix (see pic!)
  - Ethernet RX OK, auto-negotiation starts OK. BUT ..
  - Ethernet TX appears corrupt
  - random glitches and/or clock recovery problems
  - PHY in loop-back OK, so looks like the SERDES
  - Investigating …
- SOME GOOD NEWS:

  ODR-LDA protocol almost finalised



LDA-DIF Connectivity

- Current boards have 8 working HDMI links
  - Option for 10 on future boards with simple change of FPGA
- FPGA is basically used as an LVDS transceiver and clock fanout, although it will probably also handle the separate prompt/fast signals to/from the DIF
- Link documentation is proceeding, large amounts have been already done

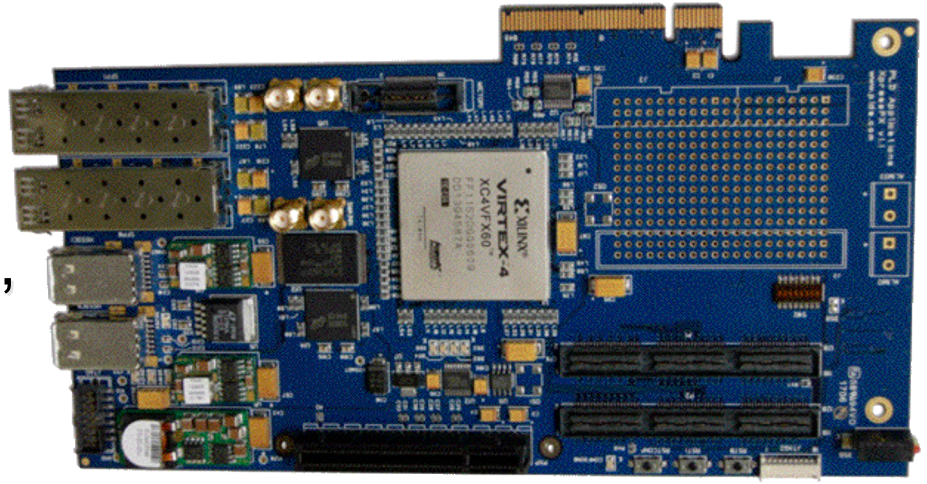


New LDA Base Board

MANCHESTER 1824

- Enterpoint is designing a replacement board for the BroadDown2 known as the Mulldonoch2
  - Extra I/O capabilities
  - EBX format board
  - PCI connector is replaced by a PC104 connector
  - SDRAM onboard
  - SPI flash ram
  - Better power system
- **Prototype production is expected sometime this month**.
- Is not designed for us especially, but rather is a generic board Enterpoint had planned already. Design time table got shifted when we found the error in the existing BD2 design
- A corrected BroadDown2 design is also going to be available in roughly the same time frame

ODR: Hardware/Firmware



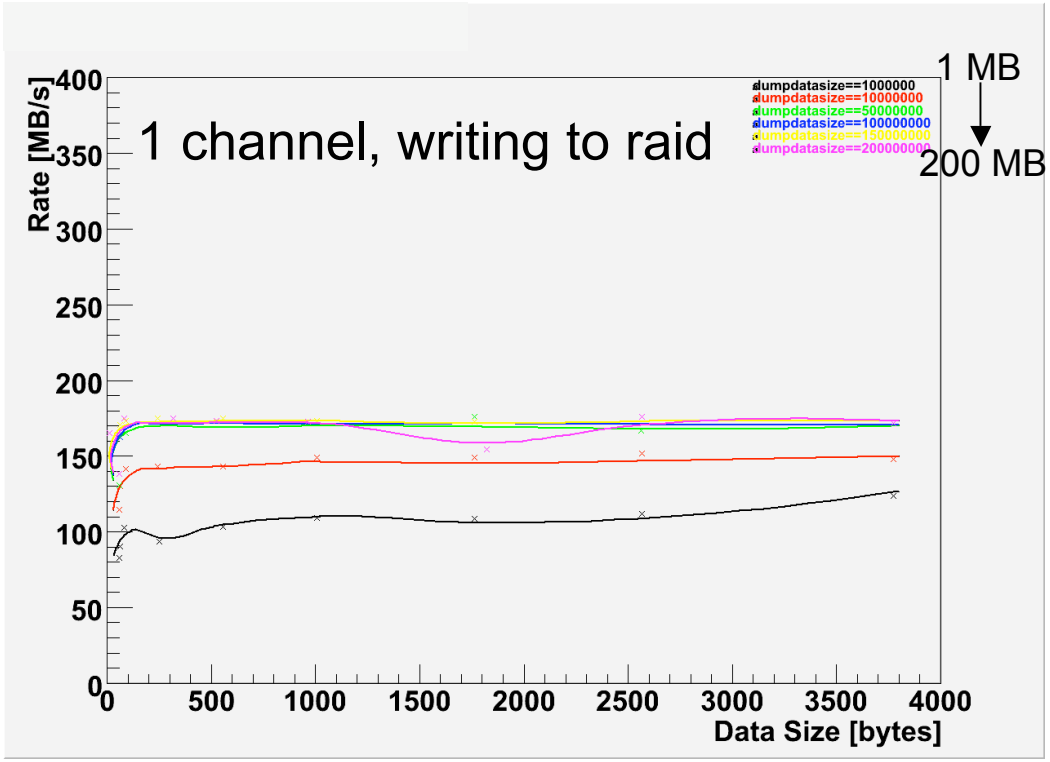
- ODR: **WORKING**
  - Receive data on 4x fibre (RX),
  - Write to disk FAST (250MB)
  - Send data up fibre (TX)
  - Controlled from Linux driver

- Future upgrade: Decode event header from LDA
  - Provides on-line info
  - Can deal with control messages from LDA
  - Allows host to write to disk without processing

ODR: Rate performance optimization (from ODR to disk)

Several factors to optimize:

- Architecture of the host (hyper-threading, raid array disks, kernel version, etc)
- Number of DMA buffers
  - currently using 950
- Number of buffers to fill before dumping the data to disk
  - best to have about N DMA buffers - 200 (so 750 for 950 DMA buffers)
- **Size of files to write** (grouping of data files)
  - Called dumpdatasize on plot
  - Dominant factor
  - chose 100 MB



DAQ status

- Overall status: all components exist, firmware needs to be developed
- LDA needs a respin, new board to arrive Mid-October (holds up integration of all other components to a testbench)
- CCC board has been delivered and will be tested soon