Electronics Integration - Status

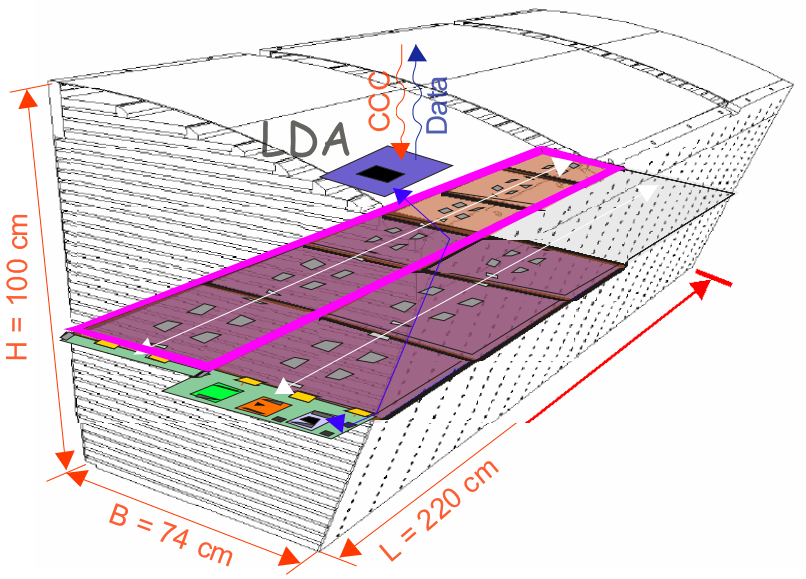
Mathias Reinecke

for the AHCAL developers

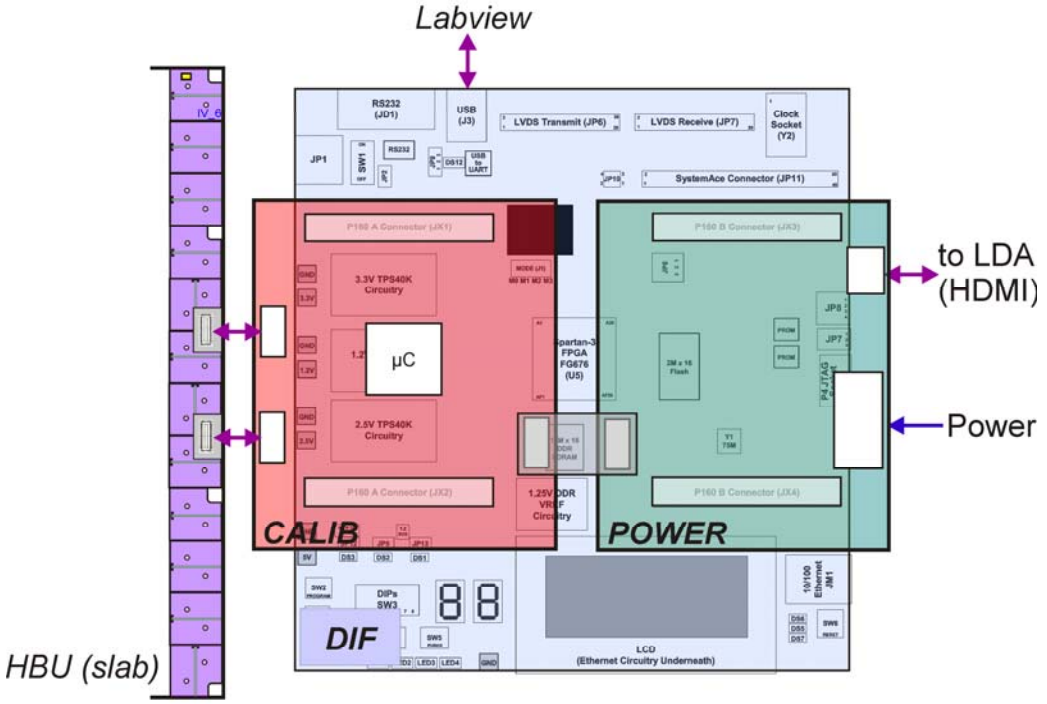
Next prototype: Architecture

FE

The goal …



1st EUDET Prototype (**1st step**)



Commercial DIF, new mezzan.
(CALIB, POWER), 1HBU (later: 6)

Prototype Tiles

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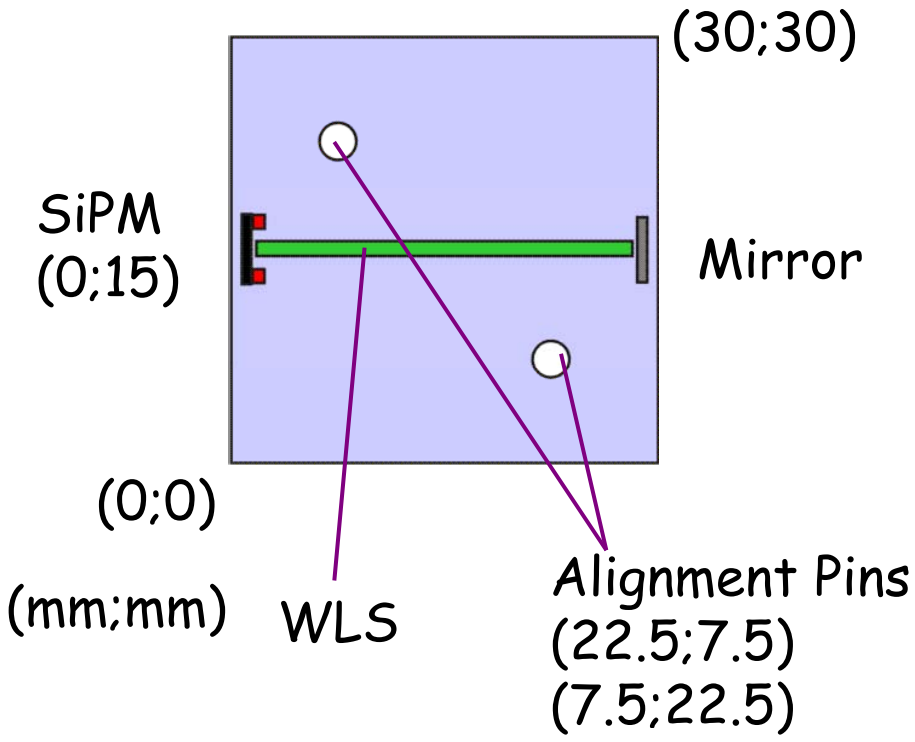
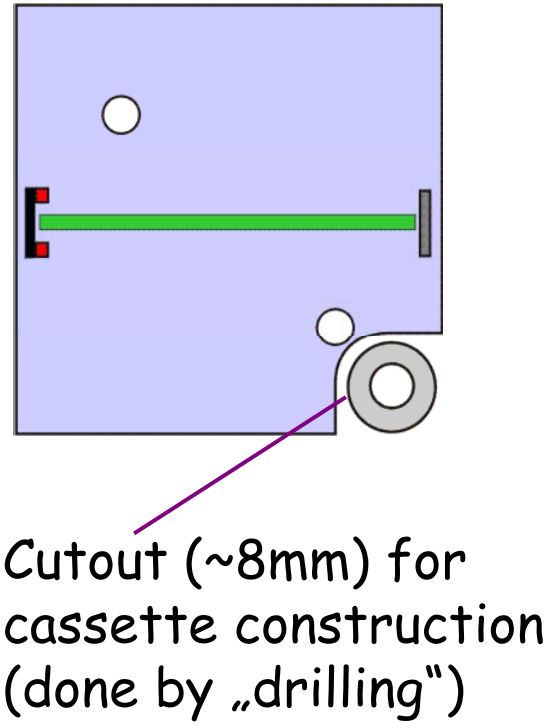
Prototype Tile for HBU0



Mechanics Tile for HBU0



100-150 prototype tiles (structures machined, not moulded) expected very soon.

Tiles for EUDET module

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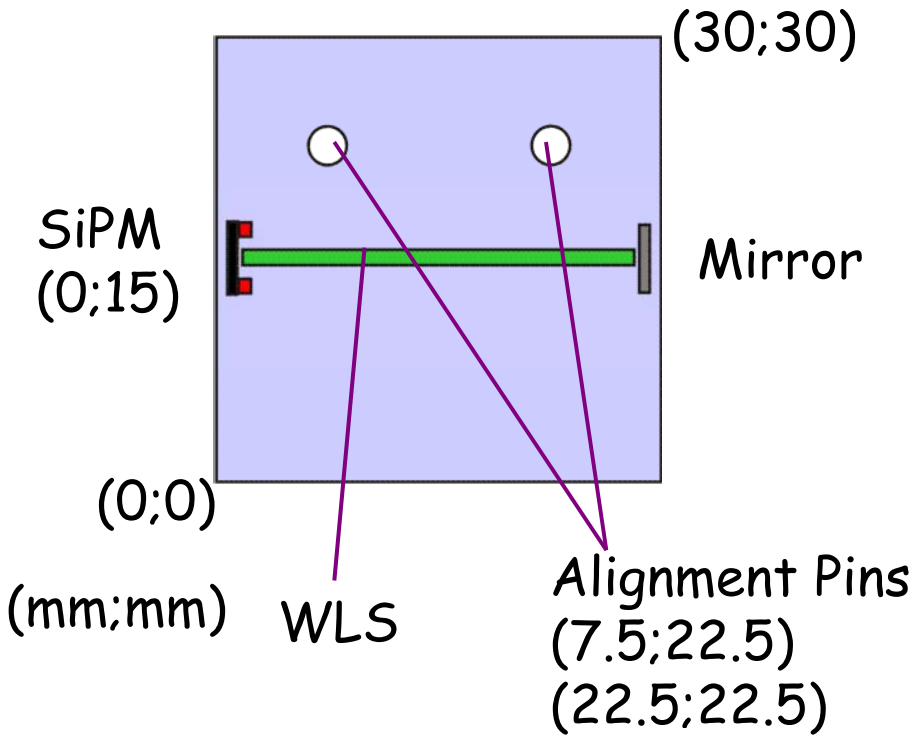
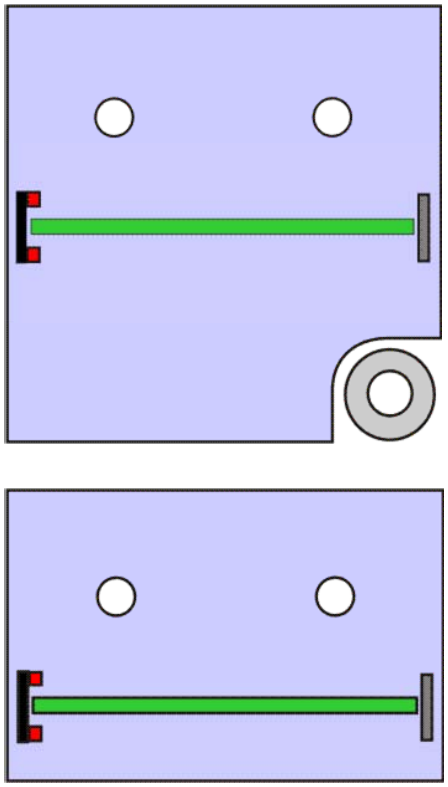
Standard Tile (moulded)





Shorted (by 1cm) tile for inter-layer sizes

Time schedule for moulded tiles not completely clear (end of 2008?).

HCAL Base Unit (HBU0)

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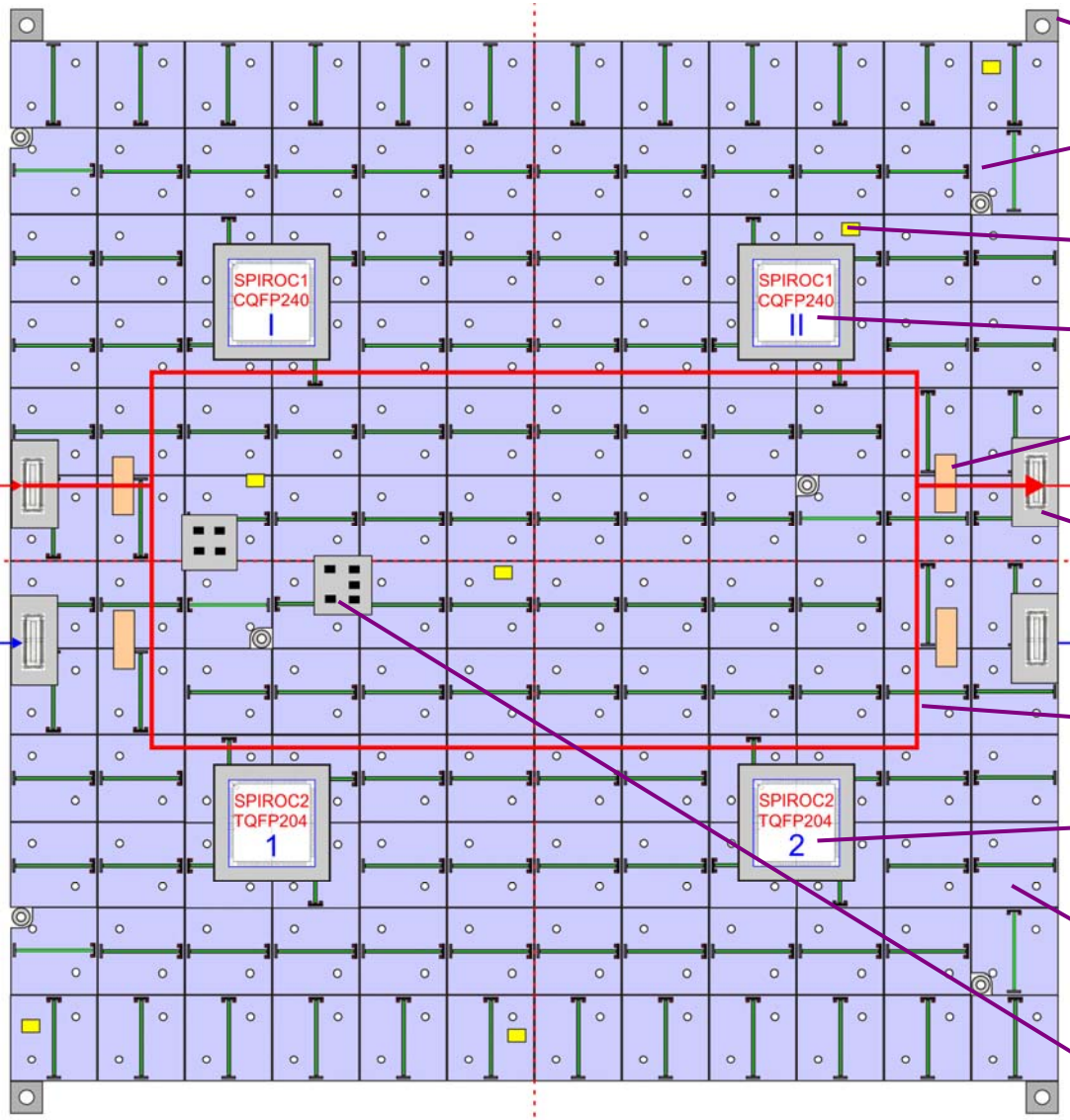


Signal IN

Power IN

Cassette fixation

Mechanics Tile

Temp. Sensor

SPIROC1

Debug Conn.

Flexlead Conn.

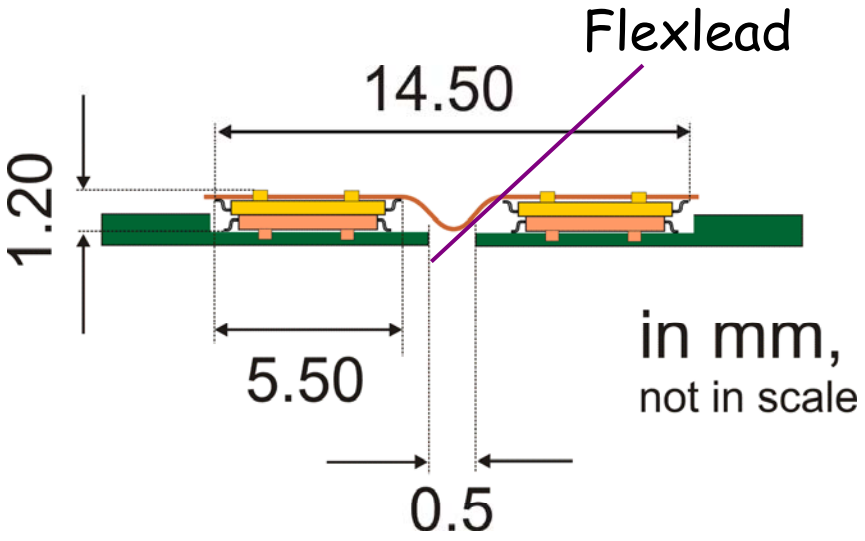
Two signal paths

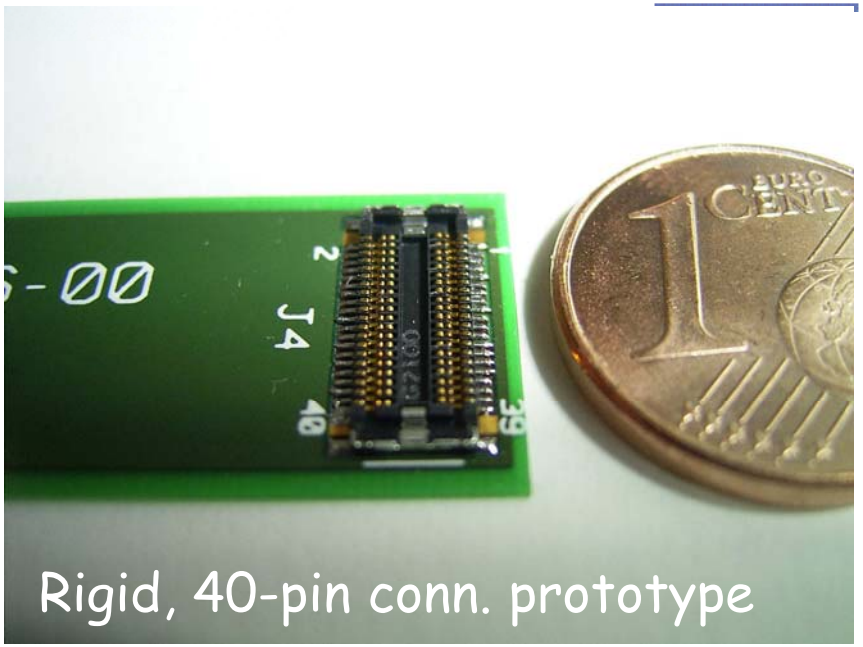
SPIROC2

Prototype Tile

Calibration Electr.
(LED + Charge Inj)

HBU0 Interconnection





Flexlead: Rigid below connectors, 4 layers,
flexible (polyimide) in between, 2 layers
80-pin connectors

Bended flexlead allows HBU-HBU displacement of ±100μm.

Concern: Bending forces (tension) might disconnect one connector.

Expected cost relation flexlead/connector: ~1.5

Under investigation: Flexleads without connectors (IR soldering)
(M. Goodrick et al., Cambridge)

HBU0 Interconnection II

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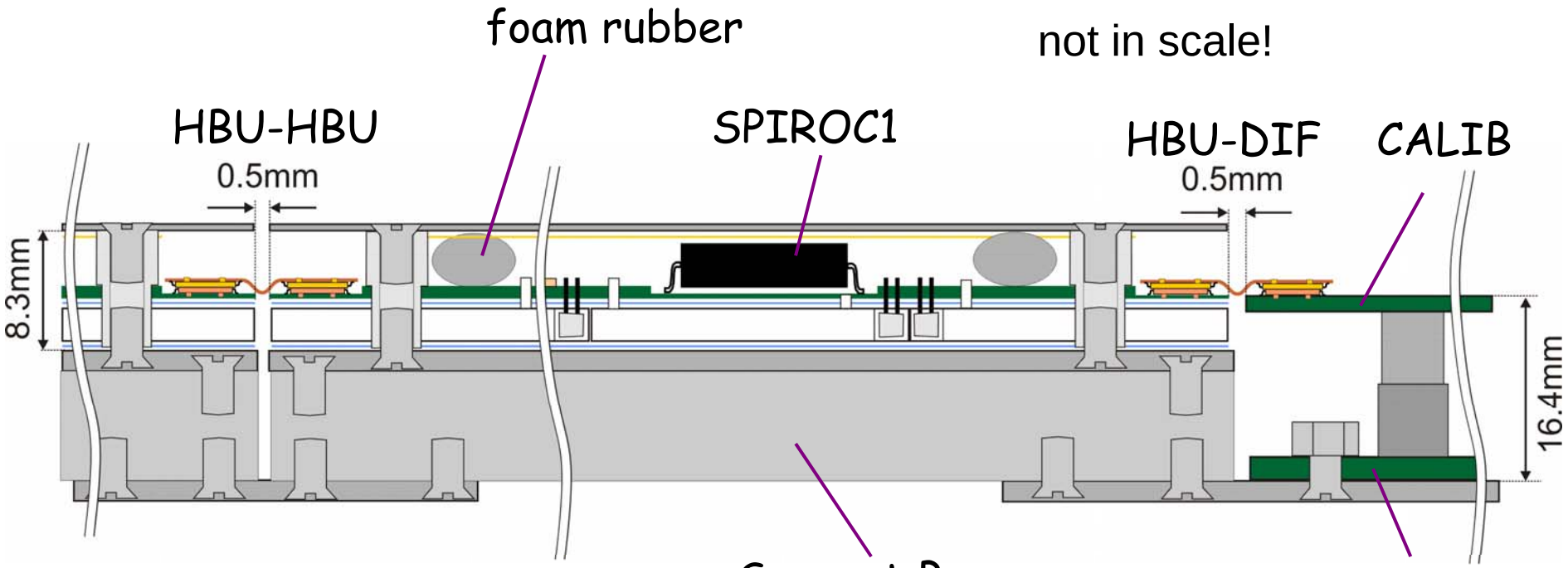
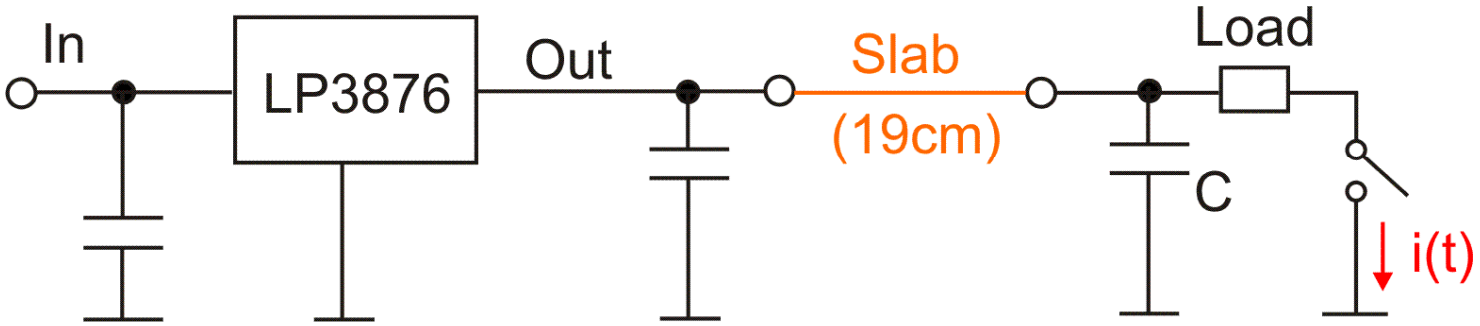


Bended flexlead allows HBU-HBU displacement of ±100μm.

Power Pulsing Tests

Detector electronics (Load) is switched between „off" (no current) and „on" (full current) with 1% duty cycle.
=> Oscillations on 2.20m-long power-ground system?

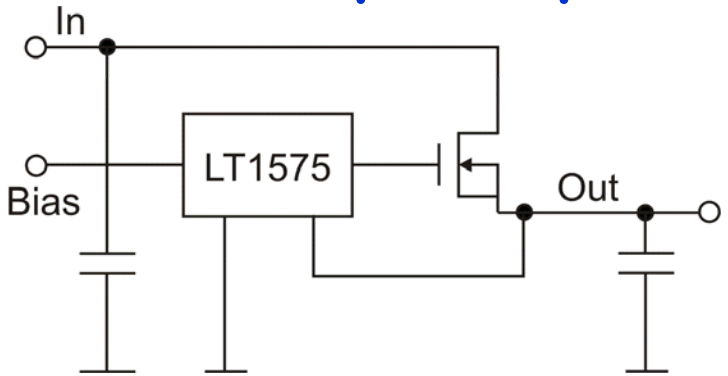
Test Setup 1



Tested:
Switched Current: 0.7…3A
Load Block Caps : 0…10µF

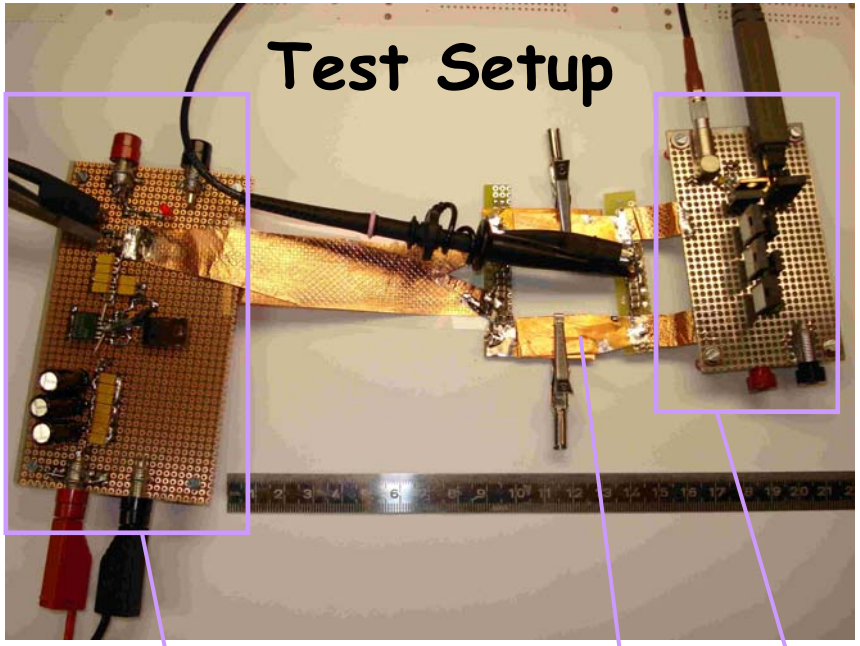
Settling Time / Overshoot = ??

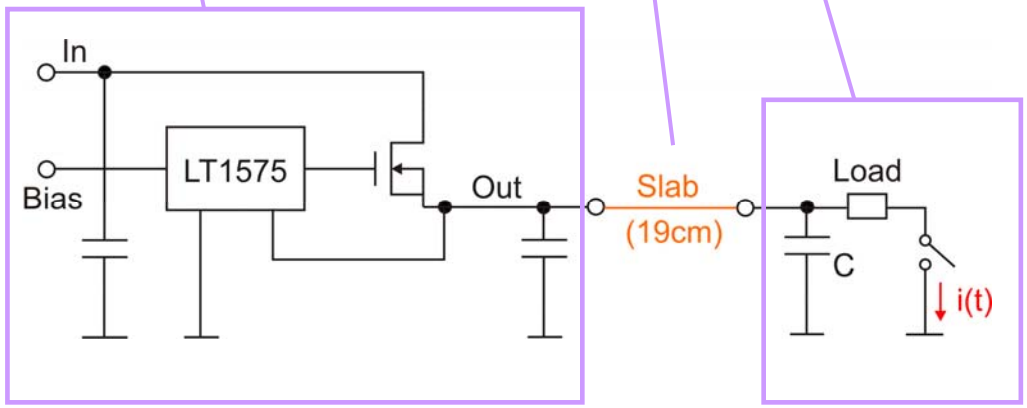
Test Setup 2 (input)



Power cycling test setup

FE





Settling time (Load side):
Voltage within 50mV of final value.
Aim: reasonable values for efficient power cycling (< 50µs)

Overshoot shown here for switch-off case (worst-case).
Aim: Protection of devices, stable register settings.

Later: Stability test for 2.20m slabs

Power Pulsing with Slab : Setup

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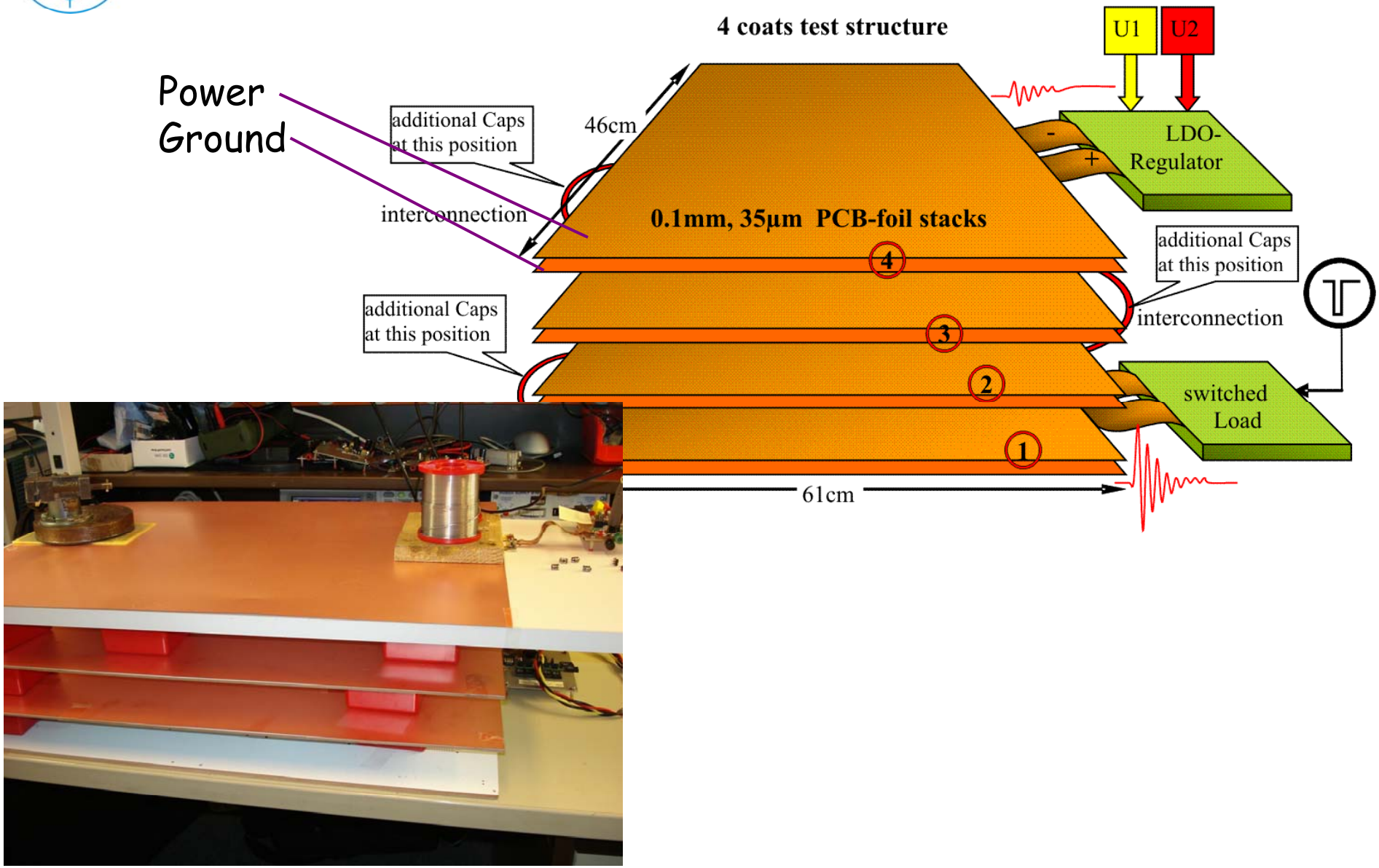

Power Pulsing: Results

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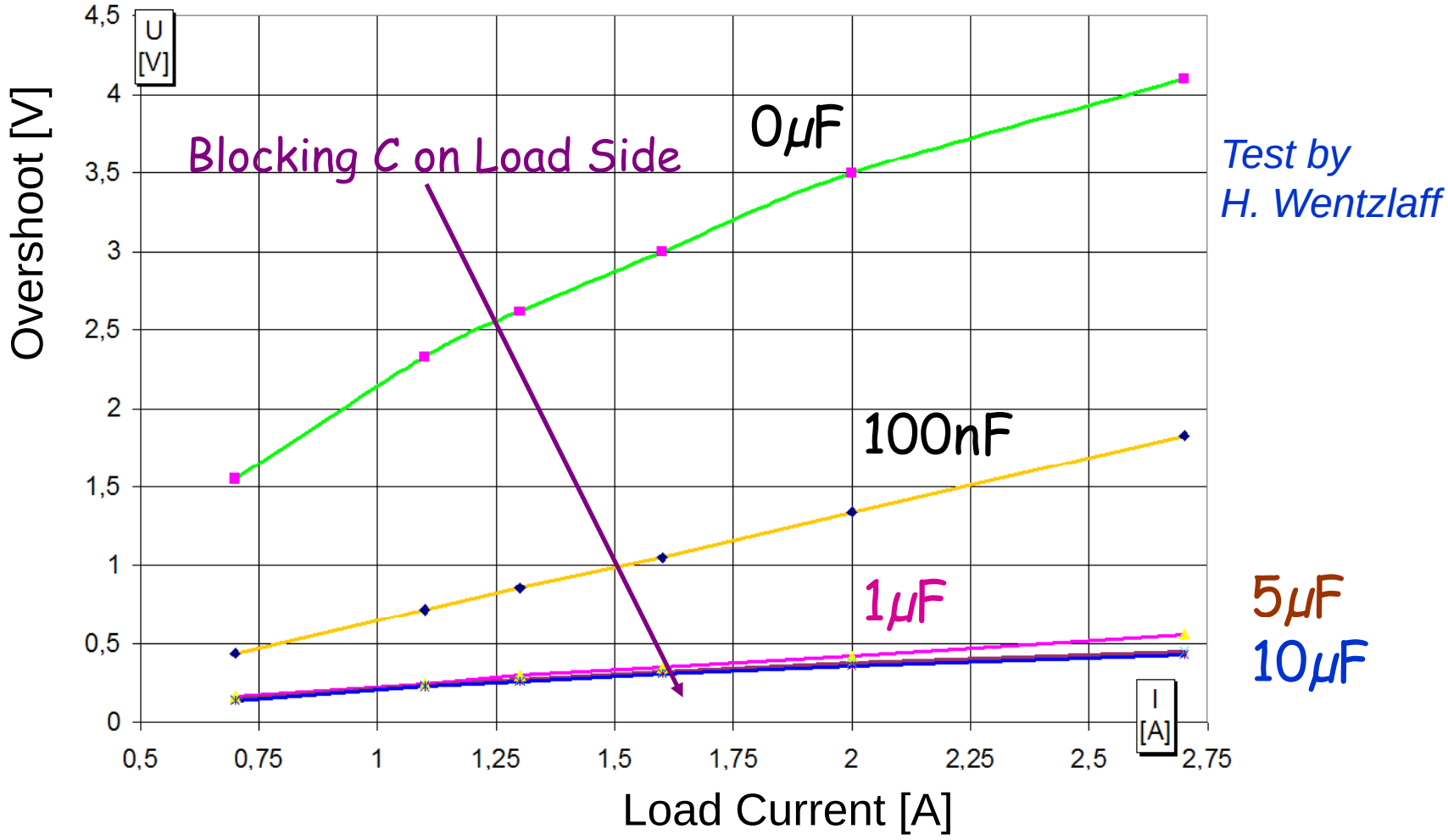
Typical results for overshoot (loadside), similar for both setups.
Overshoot on regulator side: <150mV.

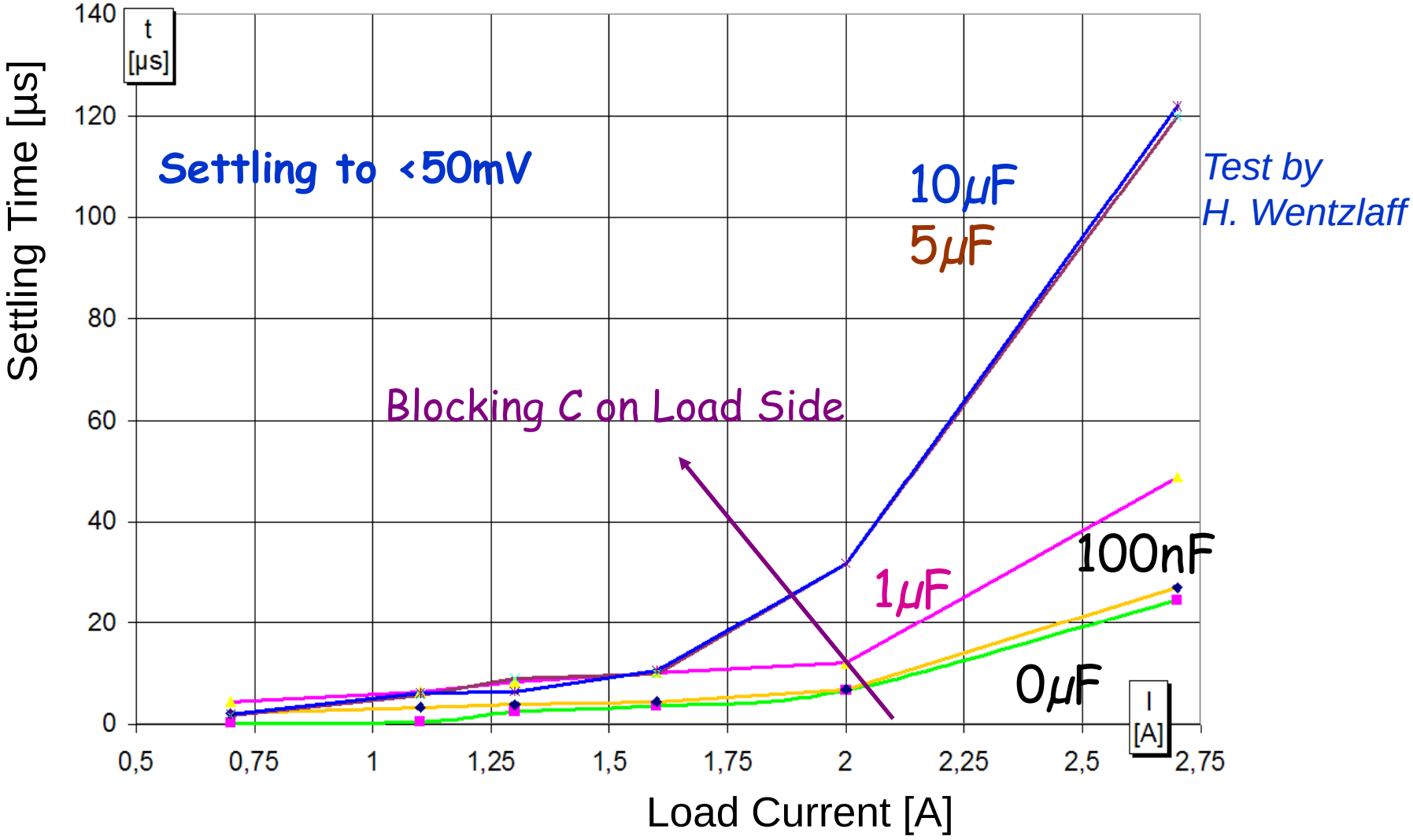


Test by H. Wentzlaff

Power Pulsing: Results

FE

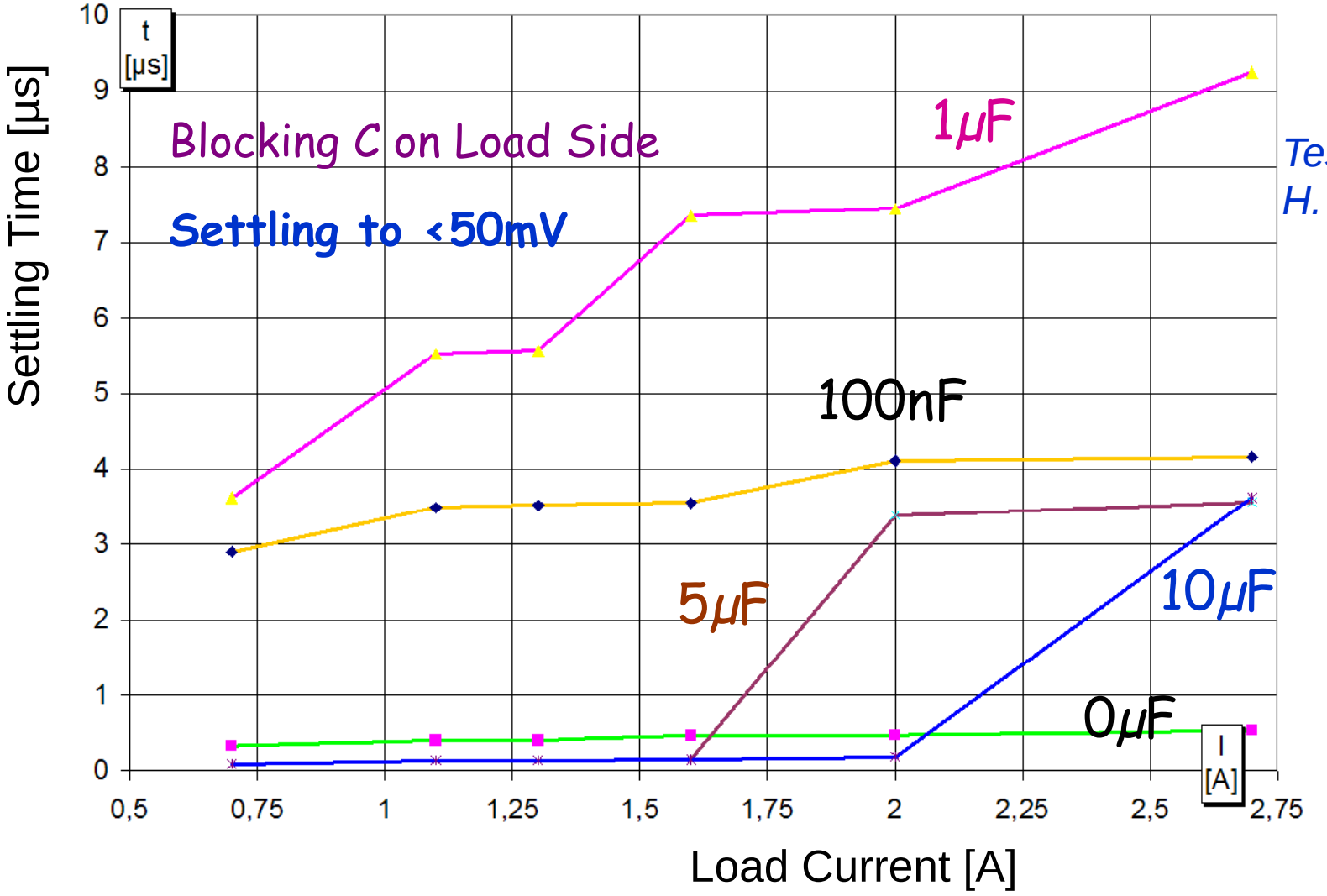
Typical results for settling time (loadside), setup 1 (LP3876)



Power Pulsing: Results

FE

Typical results for settling time (loadside), setup 2 (LT1575)



Test by H. Wentzlaff

Power Pulsing - Status

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Overshoot, settling-time good on regulator side.

Setup 2 (with transistor): better settling time (factor 10),
in the order of 5..10μs.

Overshoot is still about 0.2-0.5V (~150ns spikes) for large blocking caps on load side. Trade-off settling time - overshoot.

Dependency on load-switch transition (5-10ns now)?

Influence of the 2.20m-long slab seems to be small (analysis ongoing)

AHCAL - Status Modules

FE

DIF (AHCAL):

-Two commercial FPGA boards have arrived.
-VHDL development should starts now

POWER (supply of AHCAL electronics):

-Components and architecture fixed in principal, but:
-Regulator setup has to be checked for 2.20m slabs

HBU0 (defines timelines for all other parts):

-Schematic needs information about SPIROC2 and tiles.
-Initial setup only has 2 HBU0s (no full slab test).
-SPIROC1 and SPIROC2 in independent signal chains.

CALIB (2 LED systems (Prague, Wuppertal) and charge-injection):

-Module's duties fixed, schematic almost finished.
-Layout generation when we fix HBU interface (and design).
-Microcontroller programming starts now (SPI to DIF, LVDS)

Timeline (Rev. 1)

FE

Milestone shifted now by 1 month to Nov. 08.
Full slab not available before mid 2009.

Conclusions

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-AHCAL techn. prototype (TP) does not cover a full slab,
but ~150 channels (2 HBU0s, tile-prototypes).

-Eudet module (detector layer) requires HBU redesign (mid 2009).

-timeline for TP is defined by HBU0 (input SPIROC2, tile geometry).