

JRA2-SITRA status report

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for JRA2-SITRA partners (LPNHE Paris, Ch.U. Prague, Helsinki, Santander) and
associates (CNM Barcelona, HEPHY Vienna, IFIC Valencia, Obninsk):

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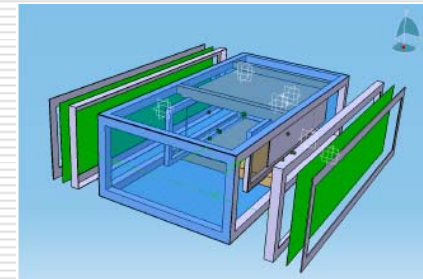
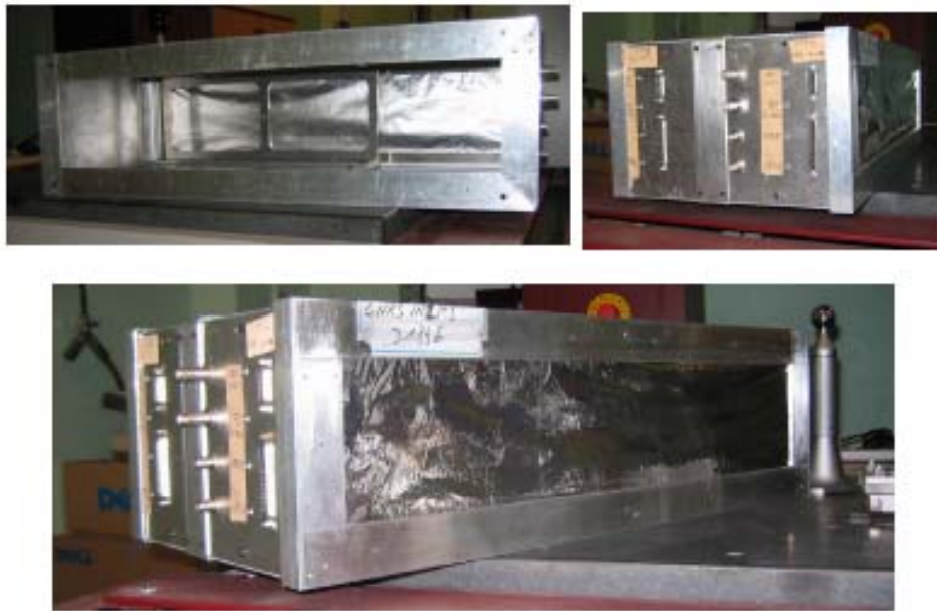
Milestones and Deliverables (Past)

Milestone Deliverable	Deadline	Status
Convection cooling system prototype	22	Ready
Motorised 3D table	24	Ready
Central tracker prototype	24	Ready
FE chip version 1	24	Ready

Convection Cooling System Prototype (LPNHE + OSU + Torino U.)

Eudet-Memo-2007-52

Insulating cage for DESY test beam

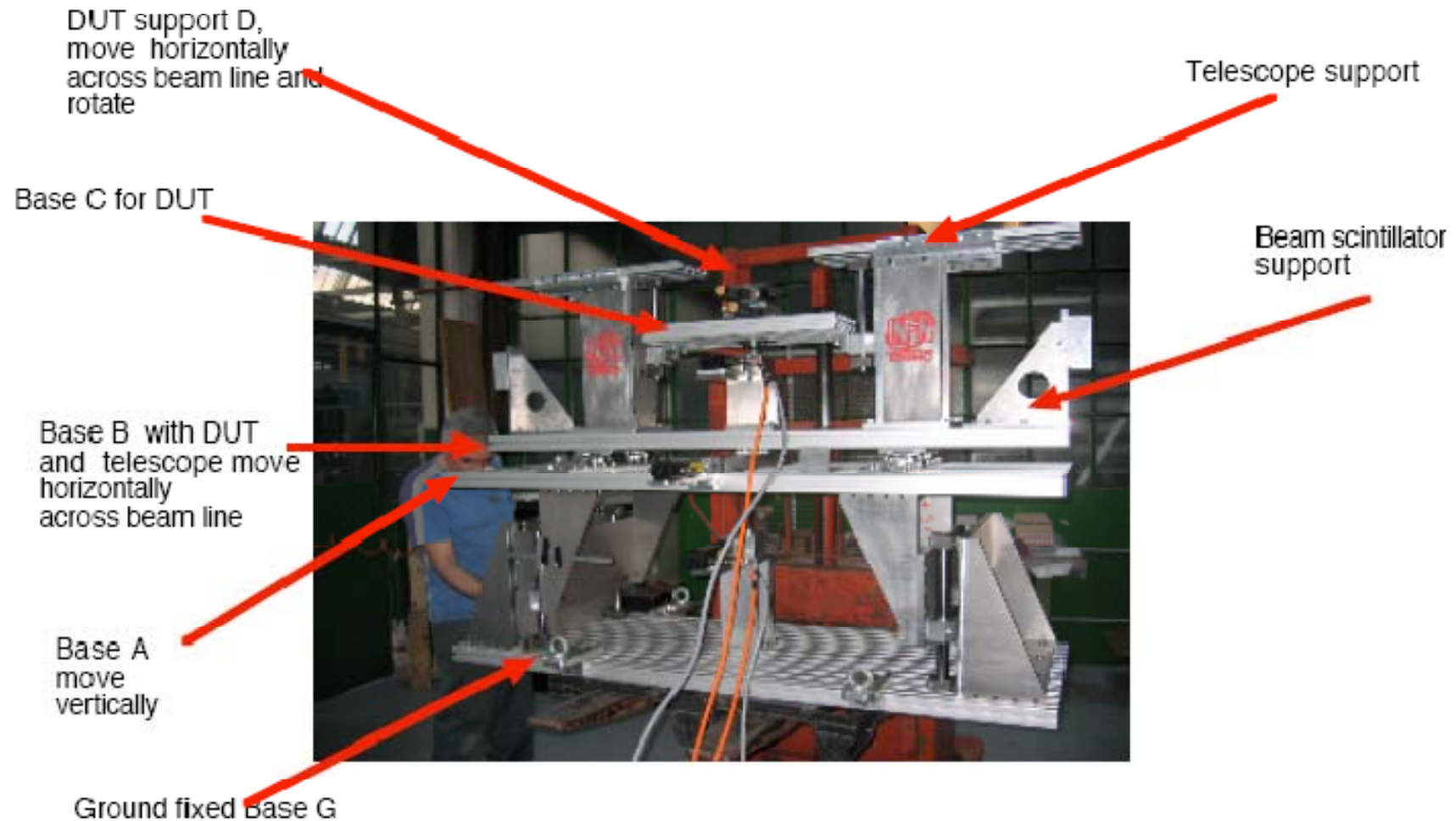


Actual FEE results: $\sim 0.6\text{mWatt/ch}$
No Power cycling included yet
→ Main problem: power
dissipation from neighbours

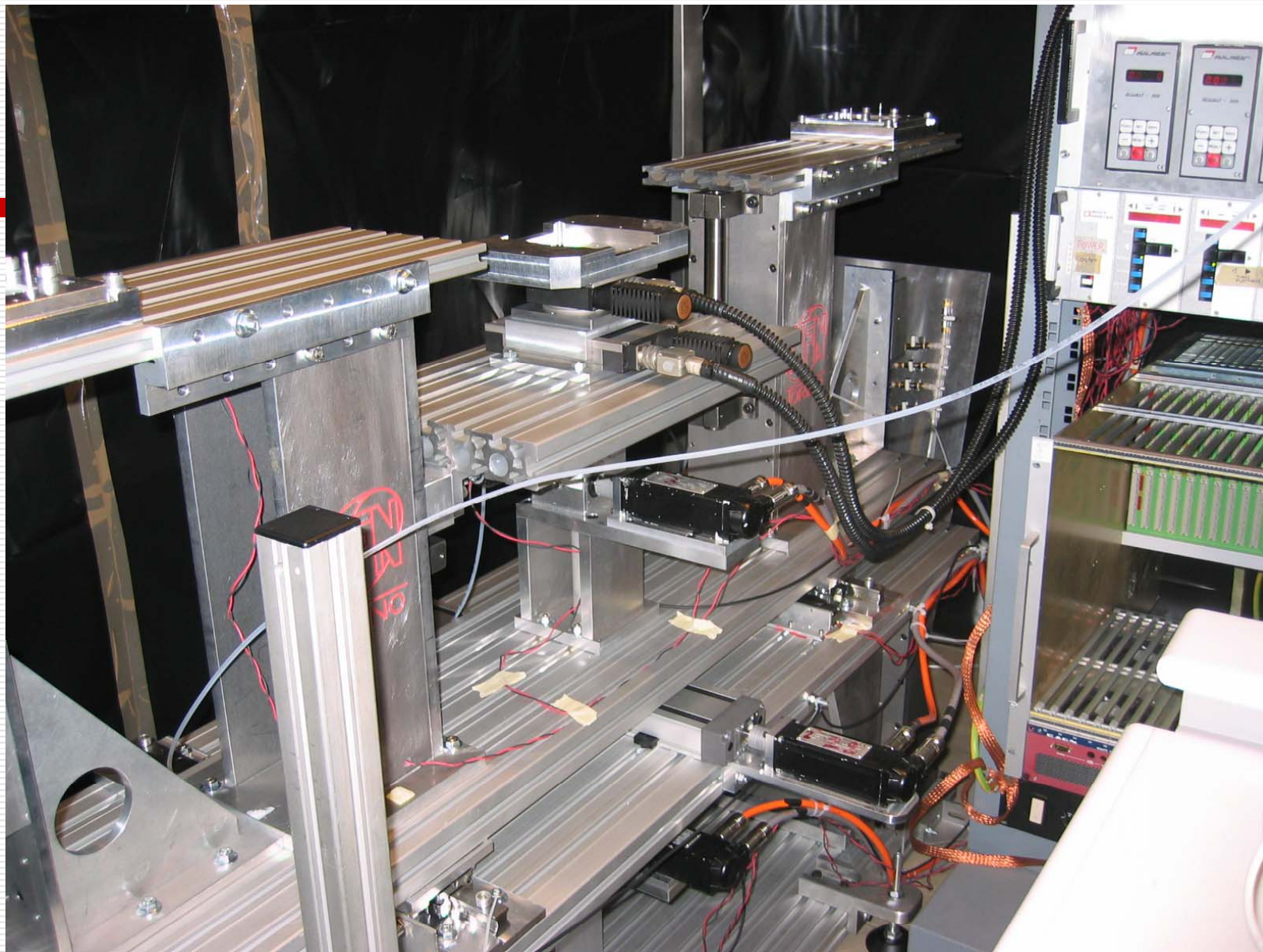
	Preamp	Shaper	Zero suppr	Pipe- line	Total Analog	ADC	Logic	Total Digital
180nm/ch	90	180			270			
130nm/ch	148	148	198	10	575	66		
Common				100		5	96	101

Motorised 3D Table (Torino)

- ❑ suitable for testing Silicon sensors, pixel and microstrips in a beam test,
- ❑ DUT can be moved and rotated with respect the beam line.
- ❑ built in a modular way, so that it can arrange different types of DUT, with alignment telescopes or without.
- ❑ 5 motors are controlled remotely via RS232, to set positions and angles, via LabView application
- ❑ Eudet-Memo-2007-59



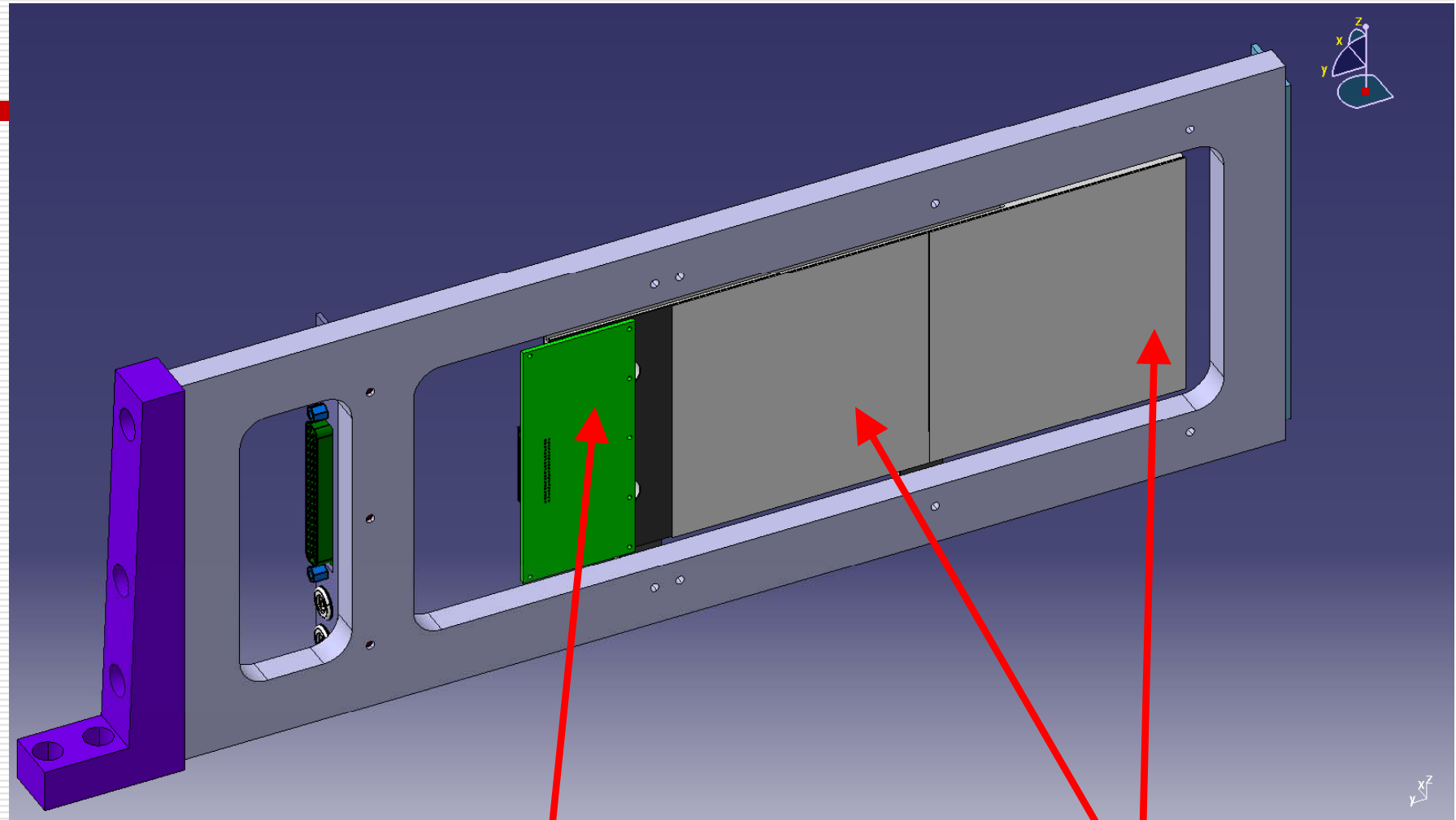
Movements:
Base A $DZ=28\text{ cm}$
Base B $DY=20\text{cm}$
Base C $DZ=16\text{cm}$
Support D, $DY=5\text{cm}, D\phi=\pm 90^\circ$



Central tracker prototype

- ❑ Several detecting module prototypes have been assembled with sensors and electronics
- ❑ Tested at Lab test bench
- ❑ Beam test at DESY and CERN

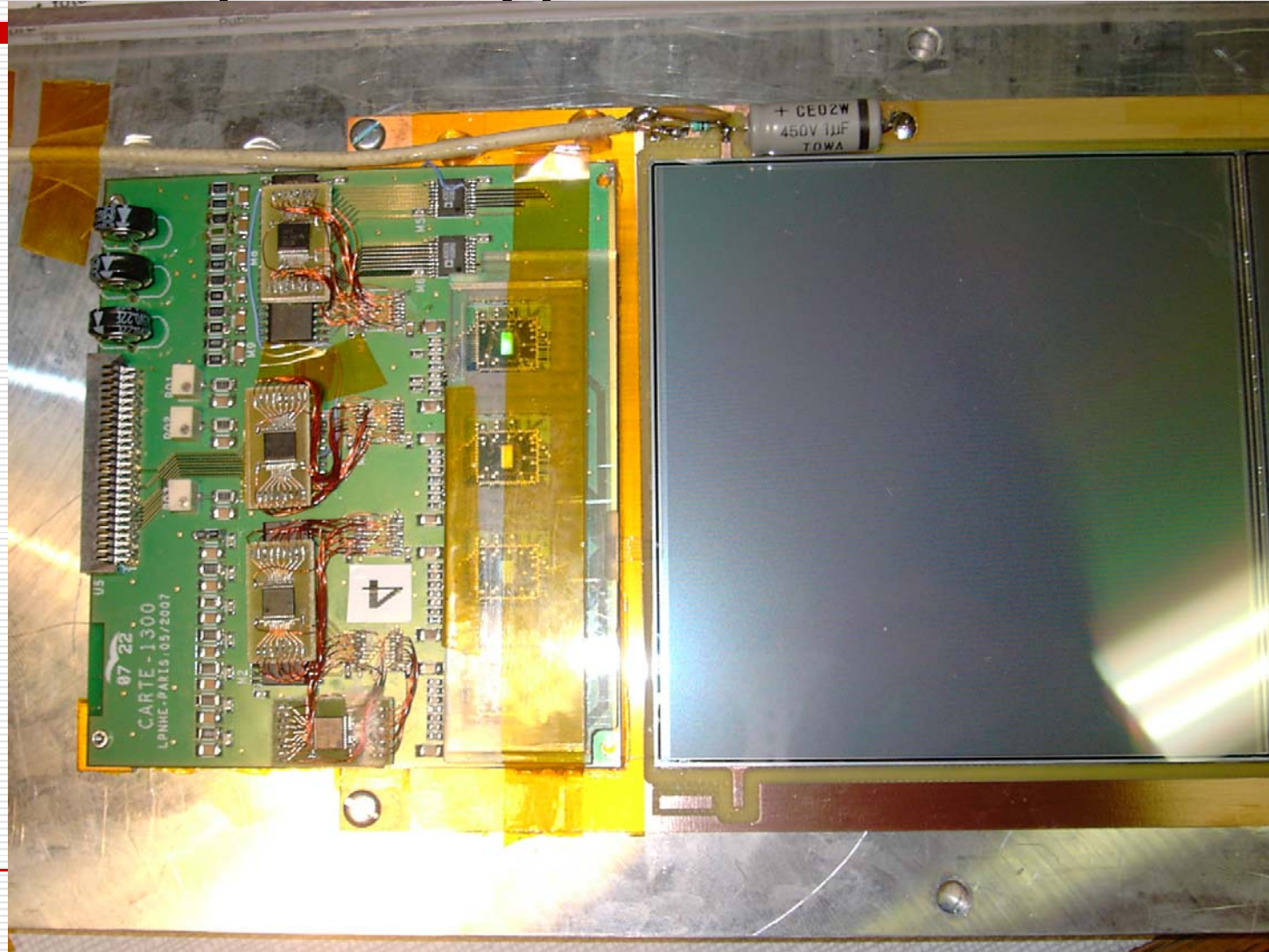
Module prototype



FE chip 130 um

2 HPK 6' sensors

Module prototype



FE Chip version 1 (LPNHE + Barcelona U.)

- ❑ After first prototype in 180 nm technology, 4-channel SITR-130_4 chip was designed in 130 nm and produced
- ❑ The chip was fully tested both standalone and with a strip sensor attached
- ❑ Based on the test results version 2 has been designed and submitted
- ❑ Version 1 documented in EUDET-Memo-2007-29

Front-end in 130nm

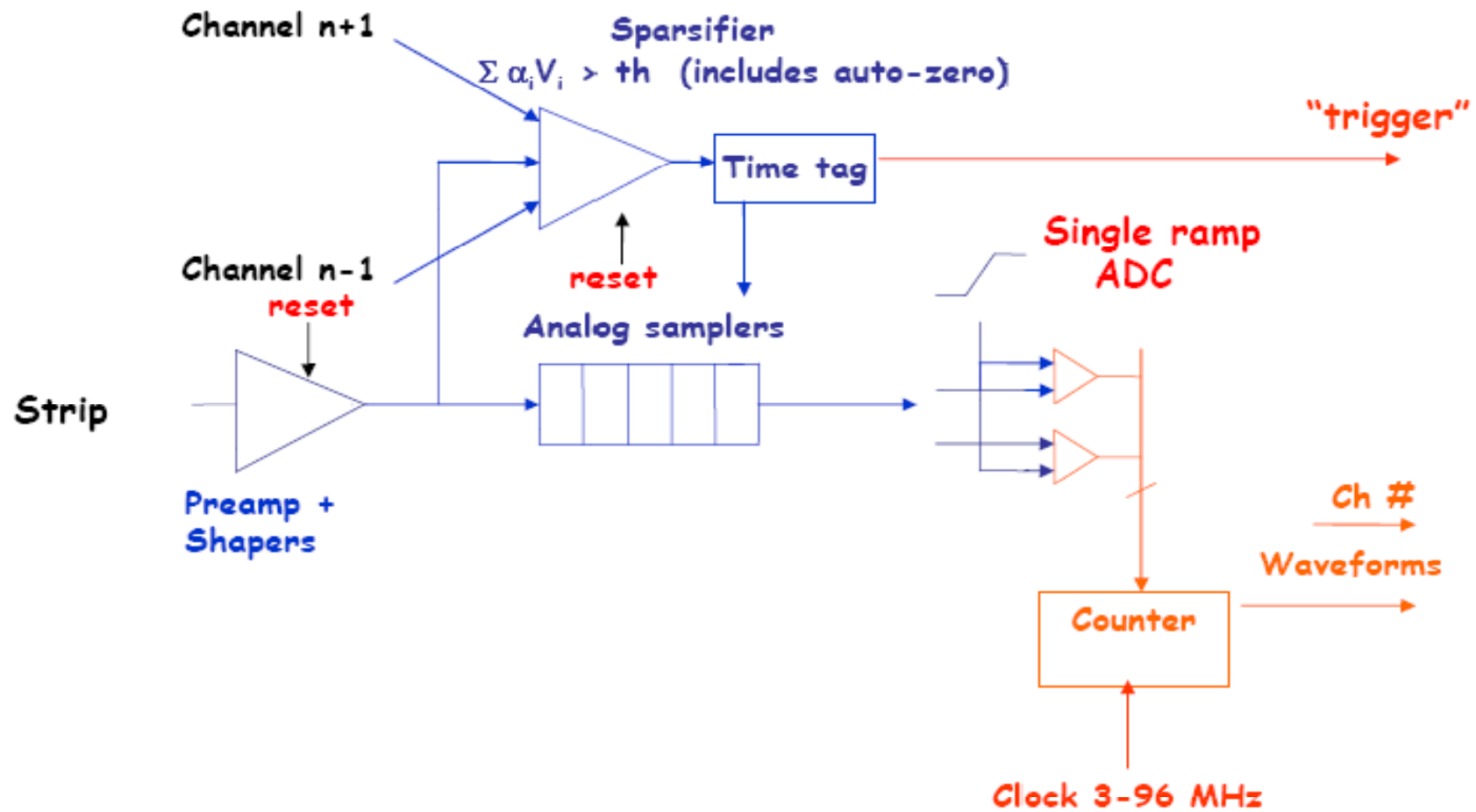
Motivation for 130nm CMOS:

- Smaller
- Faster
- Less power
- Will be (is) dominant in industry
- (More radiation tolerant)

Drawbacks:

- Reduced voltage swing (Electric field constant)
- Noise slightly increased ($1/f$)
- Leaks (gate/subthreshold channel)
- Design rules more constraining
- Models more complex, not always up to date

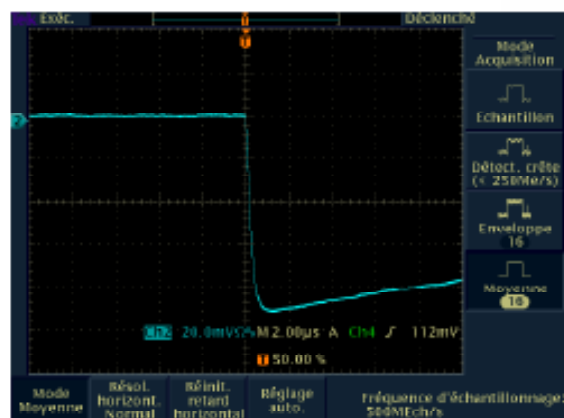
4-channel Chip



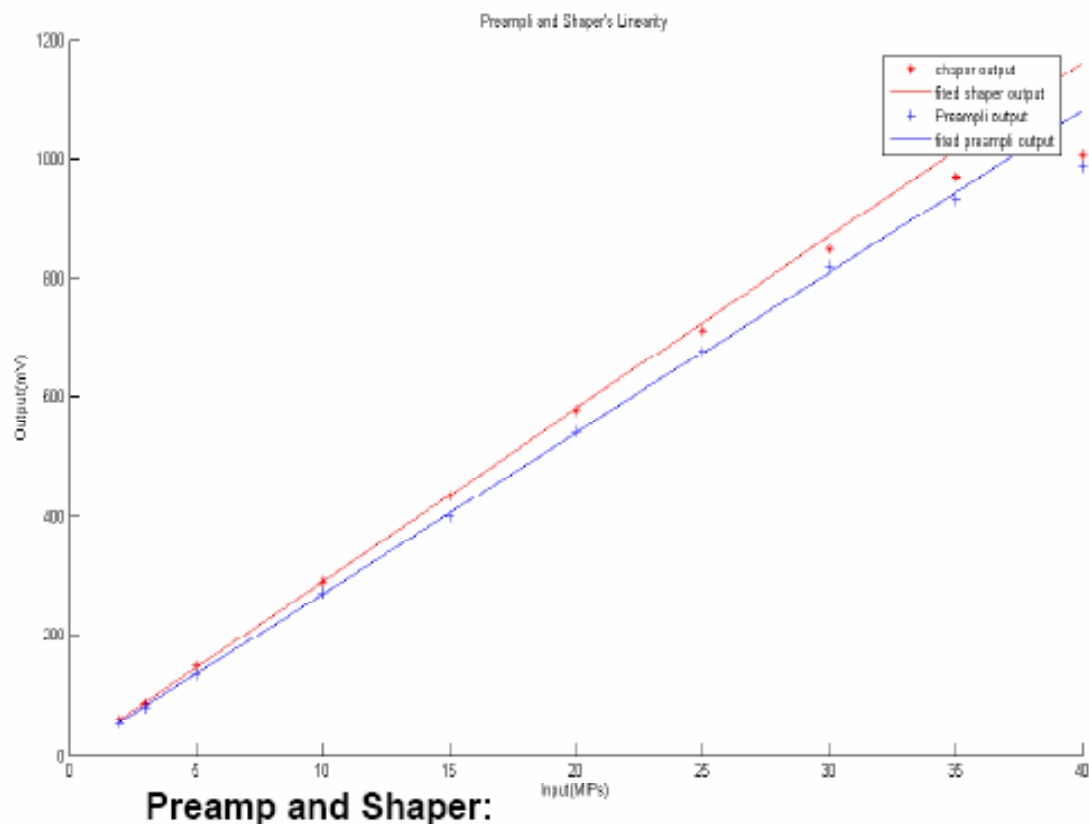
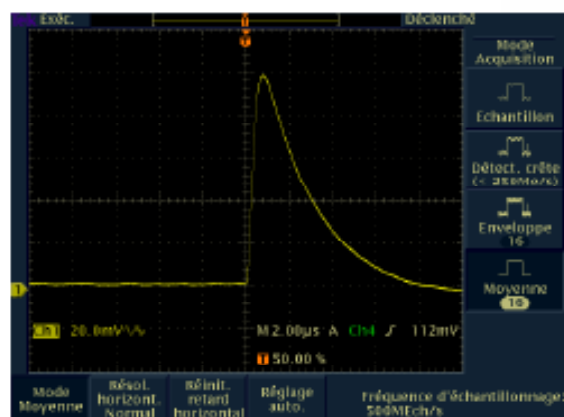
Preamp-shaper results

Measured gain - linearities

Preamp output



Shaper output



Preamp and Shaper:

Gain = 29mV/MIP
 Dynamic range = 20MIPs 1%
 30 MIPs 5%
 Peaking time = 0.8-2.5µs / 0.5-3µs expected

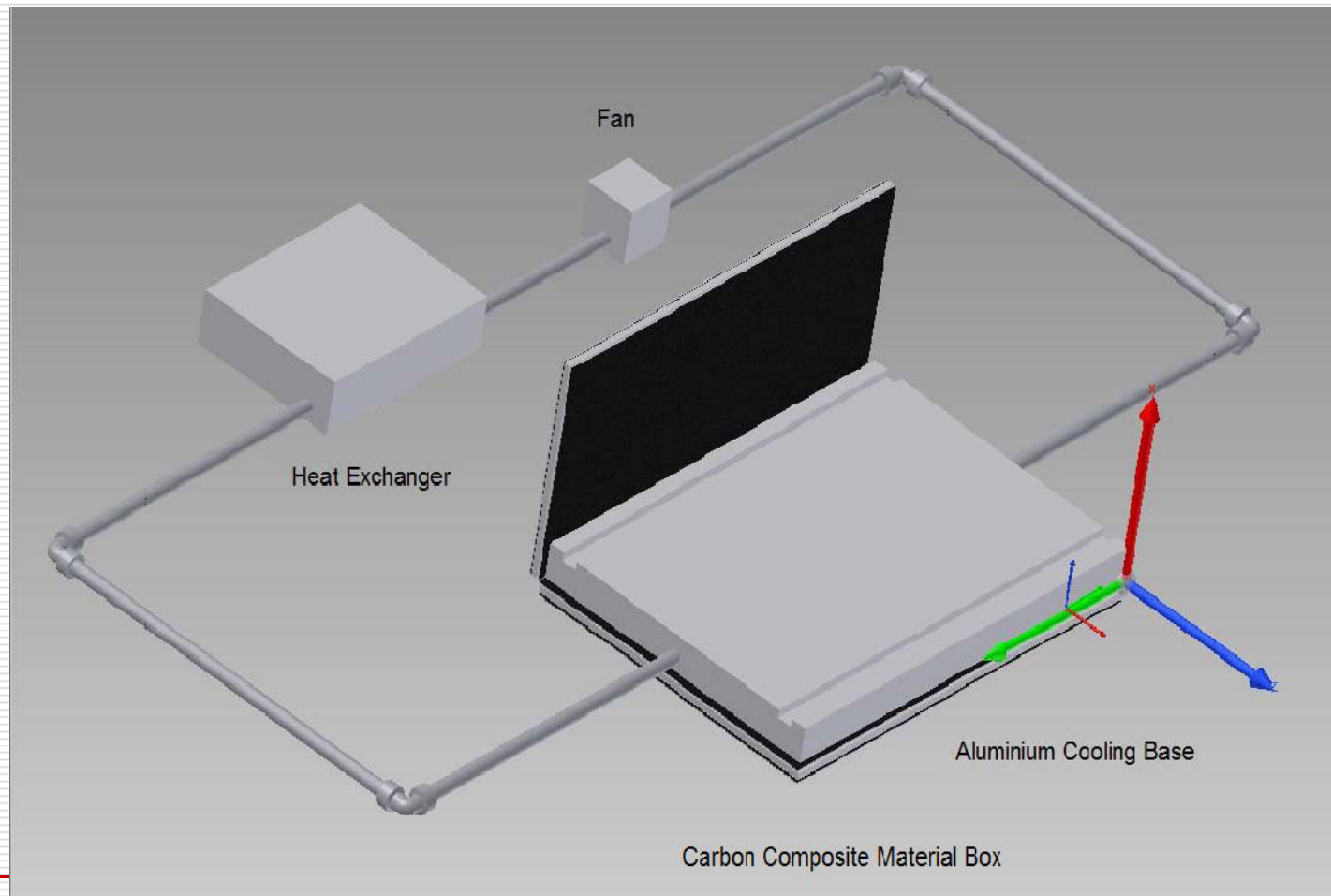
Milestones and Deliverables (Future)

Milestone Deliverable	Deadline	Status
Conduction cooling system prototype	36	In a good shape
Silicon tracking infrastructure	36	Move to 42?
Forward tracker prototype	36	Move to 42?
FE chip version 2	36	In a good shape

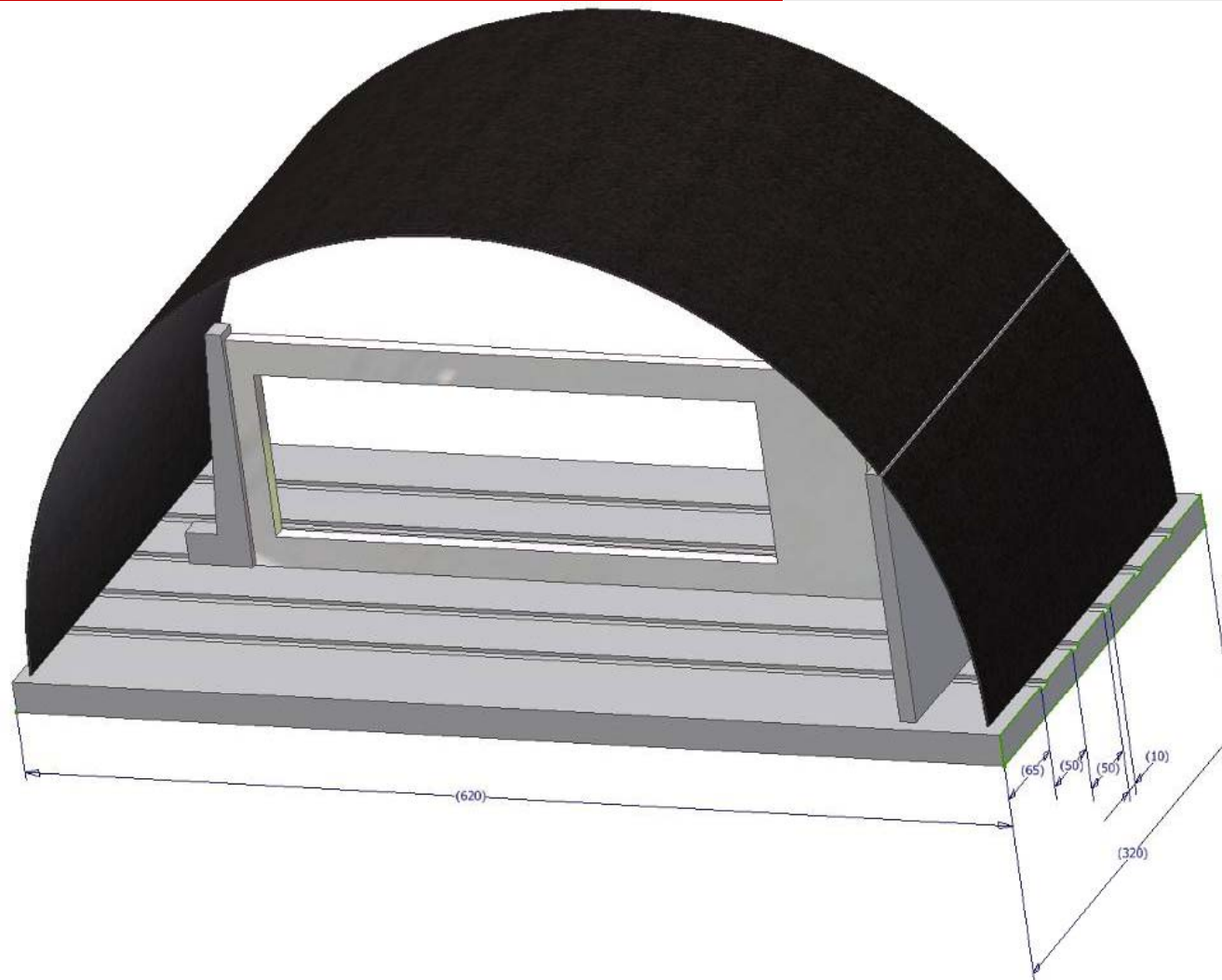
Conduction Cooling System Prototype

- ❑ Designed by LPNHE and OSU
- ❑ Description, calculations and test results in Eudet-Memo-2007-52
- ❑ Conventional material prototype ready for October 2008 CERN beam test
- ❑ EUDET prototype will be built afterwards from composite carbon fibre structures

Conduction Cooling System Prototype: Principle



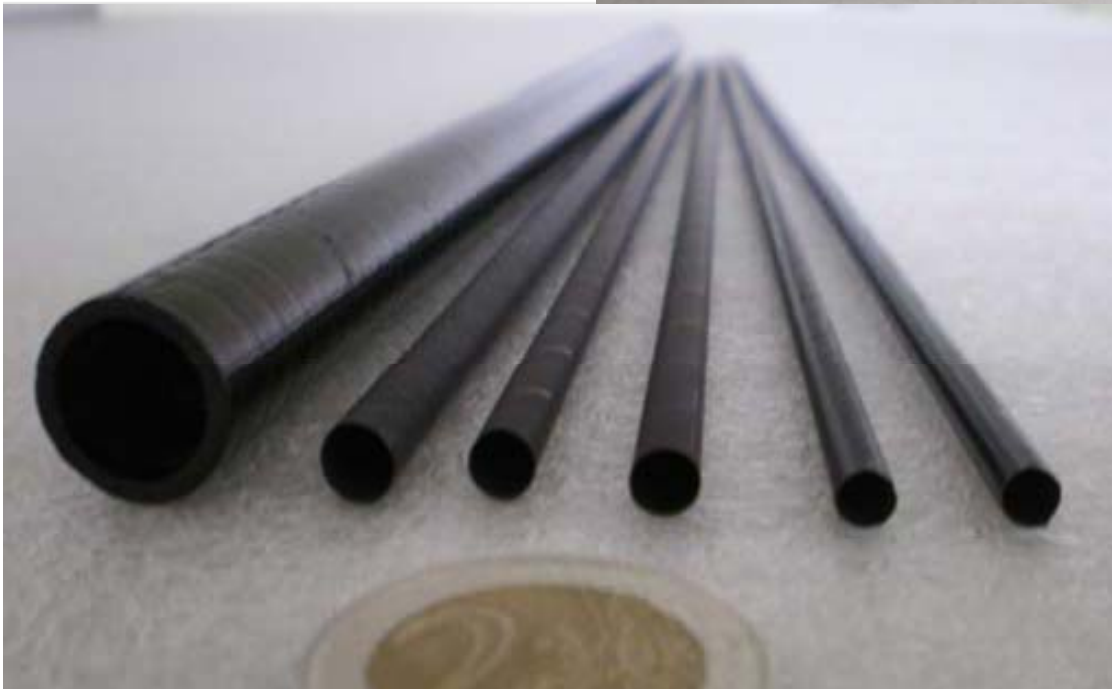
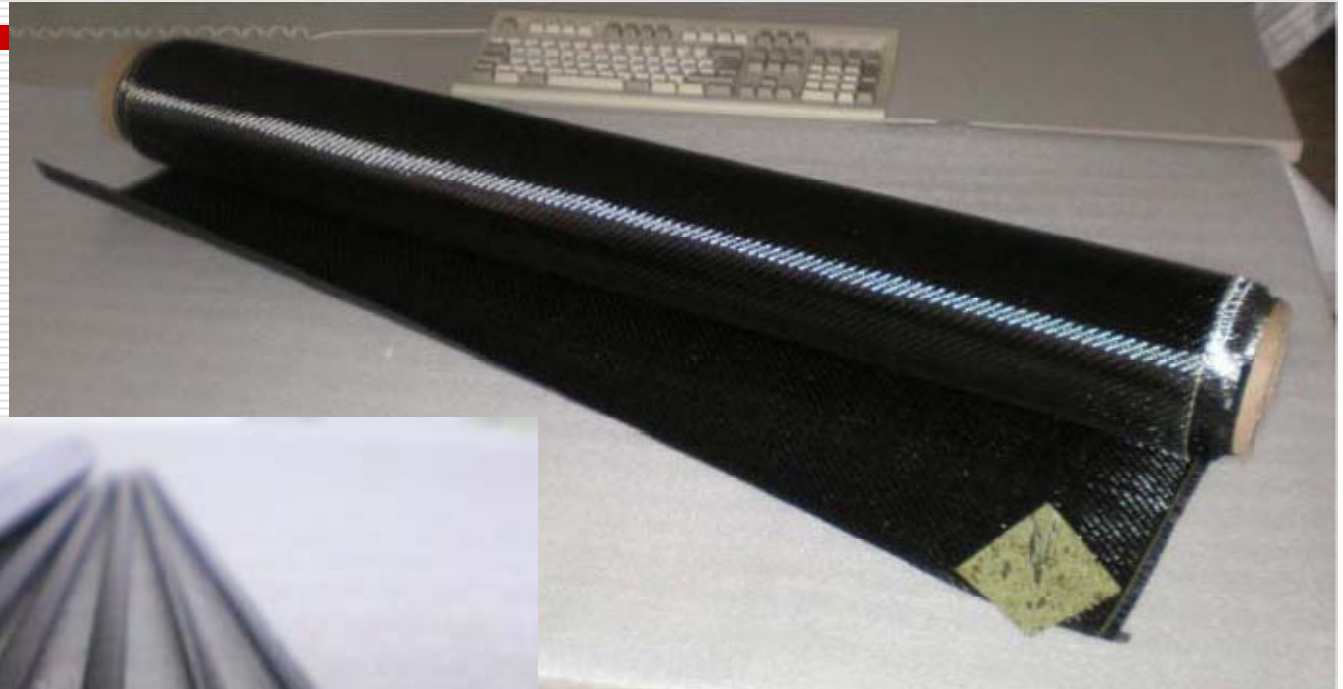
Conduction Cooling System Prototype: Module box



Composite materials

Honeycomb

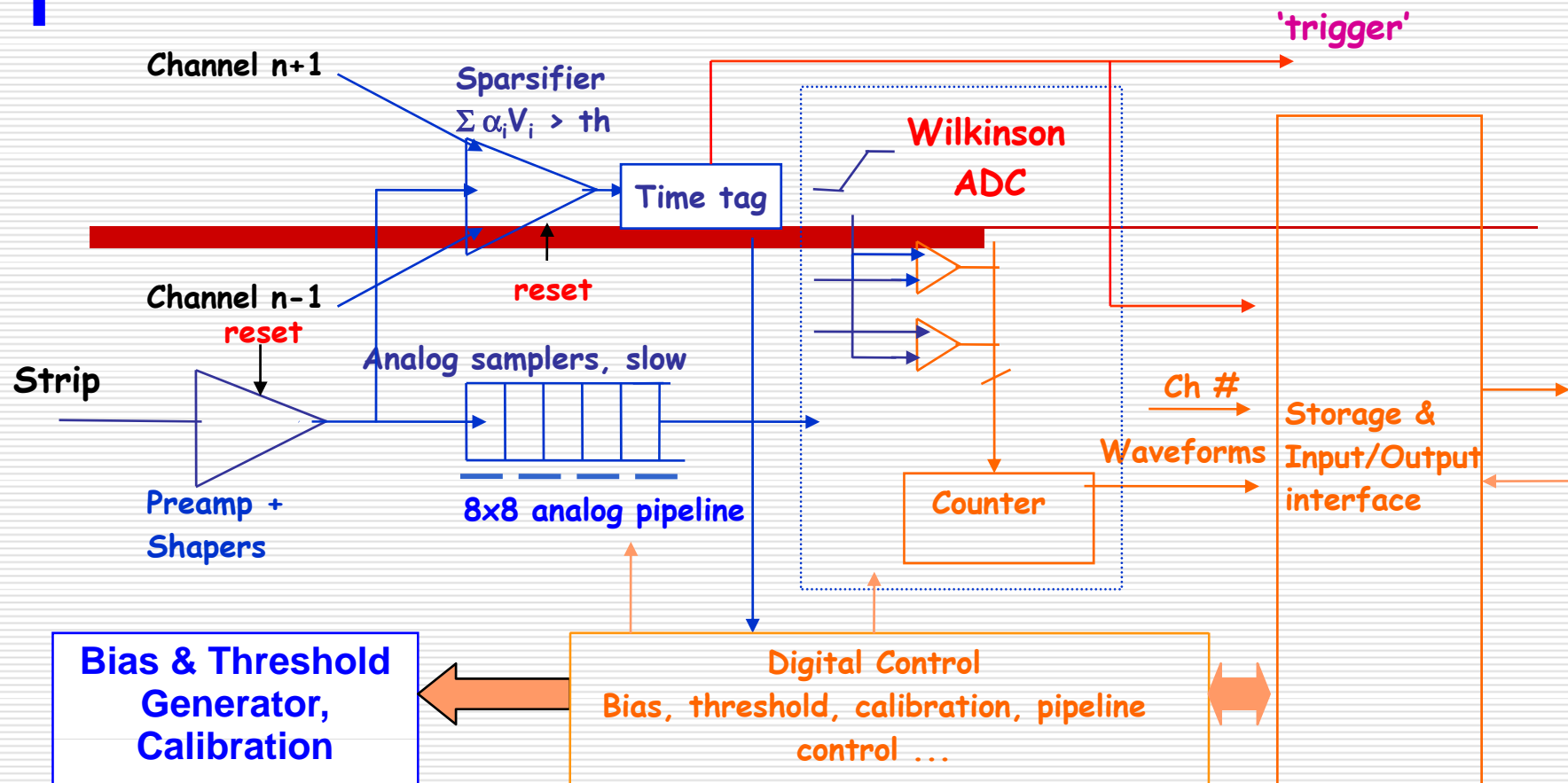
Low material budget



FE Chip version 2 (LPNHE+U. Barcelona)

- ❑ After successful tests of FE version 1 chip (SITR-130_4) 88-channel version was designed in 130 nm and submitted
- ❑ Expected delivery from the foundry is September
- ❑ After thorough testing chip will be assembled into detecting modules

General view of the circuit



Main features of new circuit

88 channels (1 test channel): Preamplifier, shaper, sparsifier, analog pipeline (8x8 cells), 12 bits ADC

2D memory structure: 8x8/channels

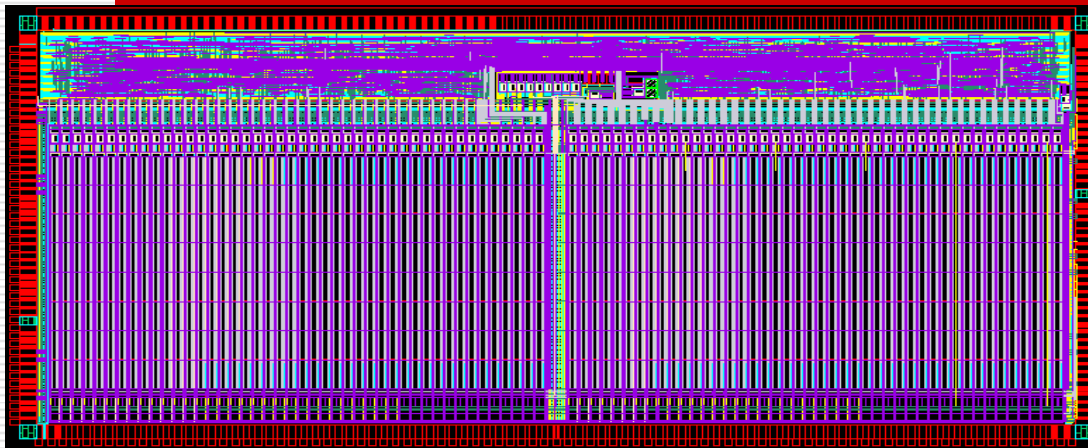
Fully digital control:

- Bias voltage(10 bits) and current (8 bits)
- Power cycling (in optional)
- Shaping time programable
- Sampling frequency programable
- Internal calibration
- Sparsifier's threshold programable per channel
- Event tag and time tag generation

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2 Trigger modes: Internal (Sparsification intergrated)
External (LVTTL) for beam test

LAYOUT VIEW



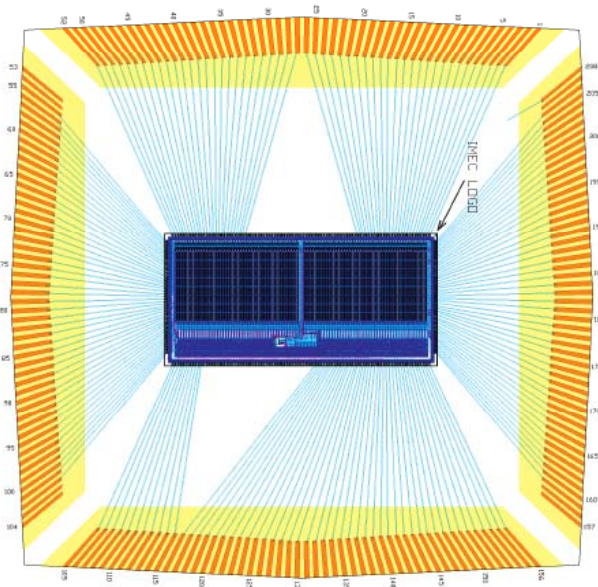
Size: 5mmx10mm
88 channels (105um pitch)
105umx3.5mm/channel

Analog: 9.5mmx3.5mm
Digital : 9.5mmx700um

Submitted June 24th '08

New readout circuit in 0.13 μm

BONDING DIAGRAM FOR CQFP208 PACKAGE



- Package 208 pins
- 50 analog input
 - 21 analog test out
 - 33 digital pin (22 test pins)
 - 107 supply pins

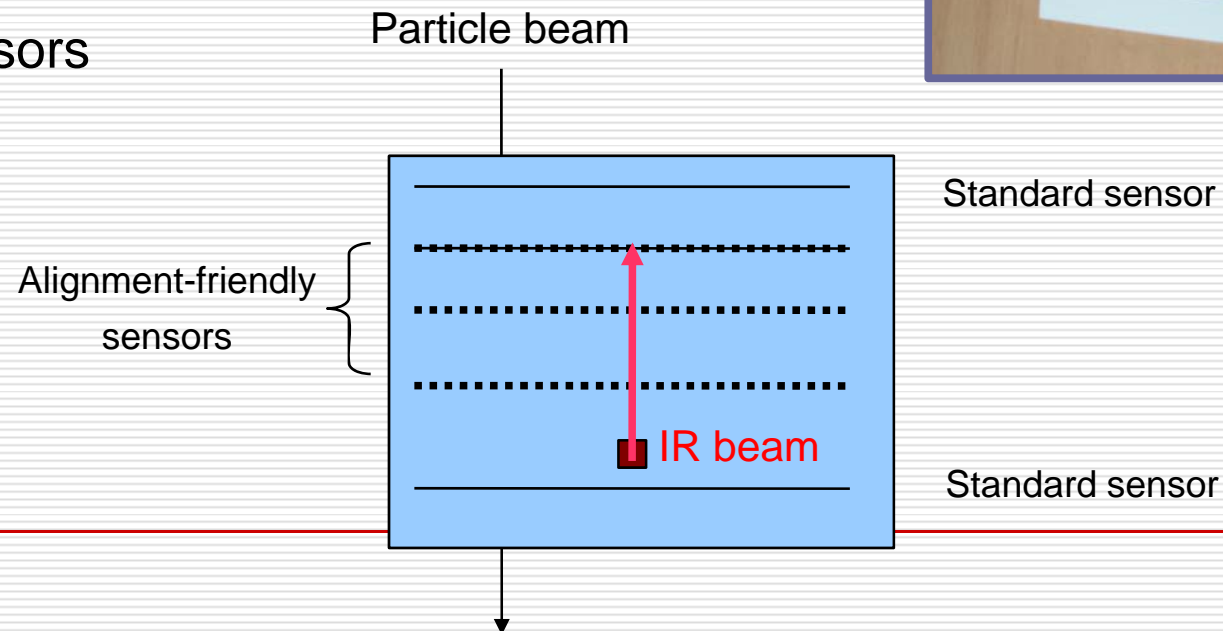
Forward tracker prototype

- ☐ Detector modules equipped with special alignment sensors
- ☐ IR Laser alignment will be performed
- ☐ These modules will be tested at October CERN beam test
- ☐ this deliverable would benefit from postponing the deadline from M36 to M42

Alignment prototype on beam

24th Sept-8th October test beam will study performance of new HPK alignment sensors
These are “standard” sensors with an Al-free window in the backside (ohmic contact)
IR beam pseudotrack can be used to traverse several sensors

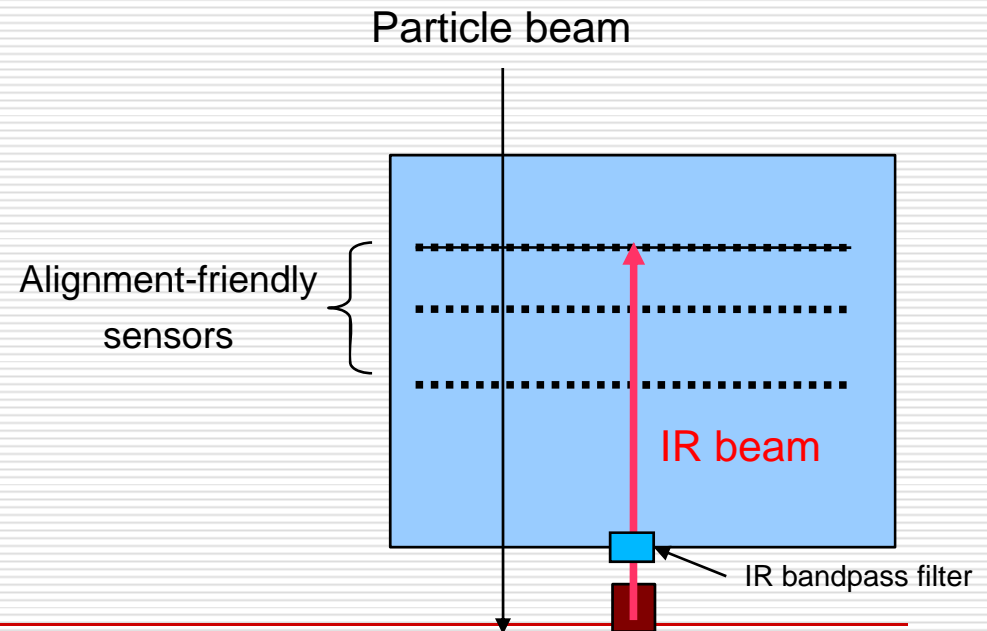
Ohmic side:
Alignment
passage



Alignment prototype on beam

- 1) Show that the performance of the alignment friendly sensors is the same as the standard ones
- 2) Compare track reconstructed geometry to IR beam reconstructed geometry
- 3) Shift only central alignment sensor and compare reconstructed displacement with particle beam and with IR beam

The same setup employed in the test beam can be used as well as an alignment monitor. We just need an IR transparent window in the front side of the cage (it can be a small bandpass filter).



Silicon tracking infrastructure

- ☐ Various facilities needed for successful detector testing
 - Cooling
 - Alignment
 - 3D motion
 - Tracking
- ☐ Integration of the other deliverables
- ☐ Could be together by M36, but would be of better quality if postponed to M48

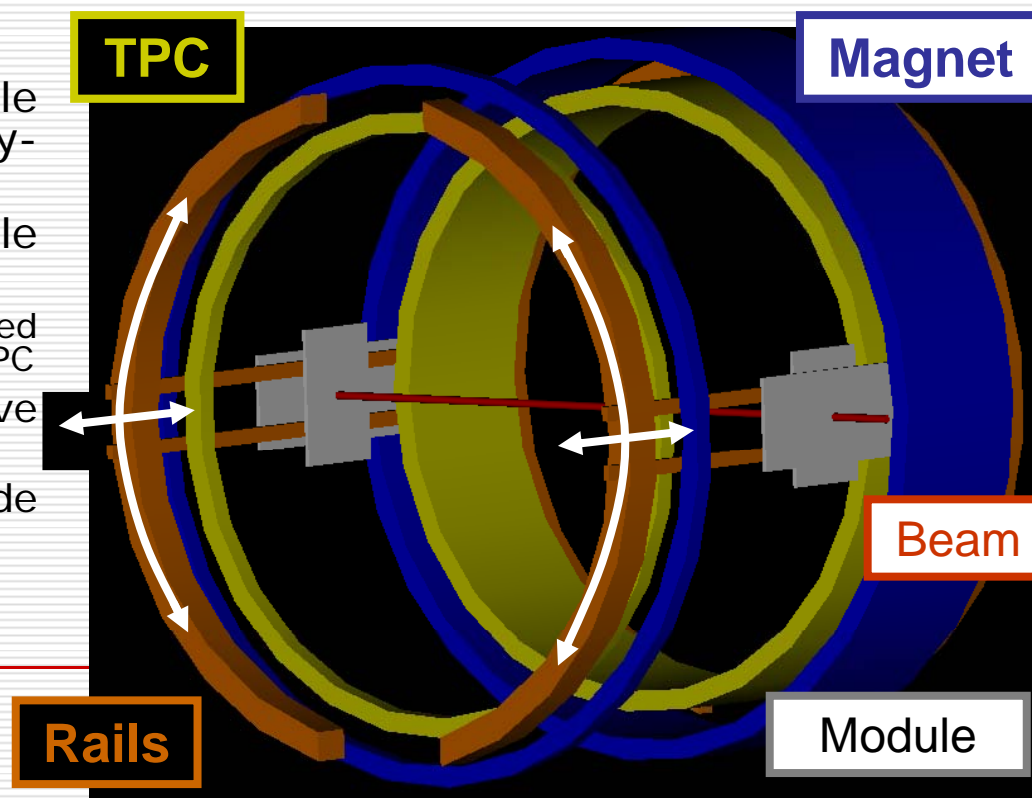
LP-TPC: Silicon Envelope (HEPHY, IEKP Karlsruhe)

□ **four silicon modules** will be installed:

- two in front and two behind the TPC, with respect to the e-beam
 - two independent support structures are needed
- on each side:
 - one horizontal module consisting of two daisy-chained sensors
 - and one vertical module consisting of one sensor

□ **movable support system** is needed because it must be possible to scan the TPC

- the TPC and the magnet will move relative to the beam
- the sensors have to stay inside the beam line



Memos + Reports

Year	Memos	Reports
2006		1
2007	9	
2008	~ 6	~1

Other SITRA/SiLC activities

(not included in EUDET but necessary for successful EUDET accomplishment)

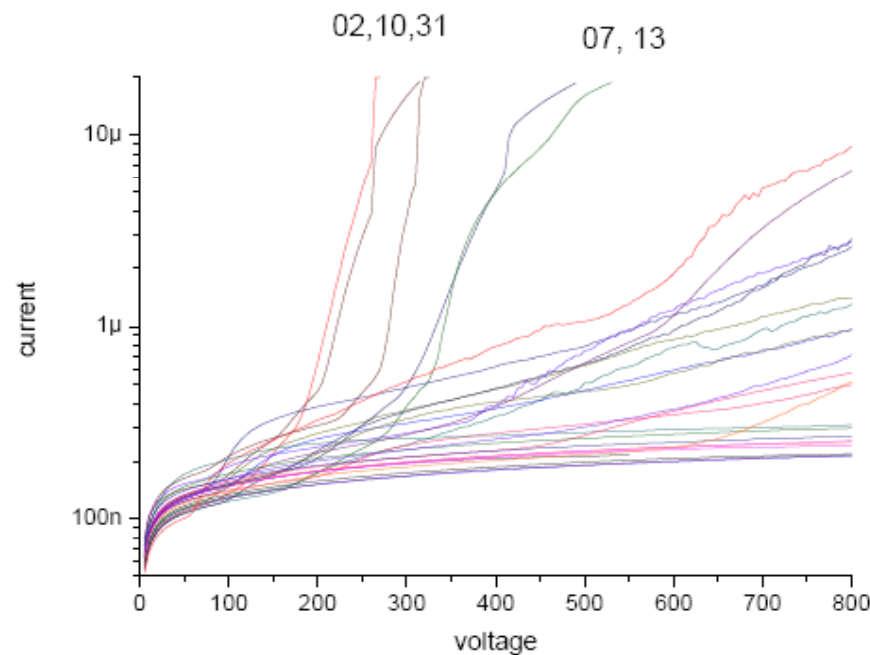
- ❑ Si sensor development, production and testing
- ❑ Module construction (engineering, tooling)
- ❑ DAQ (FPGA, off-detector, TLU/EUDET integration)
- ❑ Lab and beam tests
- ❑ Simulations

Si-sensors

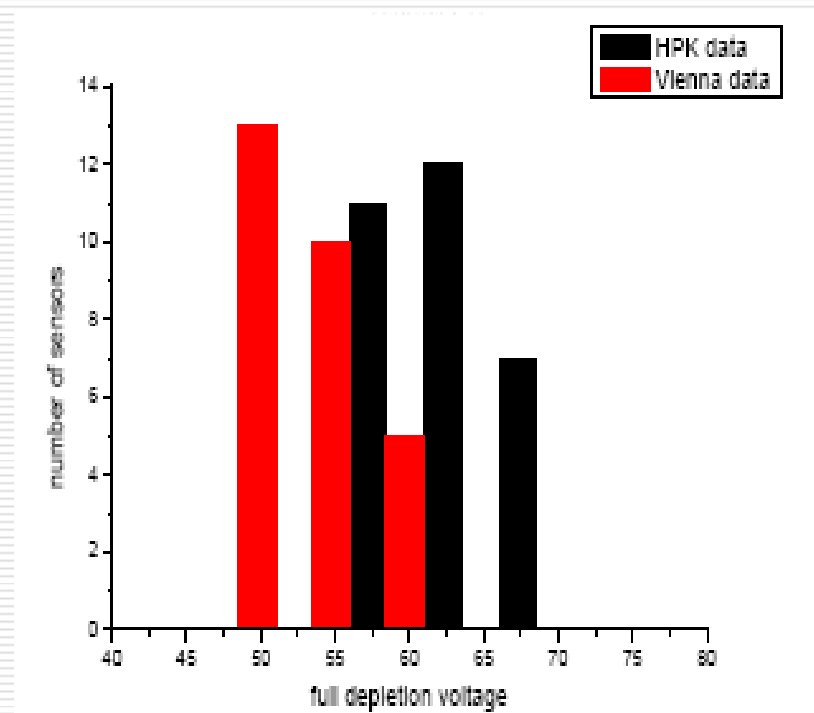
- ❑ Dedicated SiLC strip sensors designed by HEPHY and manufactured by HPK
- ❑ Test structures already tested in the beam test (June 2008, CERN)
- ❑ Full-sized sensors with alignment treatment will be tested at CERN in October
- ❑ VTT 3D structures

HPK strip sensors

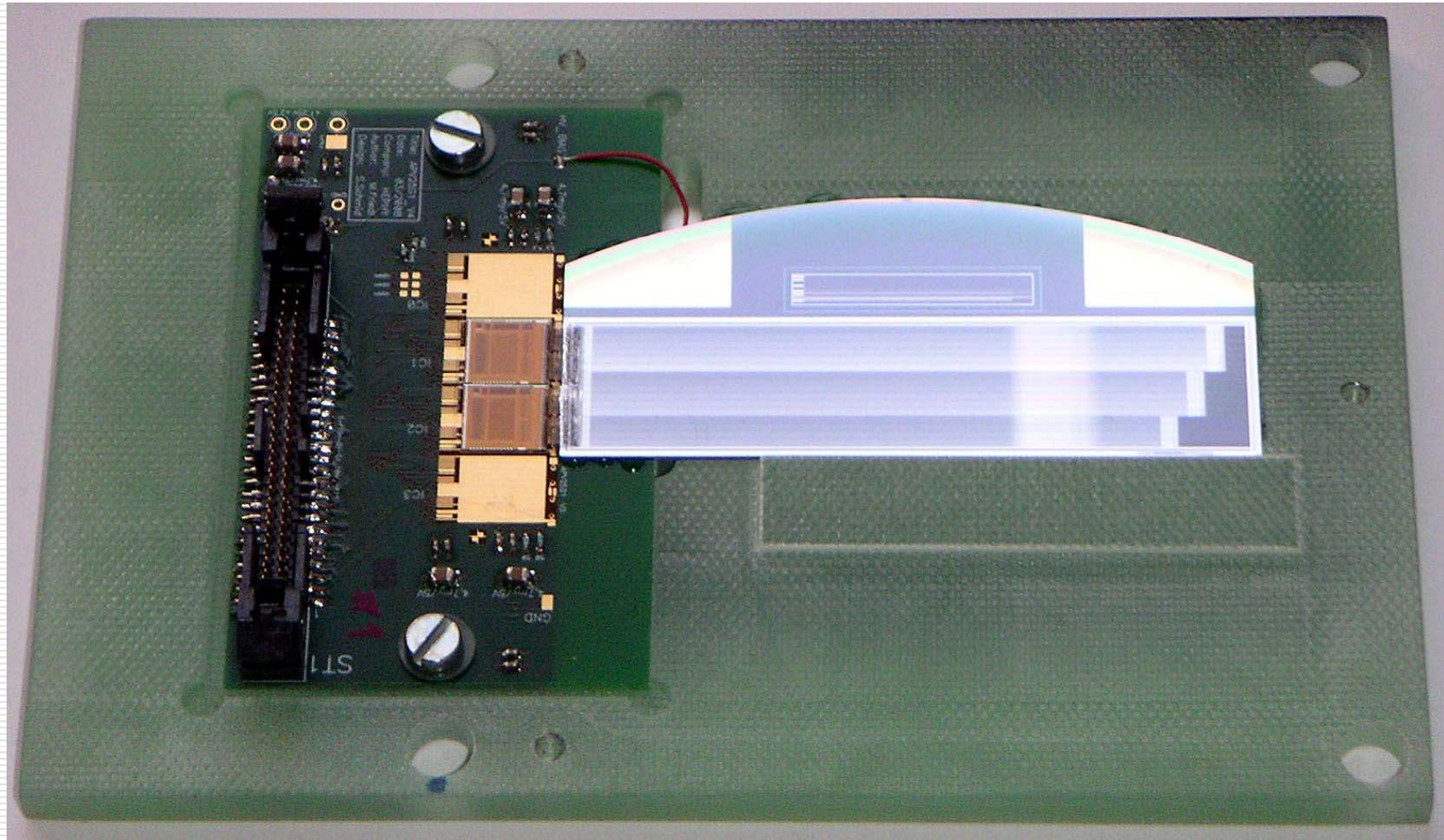
IV curves



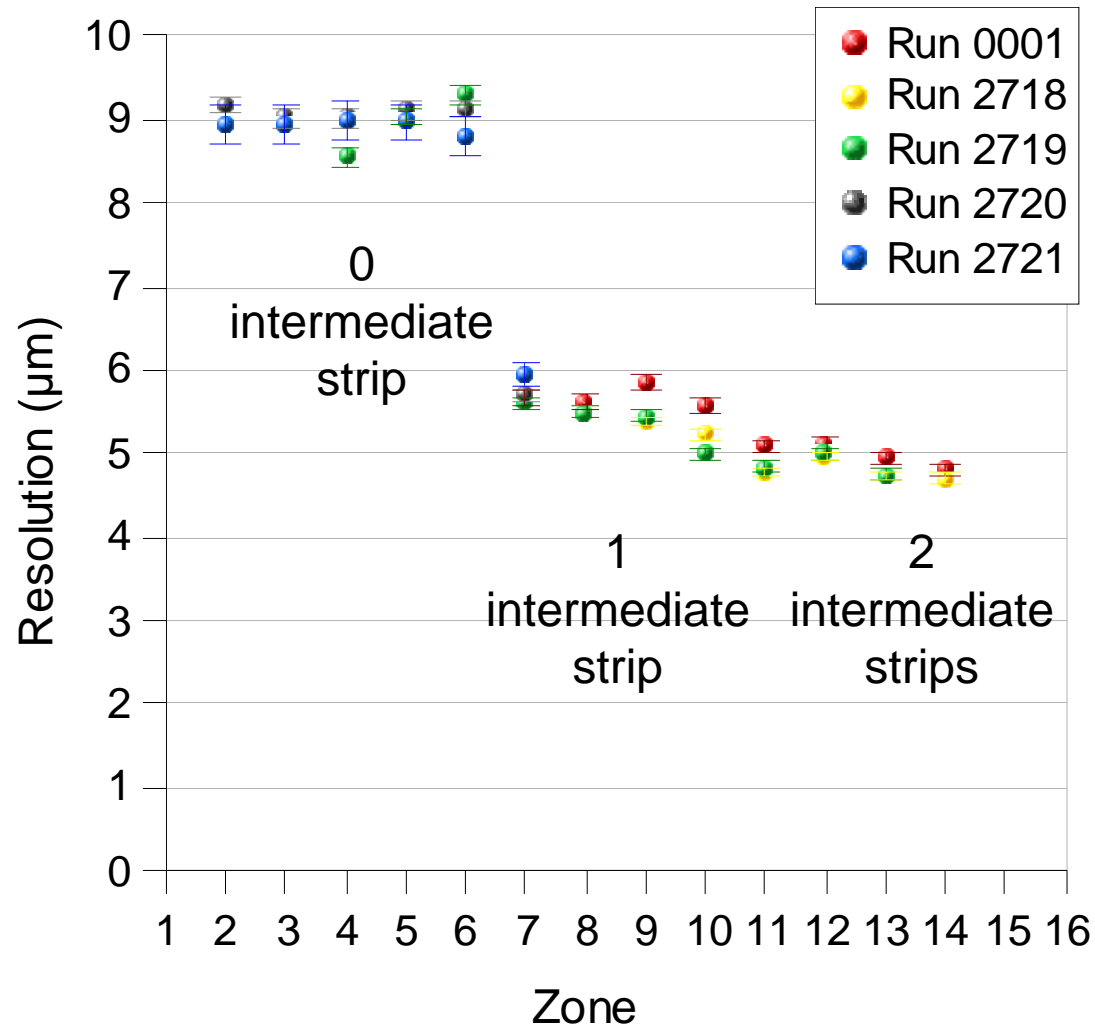
Depletion voltage



DUT with HPK test structures at CERN beam test



Spatial resolution vs. strip geometry



- 50 μm r/o pitch
- 0,1 or 2 intermediate strips)

Beam tests

- 2008 (CERN):
 - June: Hamamatsu test structures
 - Sep-Oct: Hamamatsu alignment sensors
- 2009
 - March: DESY, FE chip+HPK sensors
 - Later: CERN (HE beam)
 - Later: FNAL (combined)

Conclusions

- ❑ Past deliverables: all completed
- ❑ 4 M36 deliverables:
 - 2 almost complete
 - Other 2: SITRA working with full speed towards completion, but postponing the deadline to M42 or M48 would allow higher quality results