Clock & Control Timing and Link

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Matt Warren
Maurice Goodrick, Bart Hommels, Marc Kelly,

Timing Overview

- C+C provides a fast clock (CLOCK)
  - Expected to be 50-100MHz, local or machine.
- CCC does NOT support varied delays on individual outputs.
- LDAs do not adjust individual link timings
  - Presumed cables to all LDAs equal length in a timing domain.
- Hoped that DIFs can adjust own timing if really needed using FPGA resources.
- CCC card can adjust timing of synchro-signals wrt CLOCK
- BUNCH-CLOCK (slow clock) derived as CLOCK/n
  - Produced by a counter on the DIF
- Start of train signal (TRAINSYNC) synchronises bunch-clocks on all DIFs.
  - Requires fixed-latency signal – a SYNCCMD.
  - SYNCCMD "qualifies" CLOCK edge

CCC Link Interface

- CCC should connect to LDA, DIF and ODR using the 'standard' HDMI cabling and connectors and pinout (*CLink*)
  - But only a subset of the signals/functions used.
  - CCC can be used as a pseudo-LDA for stand-alone DIF testing
- A distinction is made between fast and fixed latency signals.
  - Fast signaling is asynchronous and uses a dedicated line to transfer a pulse. No attempt is made to encode data.
  - Fixed-latency signaling will not arrive fast, but will arrive a known latency after reception by CCC.

HDMI Signals			
CLink Signal	***Direction***	***Function***	***Type***
CLOCK_L2D	LDA→DIF	Distributed DIF Clock	STP
DATA_L2D	LDA→DIF	Data to DIF (mainly configuration)	STP
DATA_D2L	DIF→LDA	Data from DIF (mainly events)	STP
ASYNC_L2D	LDA→DIF	Asynchronous trigger	UTP*
GEN_D2L	DIF→LDA	General use	STP

* Twisted pair not guaranteed by HDMI specification but seen in commercial cables

CCC Link Signals

CCC HDMI Signals		
CLink Signal	***CCC Signal***	***Function***
CLOCK_L2D	CLOCK_OUT	Clock
DATA_L2D	TRAINSYNC_OUT	Trainsync signal output
DATA_D2L	Unused	Unused
ASYNC_L2D	ASYNC_OUT	Asynchronous signal
GEN_D2L	GEN_IN	General purpose

- ***CLOCK***
  - Machine clock (50-100MHz)
- ***TRAINSYNC_OUT***
  - Synchronisation of all the front-end slow clocks.
  - An external signal will be synchronized to the clock and transmitted as a single clock-period wide pulse to the LDA.
  - To allow communicating with a stand-alone DIF, the CCC board will can be configured to send the LDA 8b/10b serialised command for train-sync.
- ***ASYNC_OUT***
  - Transfer asynchronous triggers as fast as possible.
- ***GEN_IN***
  - General purpose signal for use in communicating with the CCC (and therefore run control) system. A hardware OR of these signals is available on the CCC.

SYNCCMD Details

- SYNCCMD is the ONLY mechanism for synchronising DIFs
  - 4 types of command are possible, but only one is required.
- Expects a *PRE* bunch-train/spill signal
  - Signal in known phase with BUNCH CLOCK
  - Hopefully PRE-signal is a fixed period prior to first bunch of train
  - Synchronous to CLOCK
- CCC card forwards signal to LDAs
  - Synchronises signal to local clock when needed
- LDA stores arrival time wrt serialised bit number.
- Next Word to DIFs replaced with special SYNCCMD word
  - First byte dedicated K character
  - Second byte (7:6): Type; (5:0): Delay (could be 3:5 ratio too)
- SYNCCMD system on DIF delays signal specified number of CLOCKs and issues the required signal.