Si-W ECAL
Silicon wafers status

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LLR

Si overview

see my presentation at Manchester

- Hamamatsu : I(V) ok, C(V) ok, C(V,t) understood, glue ~ok
  - New size (324 pixels updated to 256 pixels)
  - Have guard rings ! External charge injection shows square events… Hamamatsu answered to bias them…
  - Large dead space : new version with 25% less dead space
- Orders for EUDET
  - Hamamatsu : ordered tomorrow
    - Yen/€ parity is an issue (165 4 months ago, 115 now : -40% !)
    - 70 k€ = ~40 sensors (70% of a slab or 5 shorts SLABs)
  - Others : delayed
- Search for new design techniques
  - Segmented guard rings to avoid square events
  - Thin edge
  - Dead space reduction

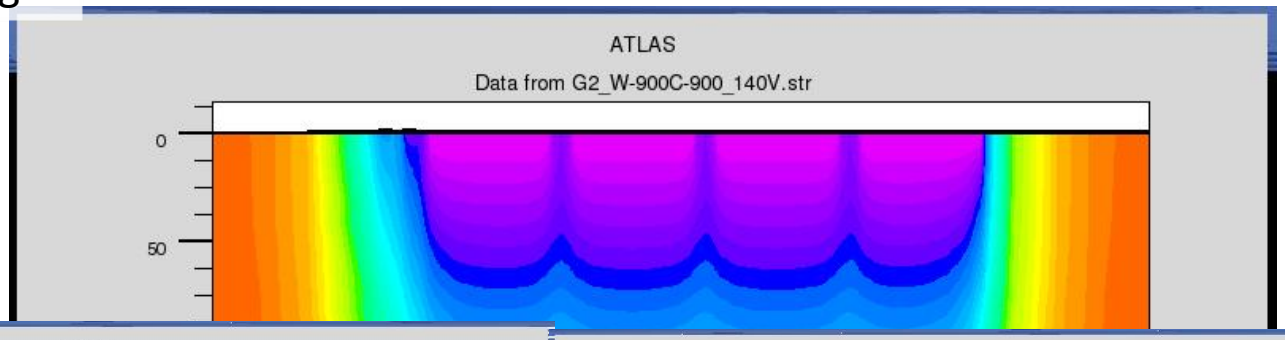
1500 € rebate negotiated this morning

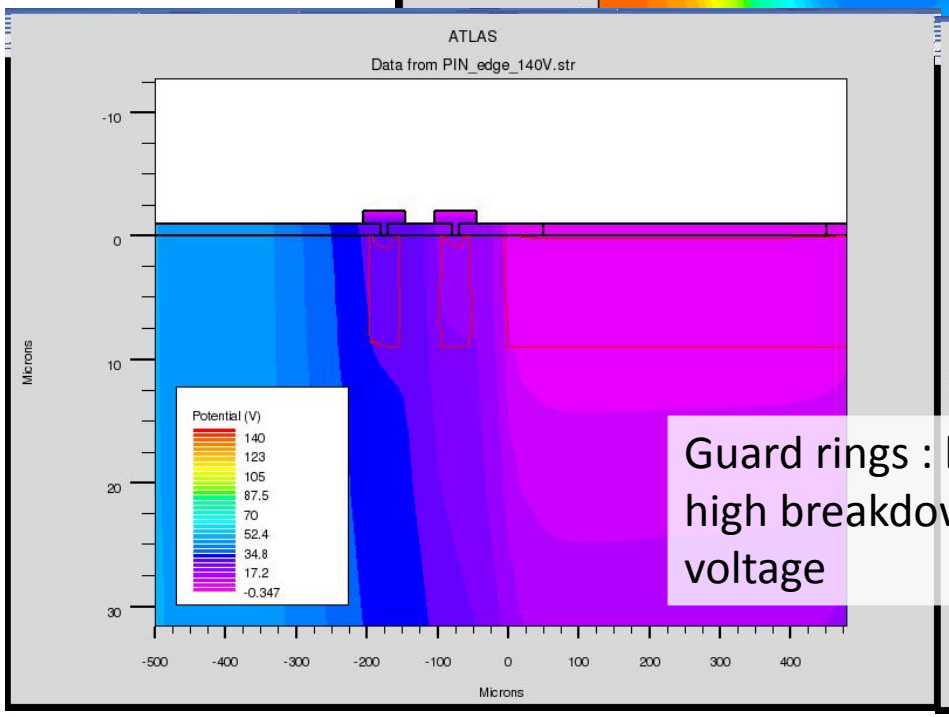
Si design

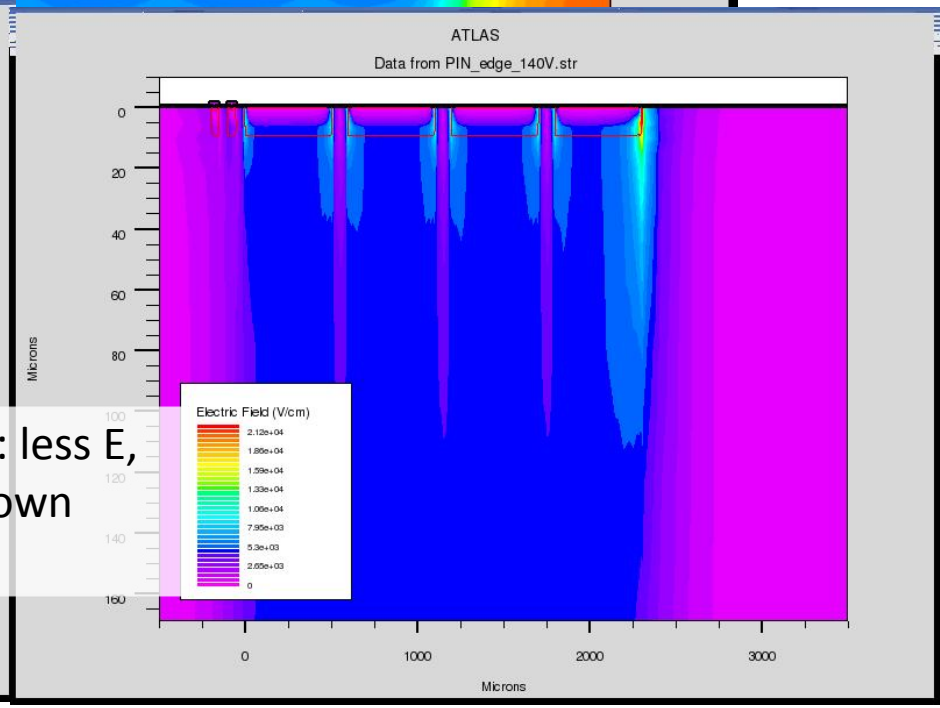
- The simplest design to control the cost
- Drawbacks : lack of optimization
  - Large dead zone at the edges
  - Floating guard rings make crosstalk possible
- Many others well known techniques
  - But costs ?
  - Design effort : simulation at first
- Disclaimer : all simulations included in this talk are doubtful, simplistic and wrong

Simulation : basic sensor

4 pixels (500 um),
500 or 700 um edges



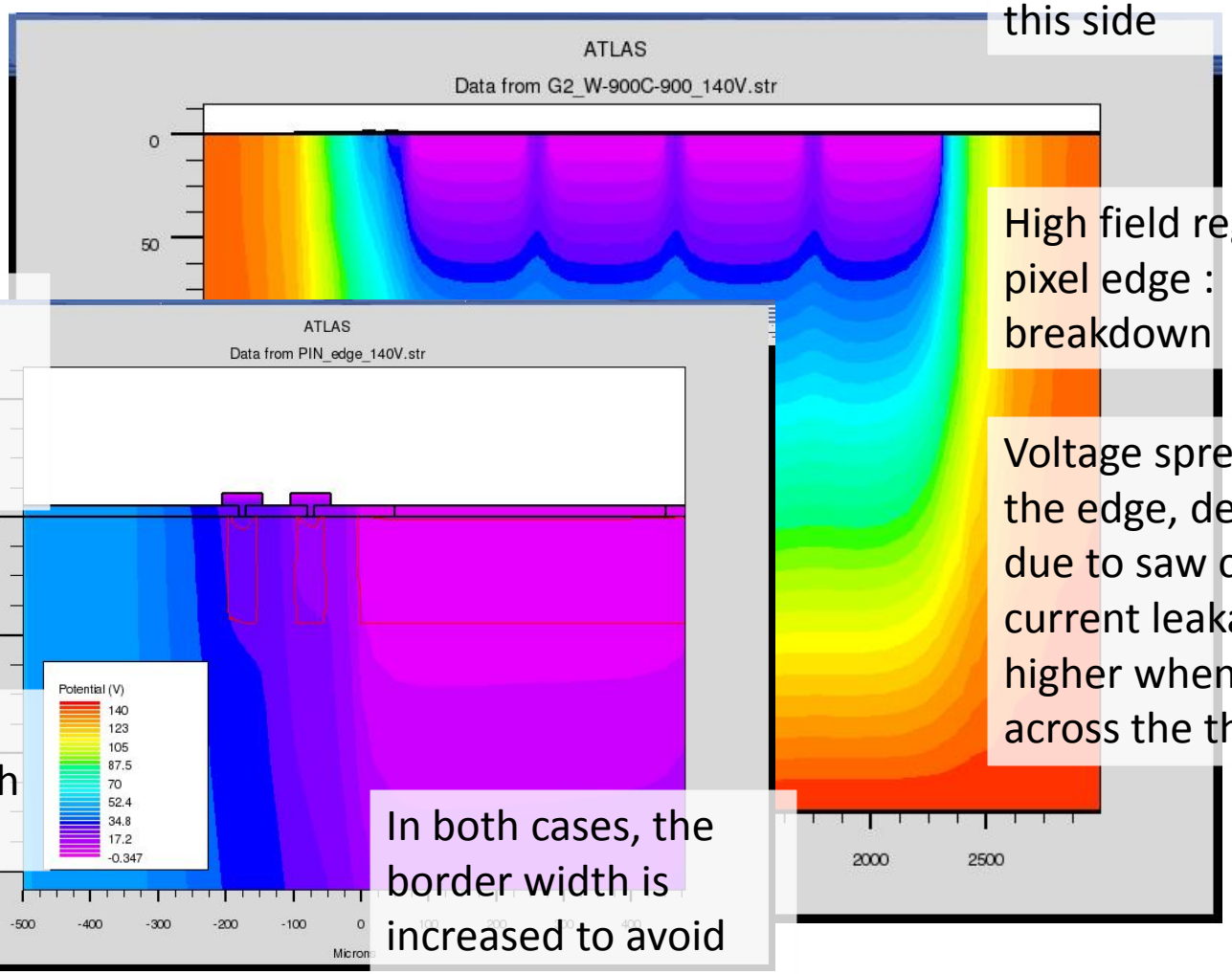




Guard rings : less E, high breakdown voltage

To guard or not to guard

No guard rings on this side



High field region at pixel edge : breakdown

Guard rings avoid high field
Lower risk of breakdown

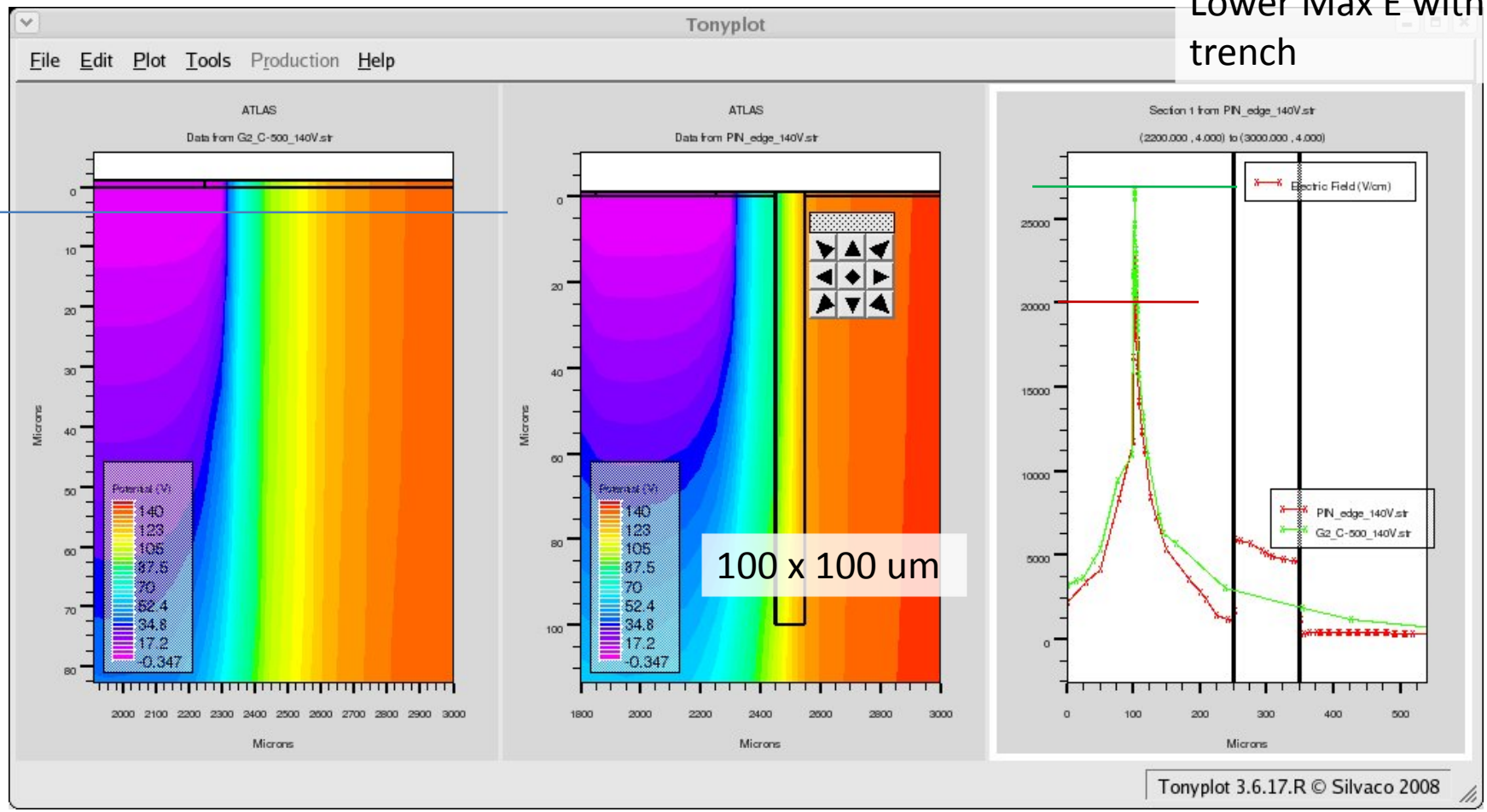
Voltage spread at the edge, defects due to saw cuts : current leakage, higher when V across the thickness

Actually, GR are biased but with high impedance

In both cases, the border width is increased to avoid current leakage

Trench principle

Lower Max E with a trench



OnSemi is equipped with a trenching machine

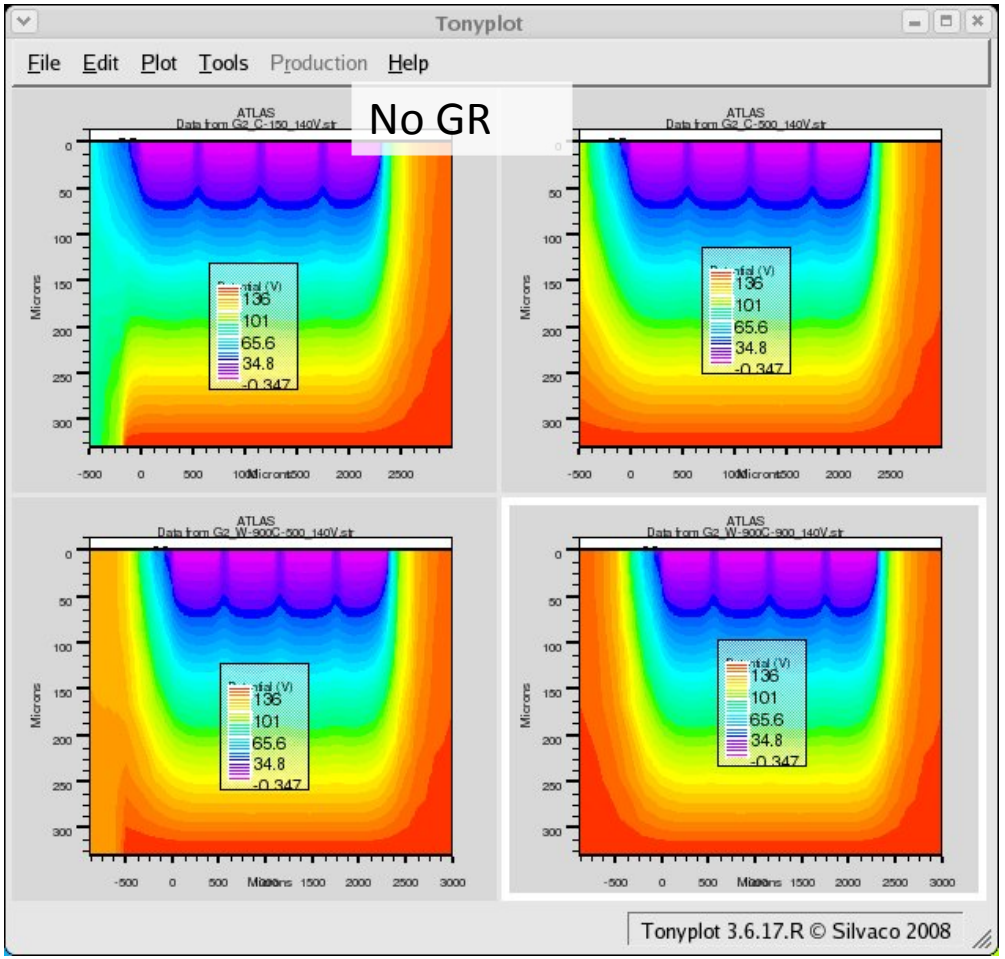
Double sided guard ring

Limited extend of the common Electrode

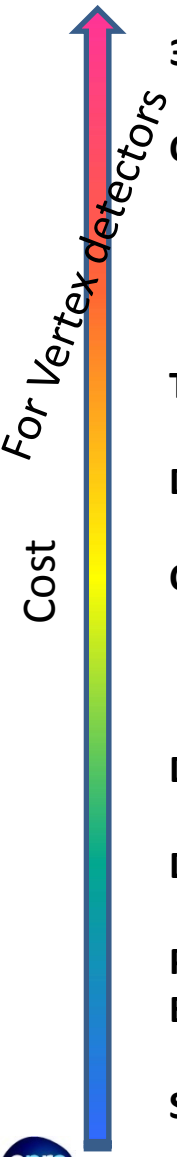
Full extend of the common Electrode

500 um

900 um



Some optimizations



3D sensors : lower Vbias, internal current flow, low sensibility to edge effects : can be ~edgeless (100 um)

Cut through edge

same technology as for 3D but used only at the edge
no saw cuts, 3D edges
4-side abuttable ~*no dead space,* Deep trench etch, n doped polysilicon fill provides edge doping

Integration ☹

Trenches + saw cut : cost of trenching, post processing of every sensors, bad control of current.

Dry etching cut

Current terminating ring

two rings but biased : thin contact needed, gluing not applicable
edge width less than ½ wafer thickness

Integration ☹

Double sided GR

Doped edges

Punch-through biasing

Biased GR

Integration ☹

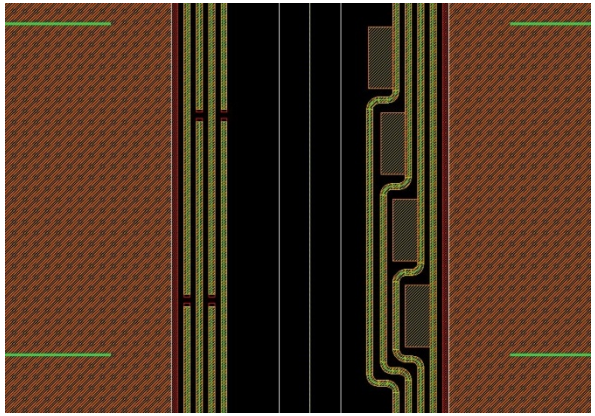
Crosstalk + ~edgeless ☺ (300 um)

Segmented GR : need further tests

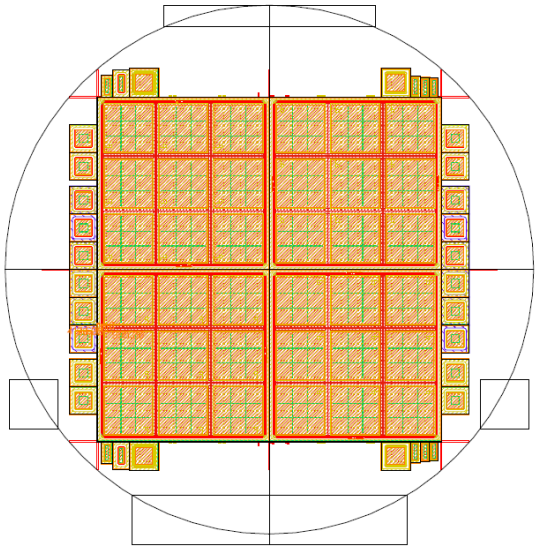
edge ☹ (800 um)

Segmented guard ring

- Should avoid the signal propagation along the border of the wafer

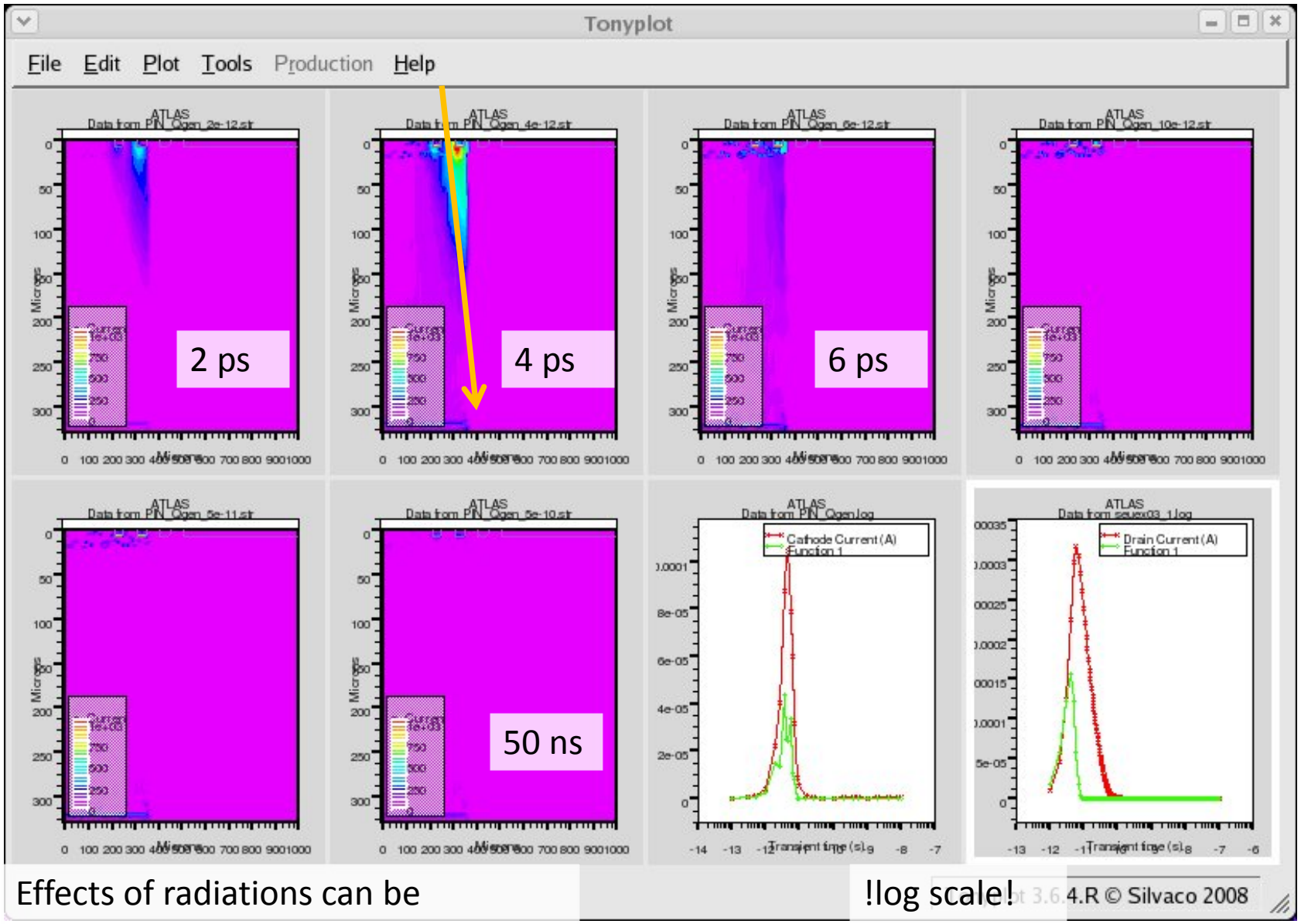


- Idea tested thanks to PCBs and test bench at LPC (CALOR'08, NSS'08 talks)
  - Segmented topology helps to prevent SqEvt (factor 50 on signal intensity)
  - What about current leakage & breakdown ?



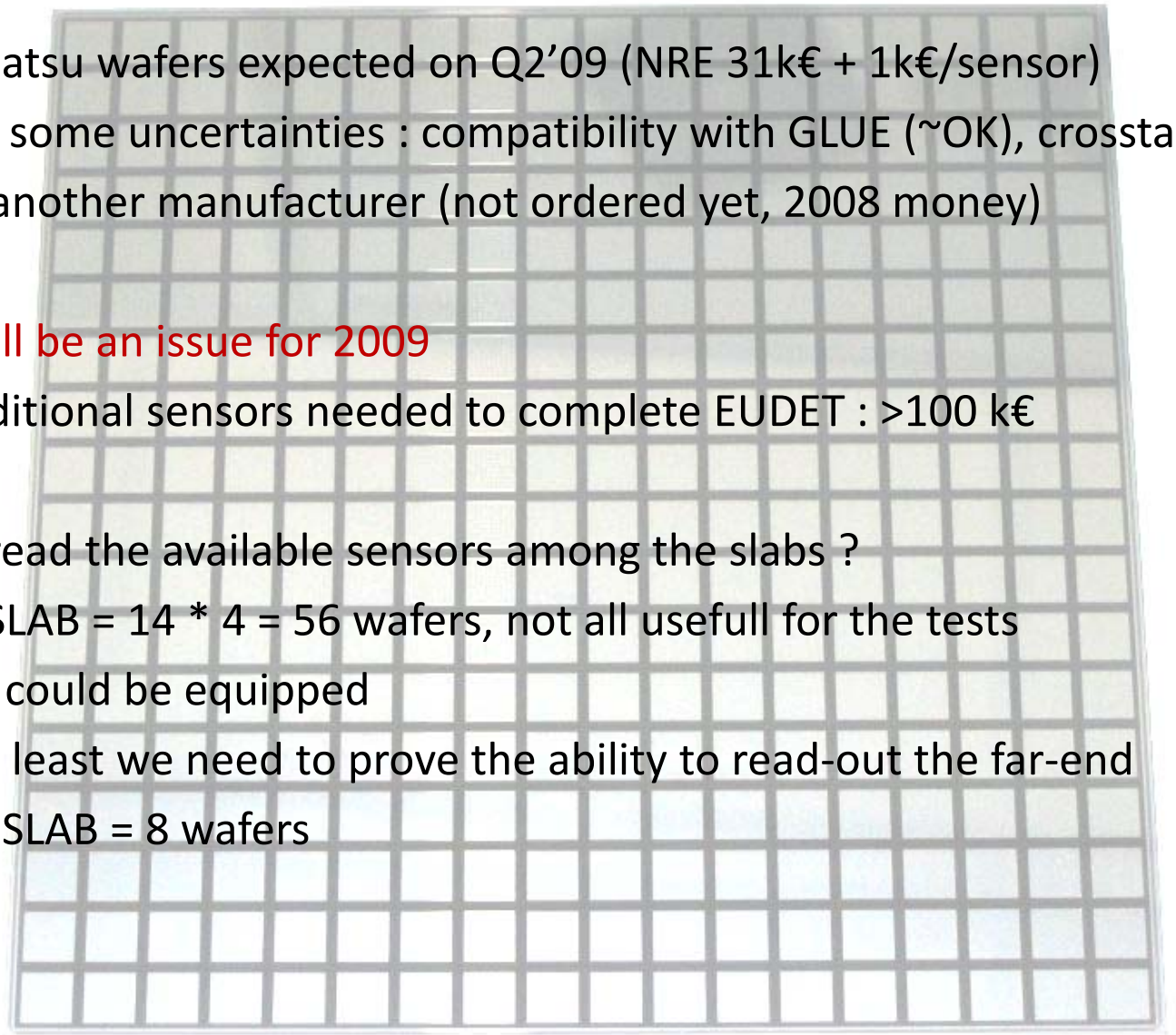
- Will be measured at LPC on January
- Prototype wafers are being manufactured (LLR made layout)
  - OnSemi/Institute of Physics (Prague), Cz
  - BhaBha Atomic Research Centre, India

More Silicon simulation



Effects of radiations can be simulated

ECAL Silicon wafers : Conclusion



40 Hamamatsu wafers expected on Q2'09 (NRE 31k€ + 1k€/sensor)

despite some uncertainties : compatibility with GLUE (~OK), crosstalk (~OK)

+ 20 from another manufacturer (not ordered yet, 2008 money)

Funding will be an issue for 2009

120 additional sensors needed to complete EUDET : >100 k€

How to spread the available sensors among the slabs ?

1 long SLAB = 14 * 4 = 56 wafers, not all usefull for the tests

½ could be equipped

at least we need to prove the ability to read-out the far-end

1 short SLAB = 8 wafers