SiW Ecal EUDET Module

From the TDR to the
Demonstrator
and beyond

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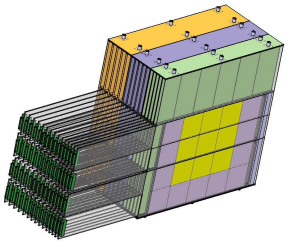
LAL Orsay

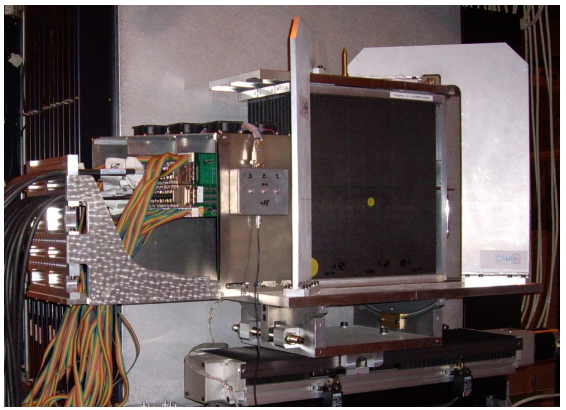
To learn more ....

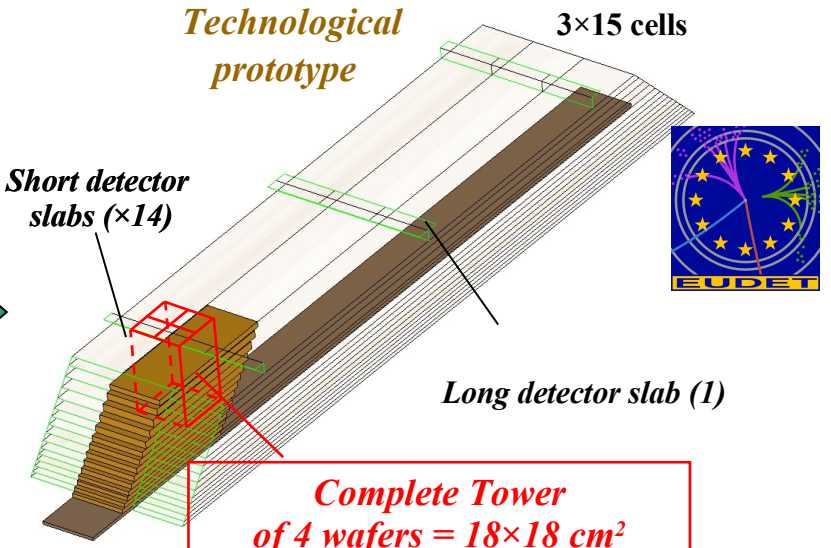
http://flc.web.lal.in2p3.fr/poeschl/siwecal.html

EUDET Prototype

- Logical continuation to the physical prototype study which validated the main concepts : alveolar structure , slabs, gluing of wafers, integration
- Techno. Proto : study and validation of most of technological solutions wich could be used for the final detector (moulding process, cooling system, wide size structures,…)
- Taking into account industrialization aspect of process
- First cost estimation of one module







• 3 structures : 24 X_0 (10×1,4mm + 10×2,8mm + 10×4,2mm)
• sizes : 380×380×200 mm3
• Thickness of slabs : 8.3 mm (W=1,4mm)
• VFE outside detector
• Number of channels : 9720 (10×10 mm²)
• Weight : ~ 200 Kg

• 1 structure : ~ 23 X_0 (20×2,1mm + 9×4,2mm)
• sizes : 1560×545×186 mm3
• Thickness of slabs : 6 mm (W=2,1mm)
• VFE inside detector
• Number of channels : 45360 (5×5 mm²)
• Weight : ~ 700 Kg

Tsukuba/

The groups working on the EUDET Electromagnetic Calorimeter

- What we call “EUDET Module” is in fact the next SiW Ecal CALICE Prototype

- Financial support by EU but largest fraction of funding still from “Calice” ressources!!!!

Time Scale of Project

~Today | Spring 2009 2009 | 1/7/09 | Summer/Autmun 2009 | 2010

← Studies on mechanical Integration and DAQ -> | Tests avec ASU1 | Tests avec ASU2

Design of Prototype concluded

Assembly and studies with Demonstrateur

'ASU 1': SPIROC2/SKIROC with FEV7

EUDET: Deadline, Alveolar Structures and ASU 1

ASU2: SPIROC2 with FEV8

EUDET-Memo-2008-07

ECAL Si/W – Design and Fabrication of moulds

for the EUDET Module

M.Anduze, R. Poeschl

July 01, 2008

Covering apects of the alveolar structures

TDR of SiW EUDET Module

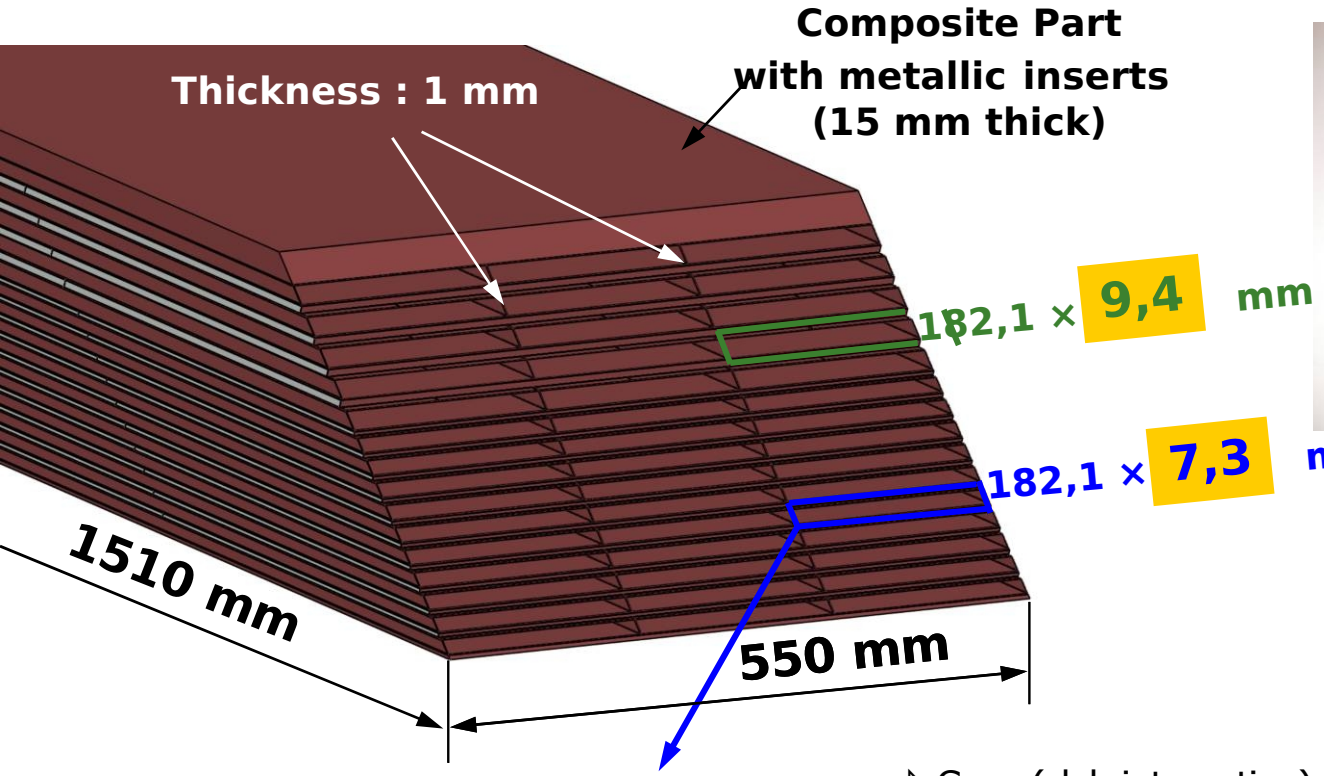
EUDET Memo 2008-11

JRA3 Electromagnetic Calorimeter Technical Design Report

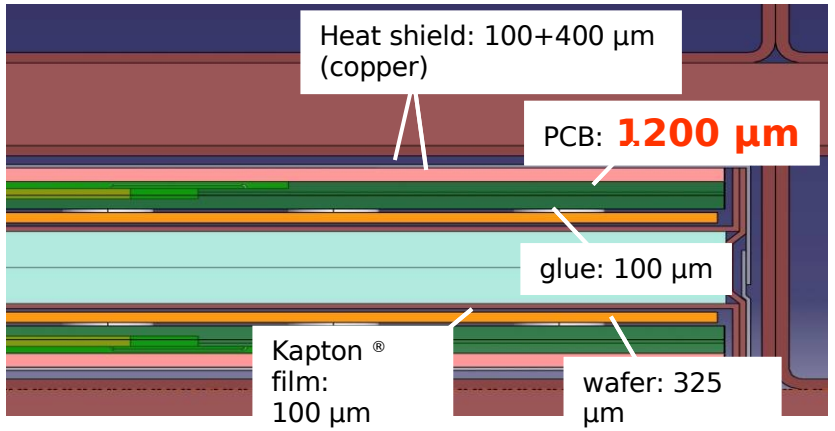
M. Anduze[1], D. Bailey[2], R. Cornat[1], P. Cornebise[3], A. Falou[3], J. Fleury[3], J. Giraud[5], M. Goodrick[4], D. Grondin[5], B. Hommels[4], R. Poeschl[3], R. Thompson[2]

Detailed Technical Design of EUDET Module

Module EUDET – Current Design (final)



Thickness :
FEV5-1 : 1.17mm (+-0.04)
FEV5-2 : 1.19mm (+-0.04)
FEV5-3 : 1.20mm (+-0.02)



- ⇨ Gaps (slab integration) : 500 µm
- ⇨ Heat Shield: **400 µm ?** Validation with the demonstrateur
- ⇨ PCB : ~~800 µm~~ **~1200 µm**
- ⇨ Thickness of Glue : 100 µm
- ⇨ Thickness of SiWafer : 325 µm
- ⇨ Kapton® film HV : **100 µm ?**
- ⇨ Thickness of W : 2100/4200 µm (± 80 µm)

Parties Involved

6 Laboratories are sharing out tasks in according to preferences and localization:

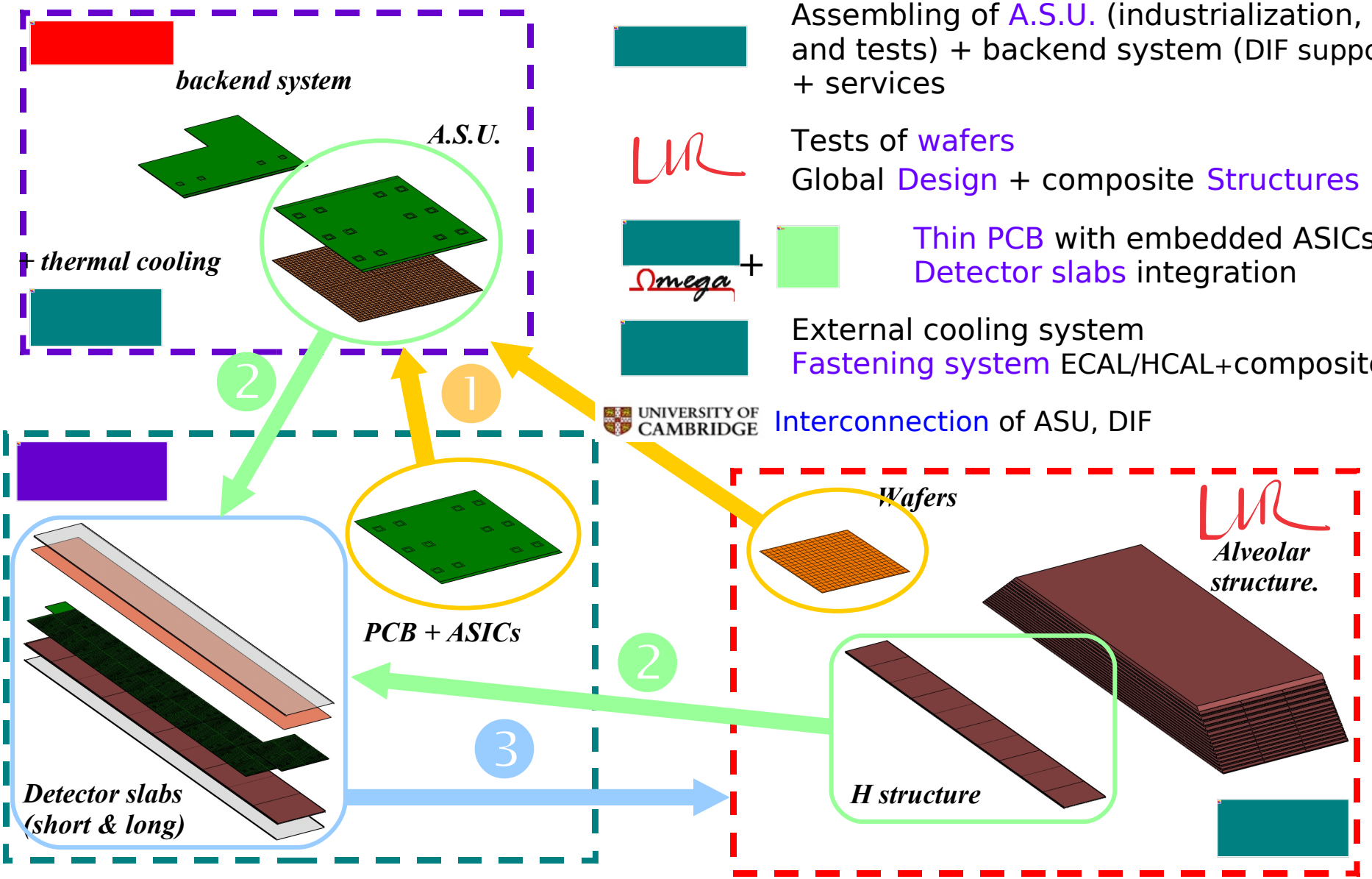
Assembling of A.S.U. (industrialization, gluing and tests) + backend system (DIF support) + services

Tests of wafers
Global Design + composite Structures

Thin PCB with embedded ASICs
Detector slabs integration

External cooling system
Fastening system ECAL/HCAL+composite plates

UNIVERSITY OF CAMBRIDGE Interconnection of ASU, DIF



Sensors layout

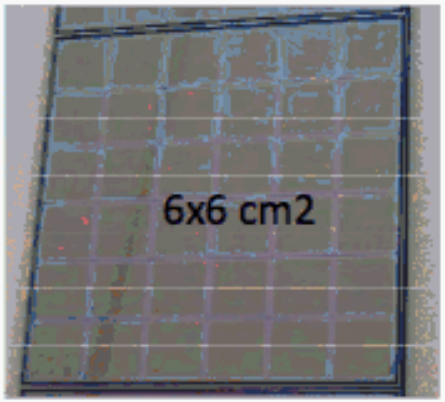
Find a **low cost** but effective sensor

Why ? **ILC would need 3000 m2 of them**

How ? **Smallest number of manufacturing steps**
- PIN diodes
- Guard-rings made with the same steps :

floating guard-rings

- Easy to integrate : gluing
- Low leakage current (<4 nA/cm2)
- Stable in time and for gluing
- I(Vbias) : leakage
- C(Vbias) : depletion and dC/dV noise



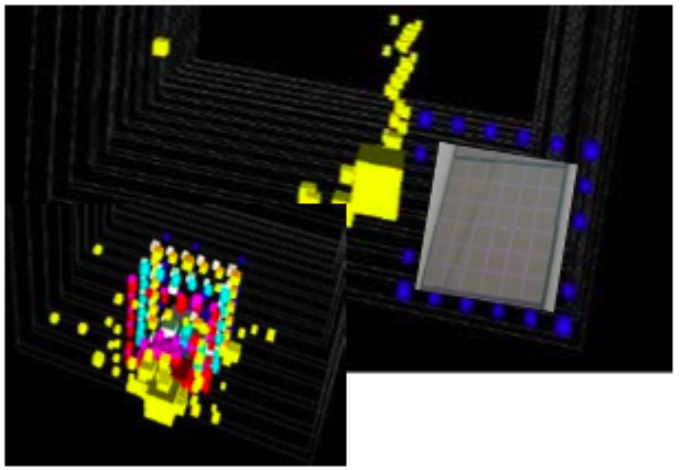
Last prototype :

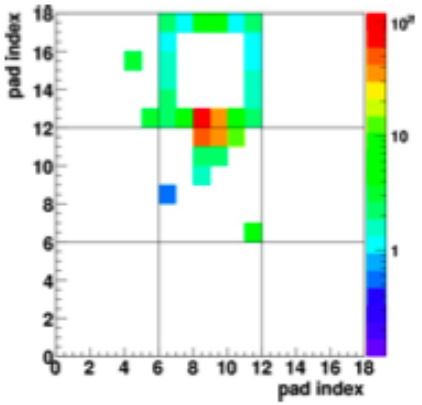
- 3 production batches (2005-2007)
  - Russia (Moscow State University)
  - Czech Republic (Institute of Physics)
  - Korea
- 6x6 pads, 525 um thick, 200V bias
- MIP = 42000 electrons

Cross talk observed during prototype testbeam

Sensors : unexpected behavior

When a particle hit the floating guard-rings...





The square shape corresponds to the guard-rings location

Unbiased guard-rings act as a pad all around the sensor

Definitely confusing for clustering and reconstruction

Guard-rings are mandatory to avoid breakdown = need to find a turnaround which meet the cost requirements

- That's (also) what test beams are good for!!!!!
- Don't think that you're perfetct - Detect the unexpected!!!

Segmented guard rings prototypes preliminary measurements results

- The segmentation of guard rings clearly contributes to the lowering of crosstalk along the edge of the wafers

Continuous		
720		
430	220	
700	460	

1 cm segments		
528	32	
50	32	31

3 mm segments		
170	17	
29	14	13

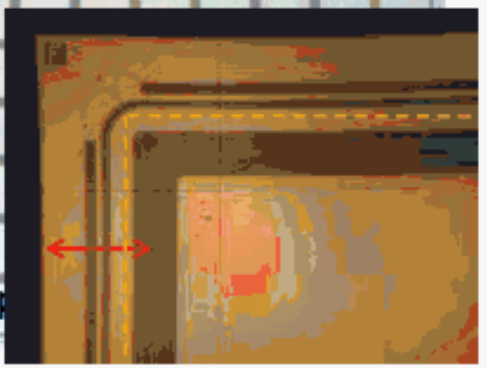
- I(V) characteristics are not standard
- Breakdown occurs early, in a 100-300 V range (non segmented: >500 V)
- BUT: no optimizations were done on the layout
  - Further investigations are needed
  - Close contacts with Onsemi: agreement to share the costs

- Measurement backed up by theroretical calculations (NSS Proceedings by R. Cornat)
- Pixel cross talk seems to be understood – Conclusive remedies are under study

Hamamatsu wafers

- 9x9 cm2, 256 pixels ordered, 40 should be delivered on April
- Cost ! (eur/yen parity)
- 300 um (may be) gained on the edges
  - 800 um dead space (1.1 mm in previous version)

- Excellent breakdown >800 V
- Low leakage <4 nA/pixel
  - DC coupling to the chips
  - 1 nA = 1% dynamic range
- Good dC/dV at Vbias, <2pF/V (full wafer)
  - Mandatory for noise (CdV + **VdC**)
  - C= 10E-12, dV=10 mV, V=150V, dC = 20 fF => ~400 MIPs...



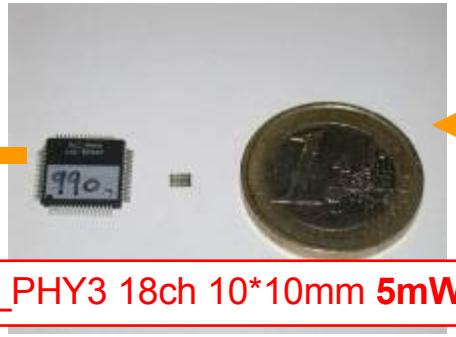
CALICE : week at Deagu, Febuary 19

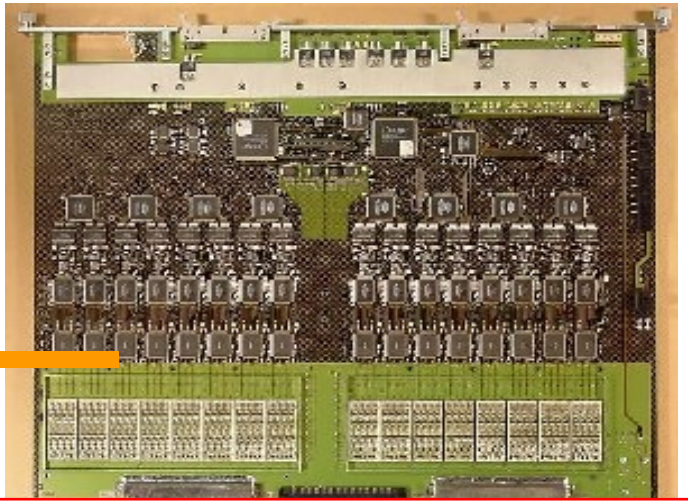
- Wafer Type at hand which meets requirements
- However, vey expensive!!!
- Broaden basis of manufacturers (FZU (Cz), OnSemi (CZ), MSU (Russia), Korea)

SKIROC Chip

- Designed to read out 64 Channels => 4 Chips per Wafer

- Ultra low power and as small as possible



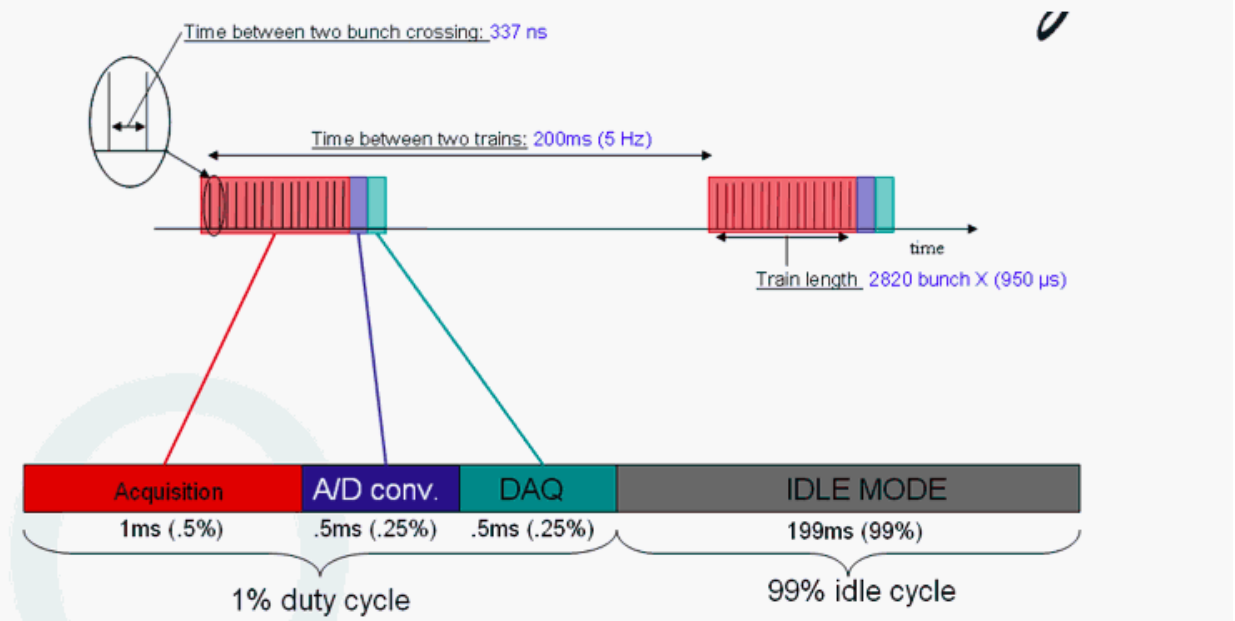


ILC : **25µW/ch**

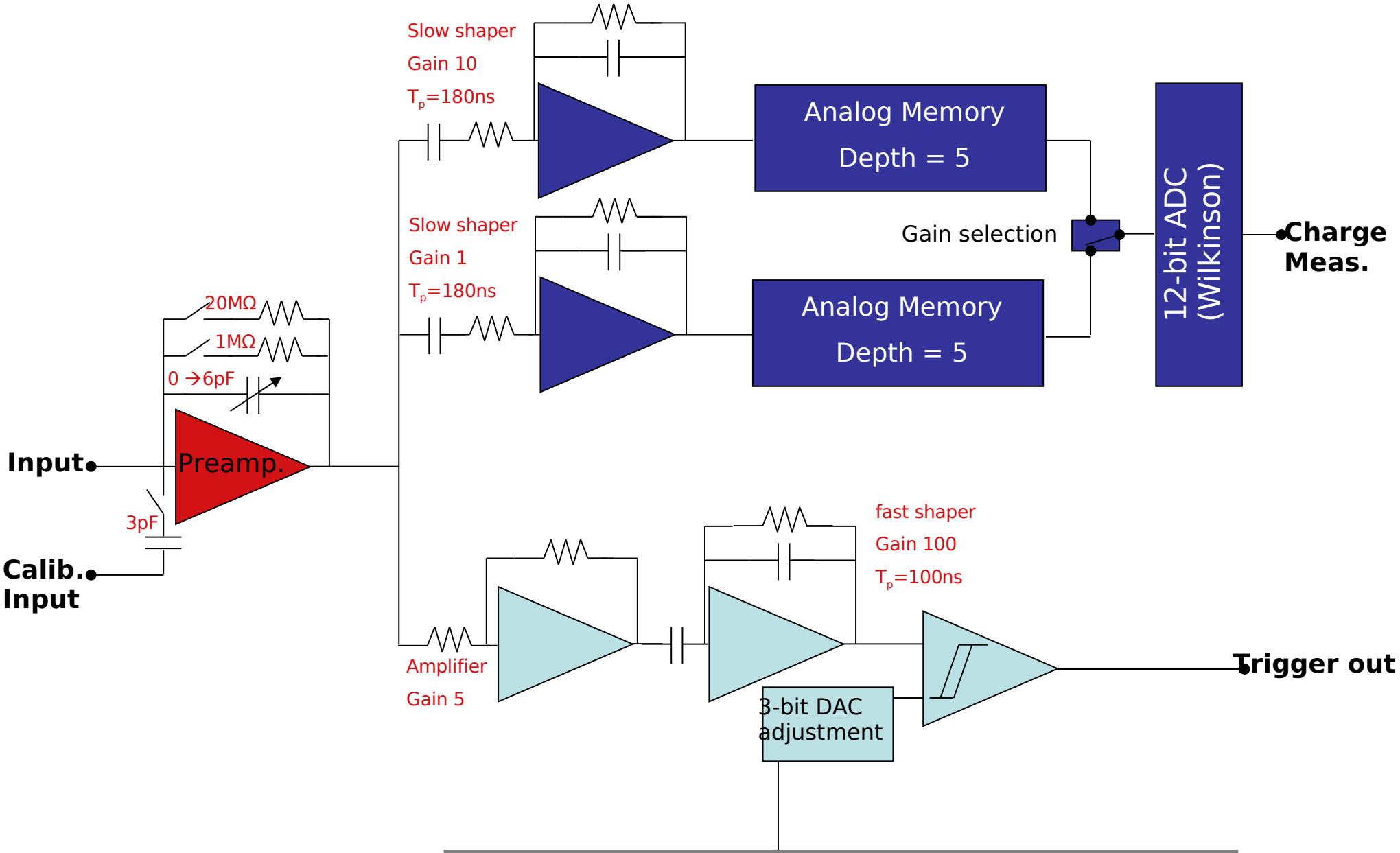
FLC_PHY3 18ch 10*10mm **5mW/ch**

ATLAS LAr FEB 128ch 400*500mm **1 W/ch**

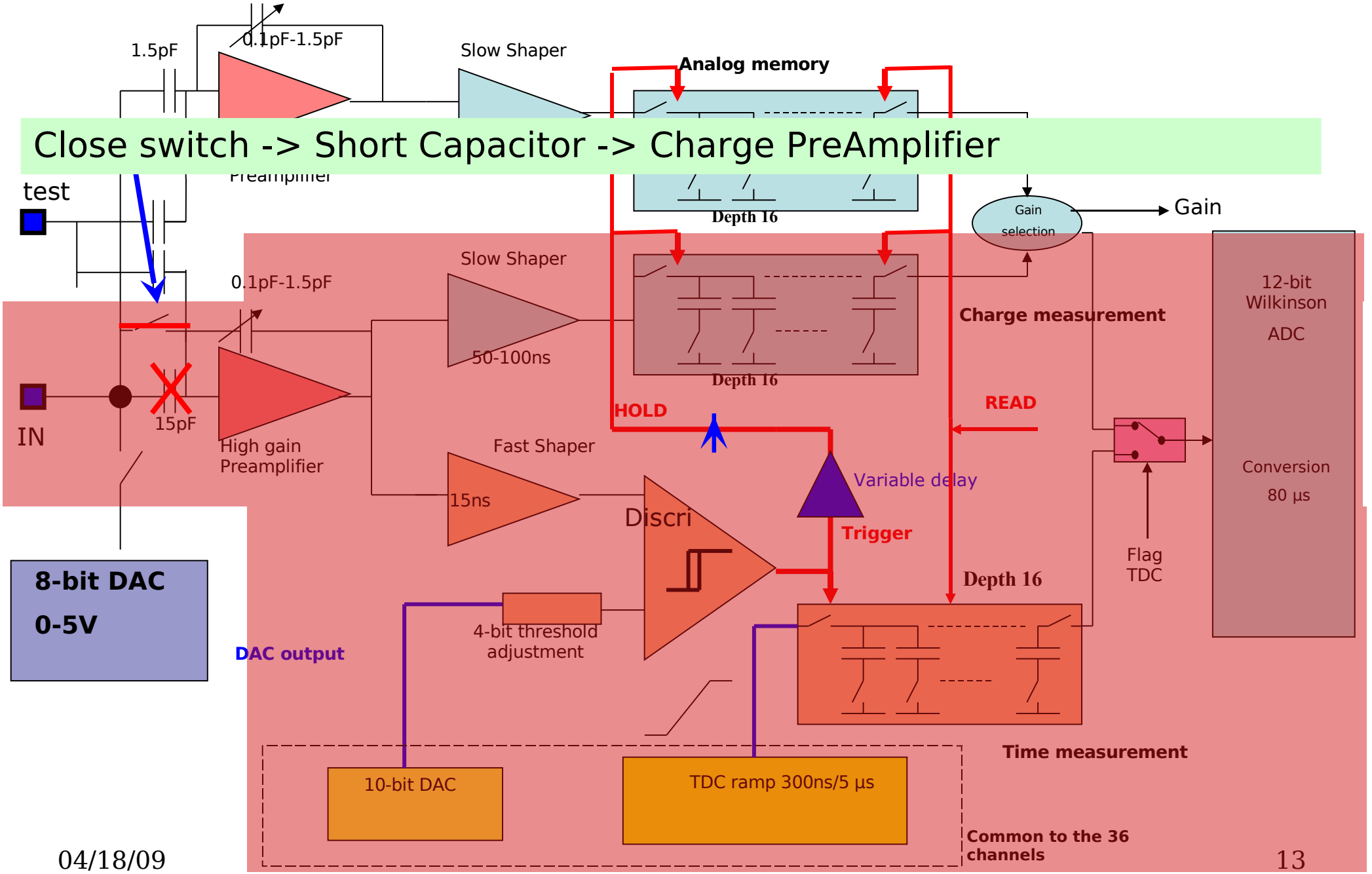
Main “tool” Power Pulsing:



SKIROC1 One channel block scheme



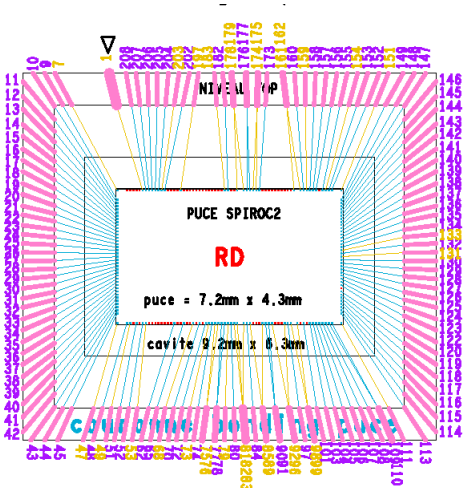
SPIROC used in SKIROC mode



Printed Circuit Board – Interface between Si Wafers and Chips

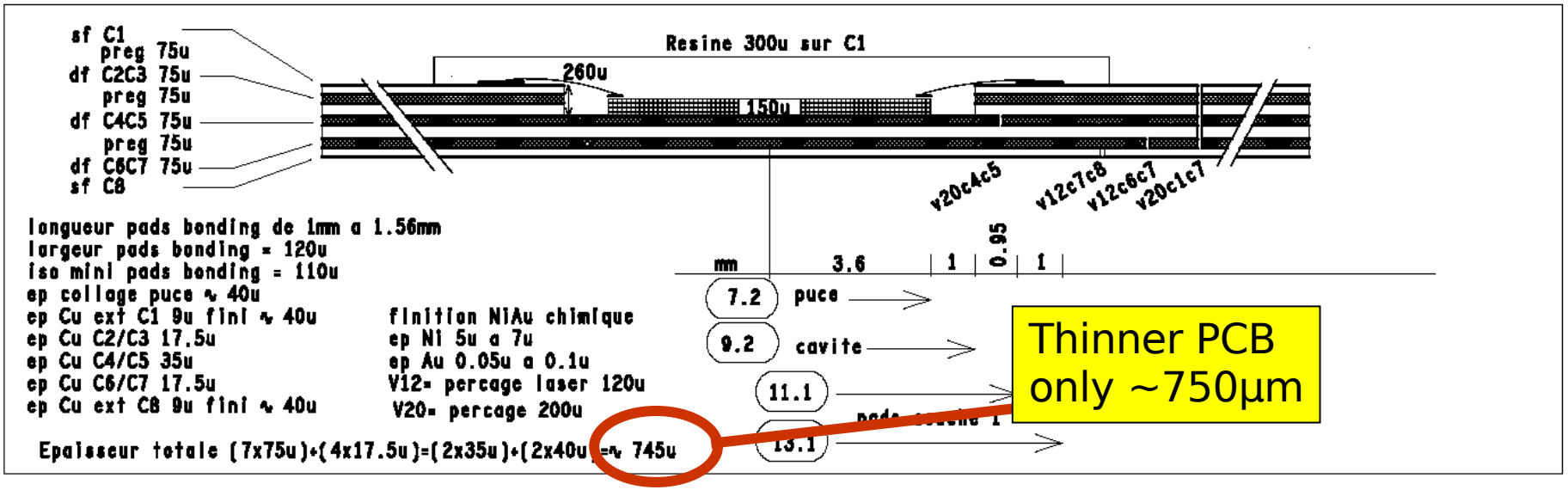
Pile-up

TOP	GND + Input chip signal
C2	horizontal routing
C3	AVDD + DVDD
C4	GND + vertical routing
C5	GND (pads signal shielding)
C6	GND + pads routing
C7	GND (pads shielding)
BOT	PADS



FEV 7

4 drilling sequences :
- Laser C7-C8 120µ filled
- Laser C6-C7 120µ
- Mechanical C2-C7
- Mechanical C4-C5



Very Challenging project – Design under revision

In contact with CERN and Industrial Partners (seems to be beyond industrial standards)

A generic DAQ System

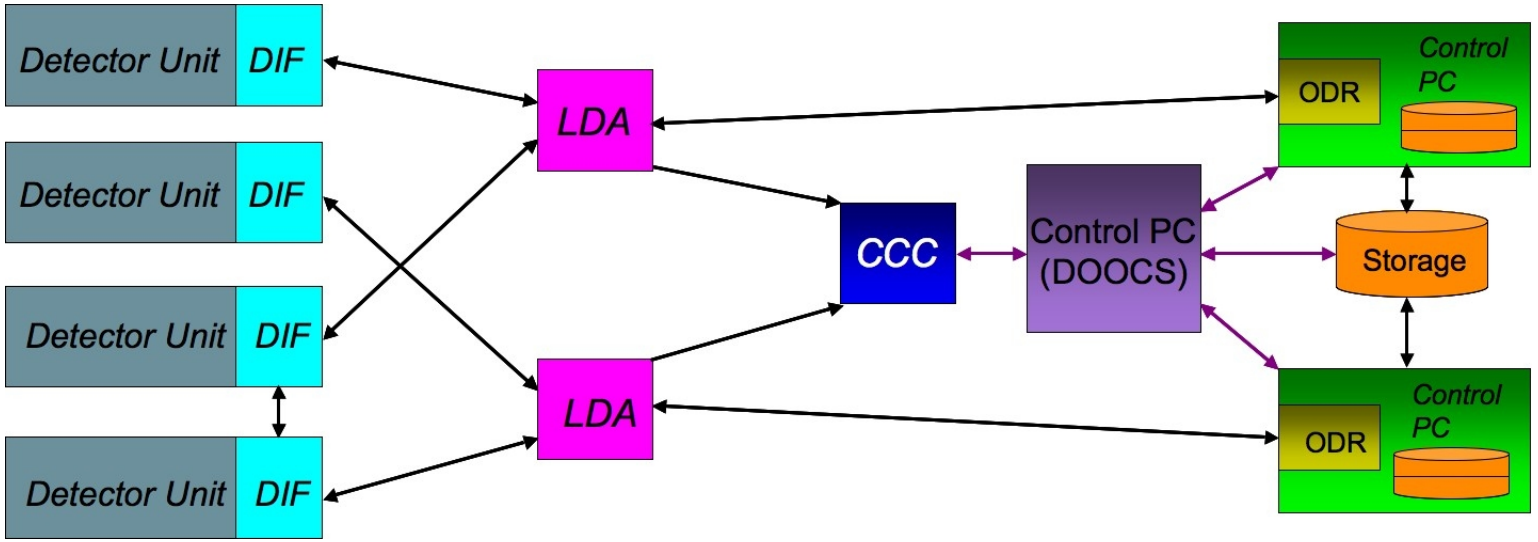
Standard

HDMI connectors
LVDS
GB Ethernet
Optical links

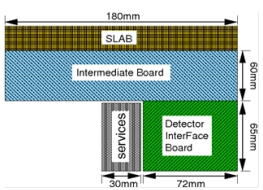
Generic

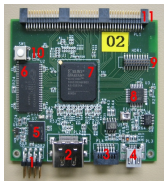
FPGA

Scalable



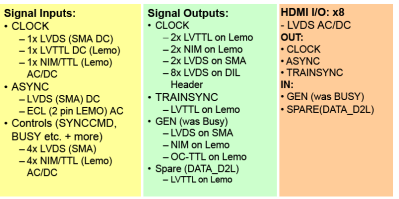
Detector Extremity – Detector Interface Card





Linked Data Aggregator

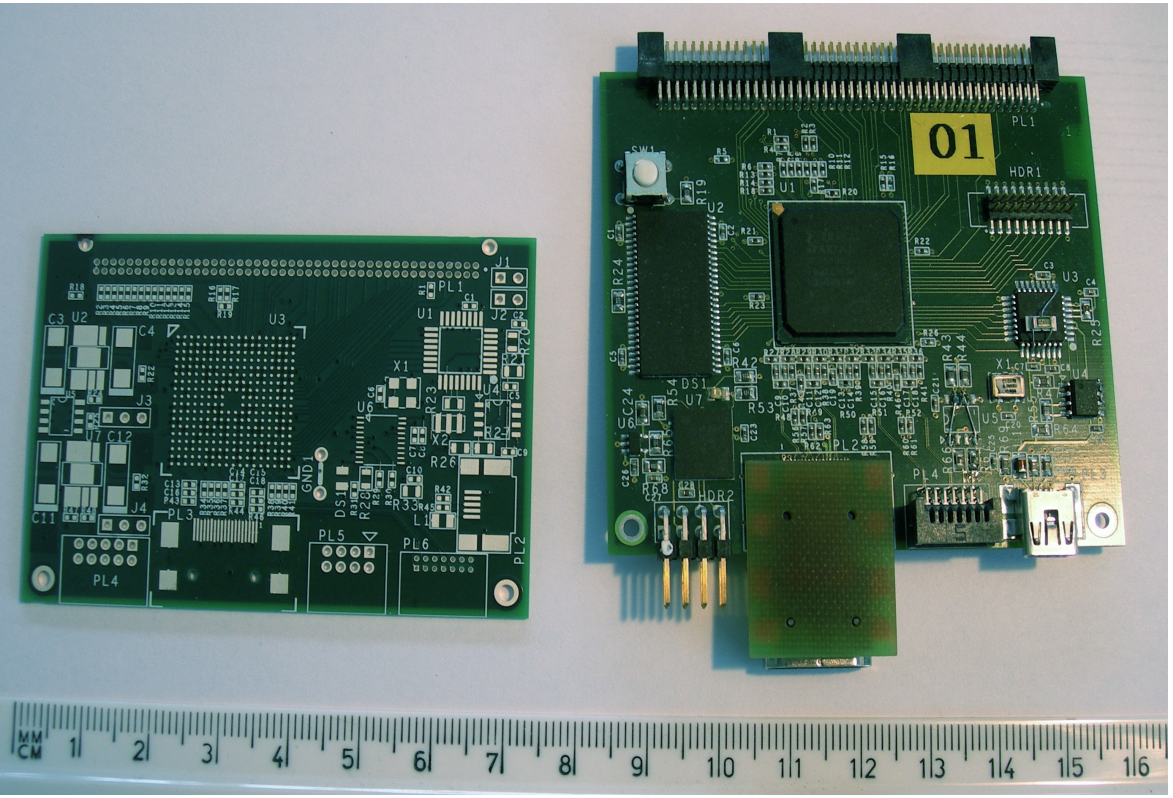
Clock, Commands and Control



Off Detector Receiver

ECAL DIF - 2nd revision coming up

Status: 8 DIF prototypes now produced and commissioned



ECAL DIF: small form factor. No room for extra features!

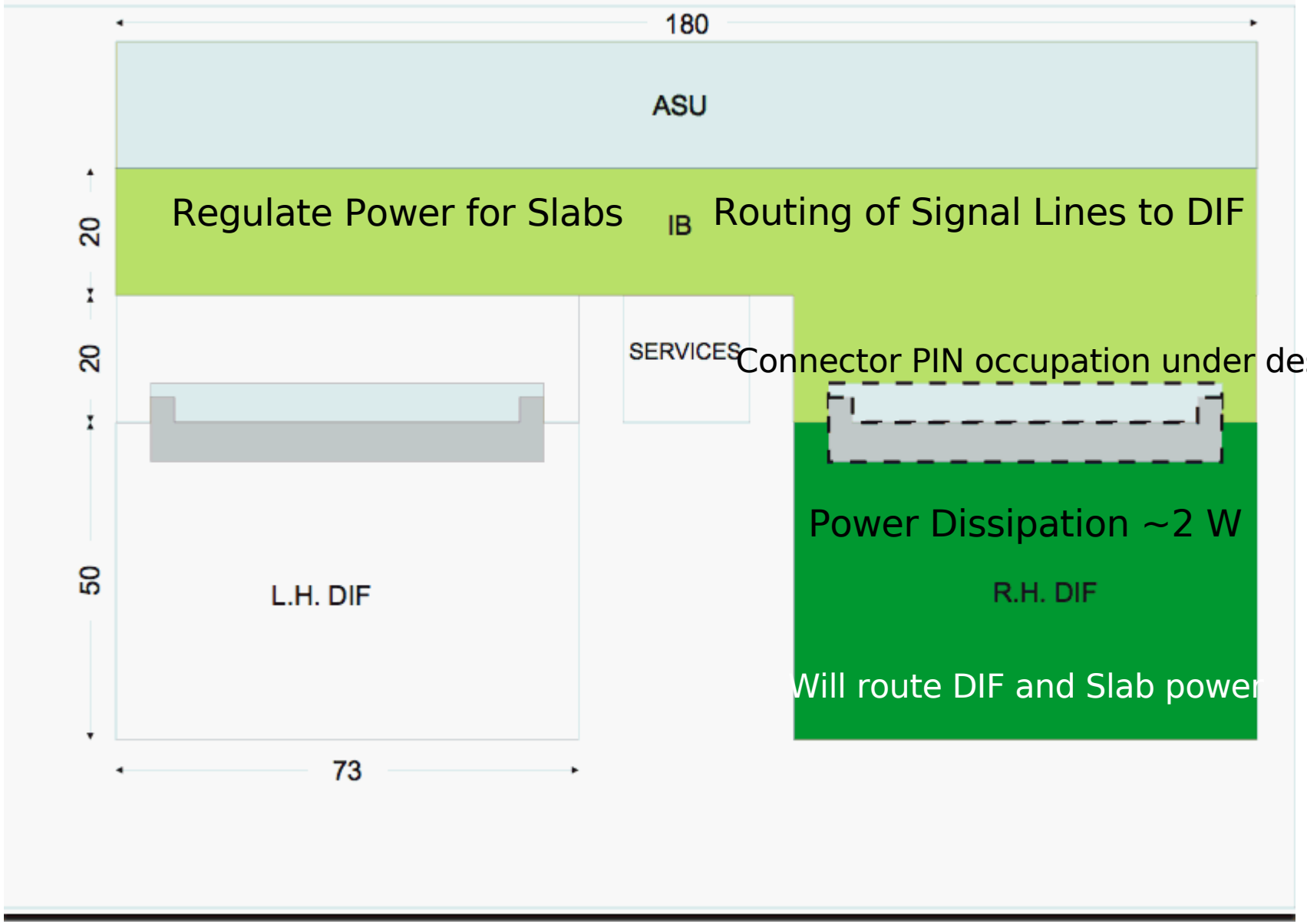
- Xilinx Spartan3 based
- USB, HDMI connections

DIF re-spin for EUDET in credit-card size form factor. Main changes:

- No external SRAM, user connector, reset button
- SPI-flash PROM, Flash RAM for VFE config

Hardware status:
PCB designed & produced, some components still being ordered, board population, testing to be done

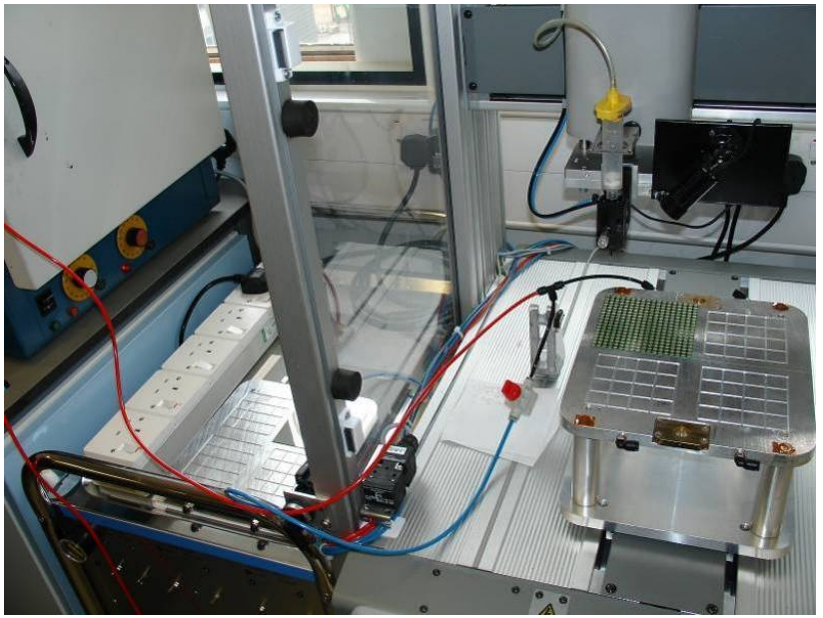
Agreed Dimensions DIF/IB Region



Gluing of ASUS

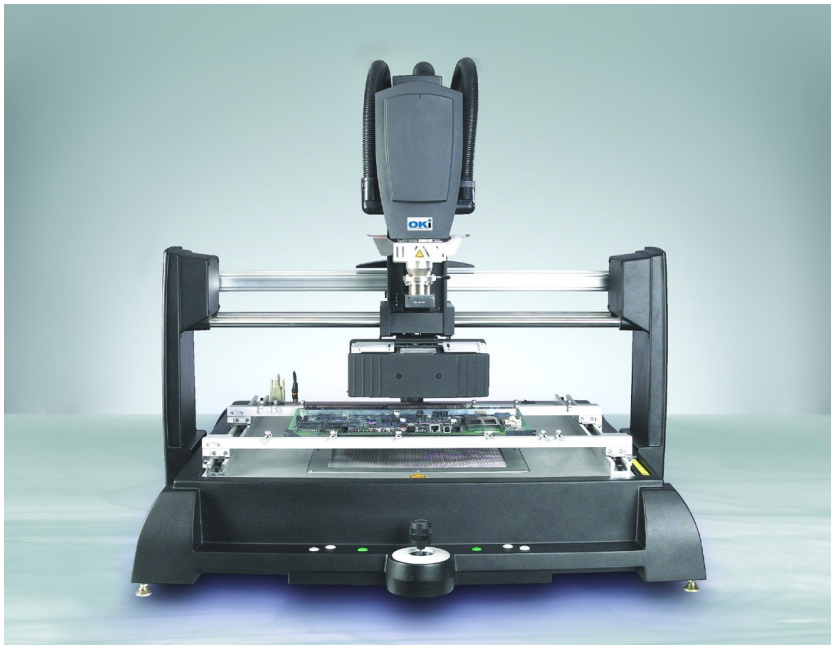
- Controlled glue dot deposition on the PCB
- The (four) Si Wafers are picked up, aligned and placed on the PCB
- Accurate thickness and planarity control via vacuum jigs
- The assembled ASU is allowed to cure

Test board with Dispenser Robot



"Gluing" rate 0.4 Hz

BGA Workstation for Wafer Placement

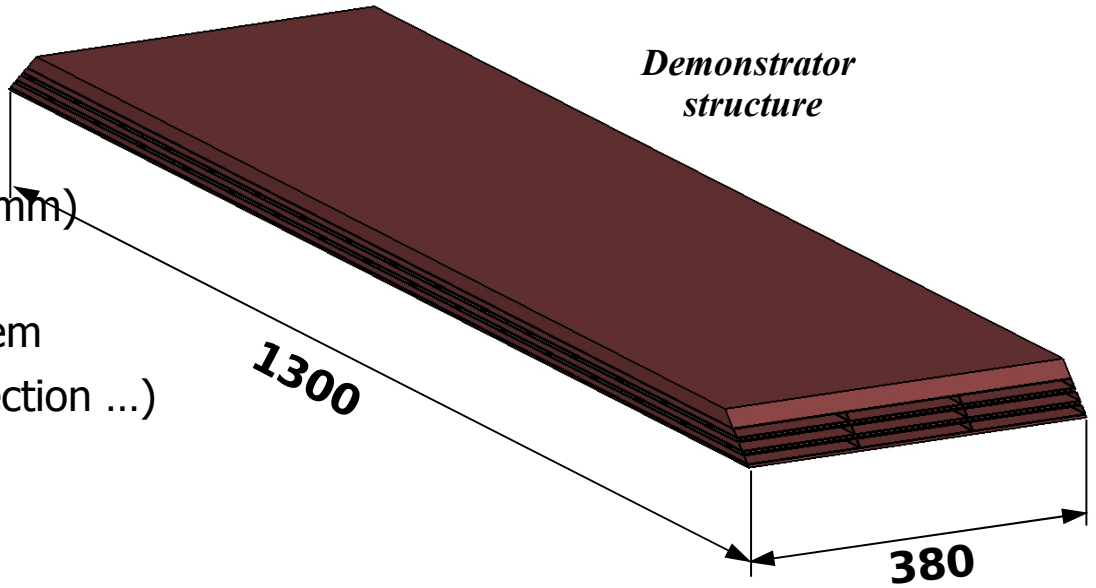


Precise Wafer Placement
by Split Field Optics

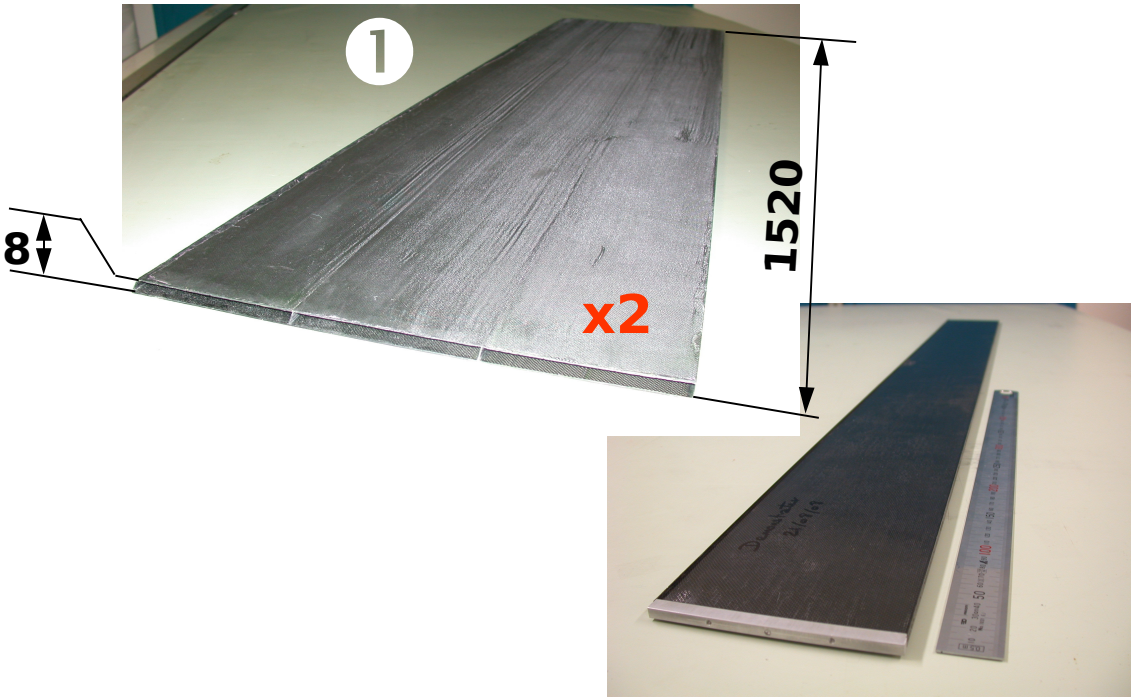
ASUs for four thermal layers glued at Uni Manchester

Demonstrator design

- **We have constructed a demonstrator**
  validate the assembly process
  before the actual EUDET Module
- Width the same as for physics prototype (124 mm)
- Thermal Studies:
  Equiped with thermal PCBs and a cooling system
- First test of slab integration (gluing, interconnection …)

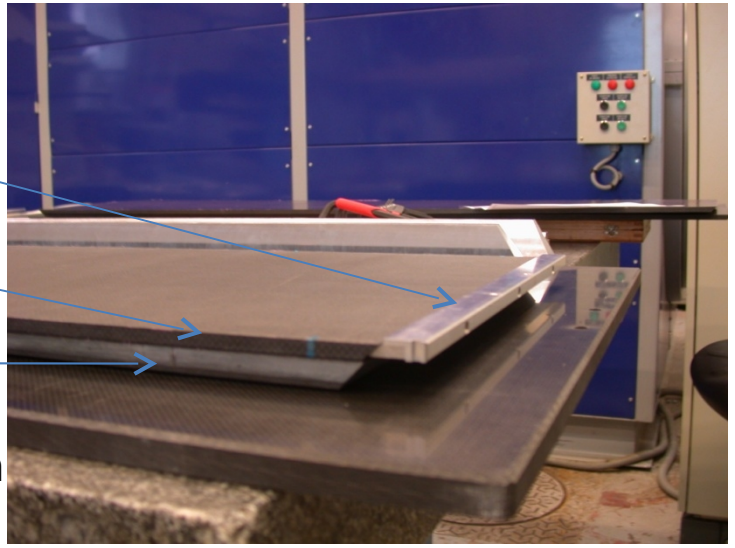


first test of alveolar layer



- **3 alveolar layers + 2 W layers**
- **3 columns of cells : representative cells in the middle of the structure**
- **Thermal studies support**
- **Width of cells : 126 mm**
- **Identical global length : 1.3m and shape (trapezoidal)**
- **Fastening system ECAL/HCAL**

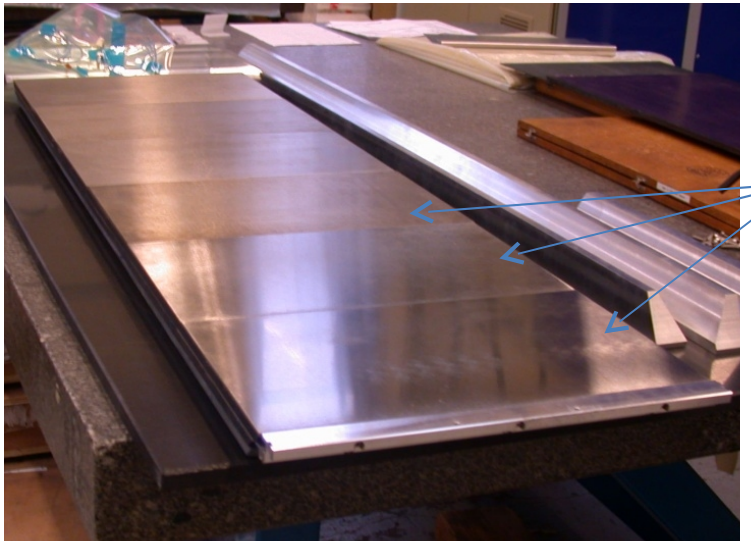
Full Assembly



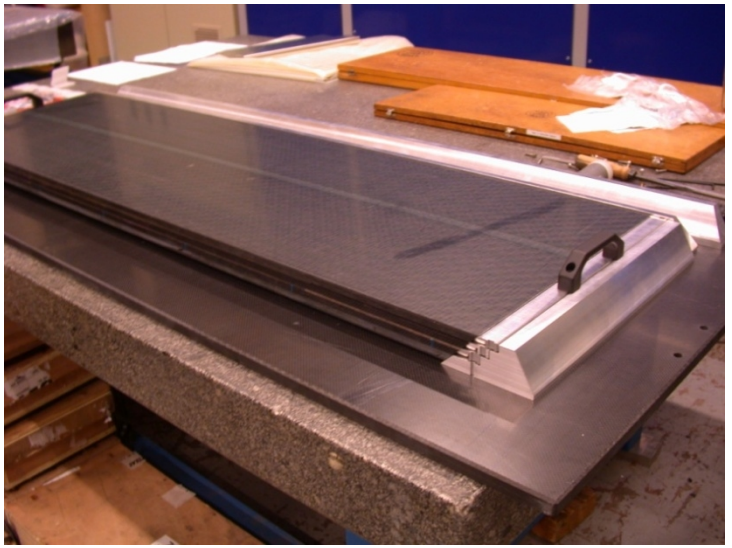
Adjusted cores

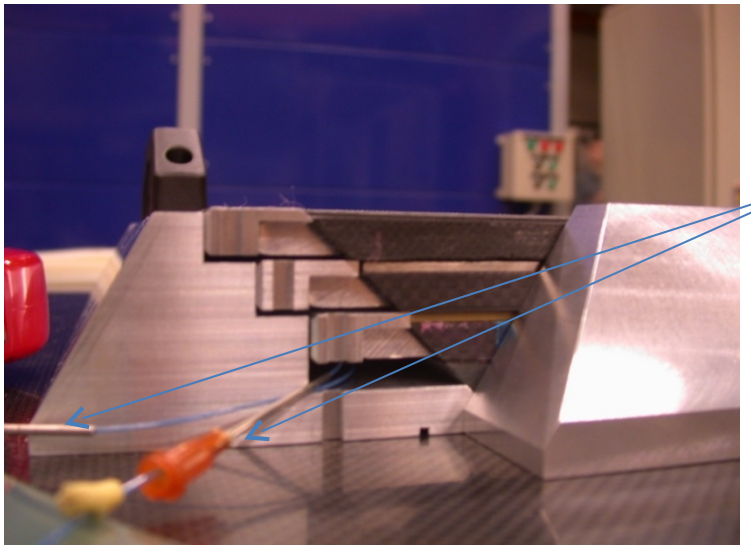
Carbon Cell

Big Carbon plate



Tungsten plate



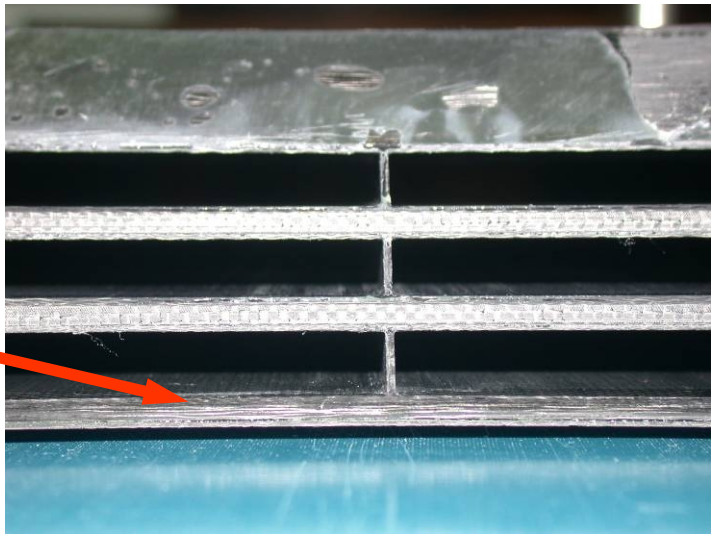


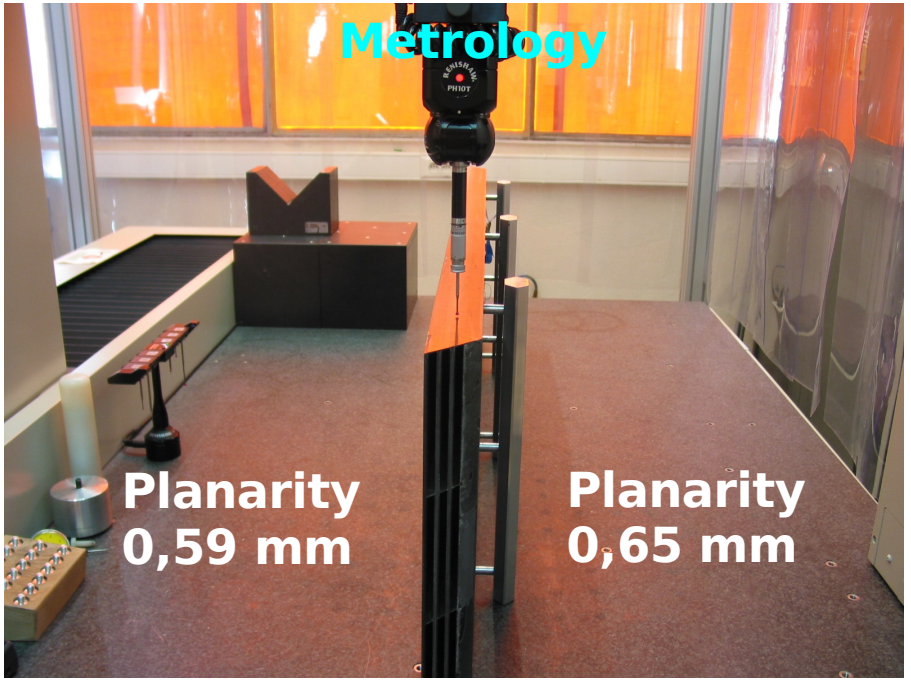
Optical Fiber to monitor stress

...including Aluminum Cores and Assembly Mould

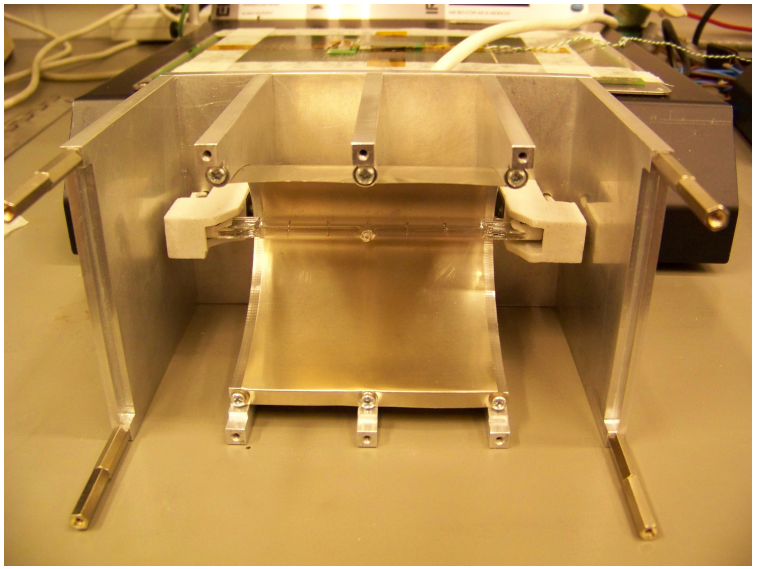
-> Ready for Curing

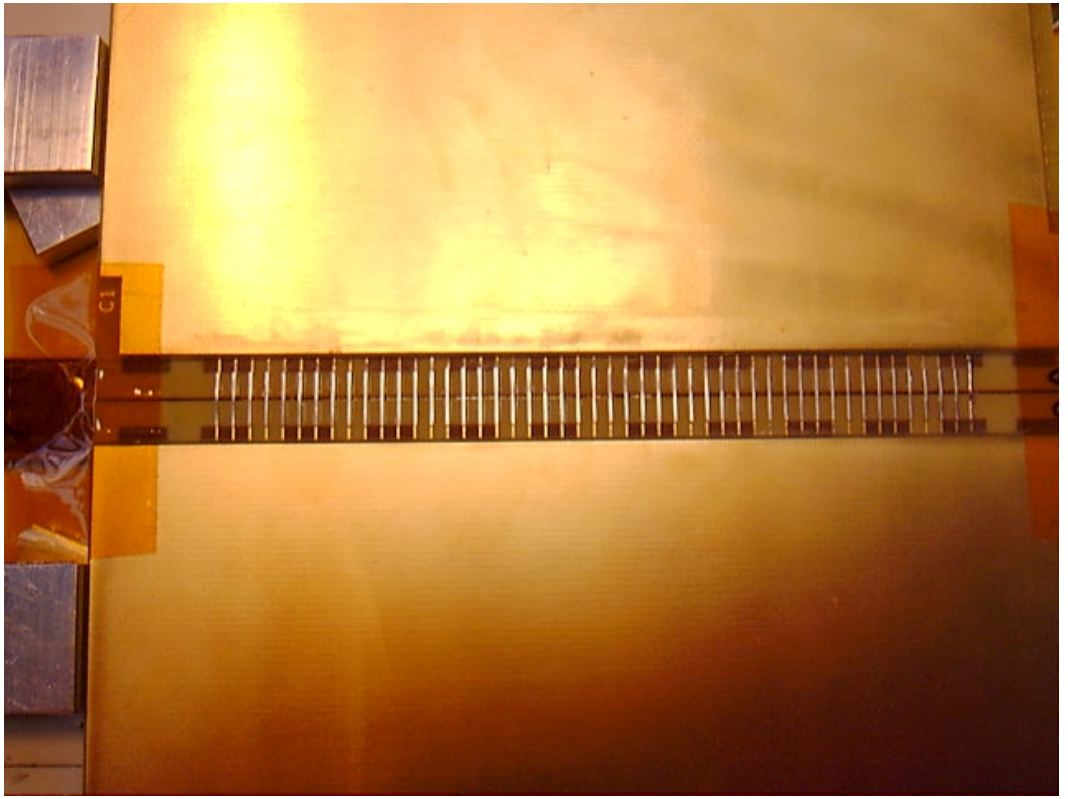
Alveolar Structures with (~) ILC Dimensions – **Yes, we can!!!!**

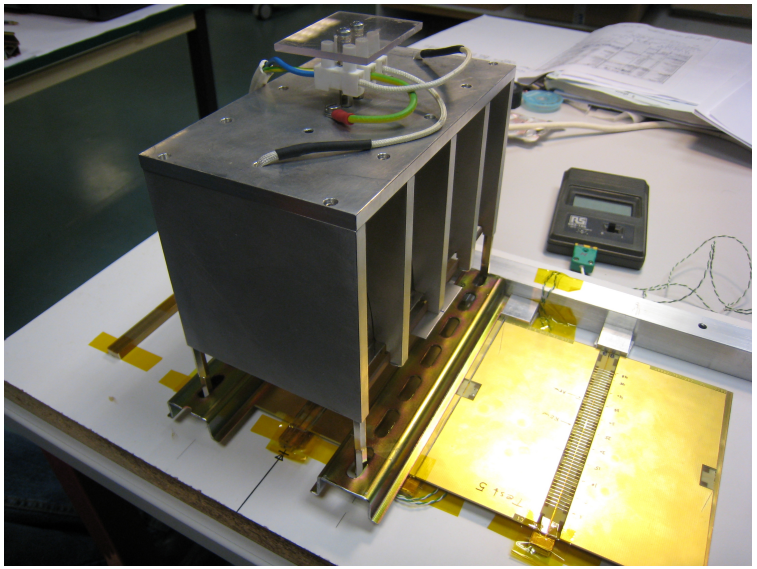




The joint between two boards





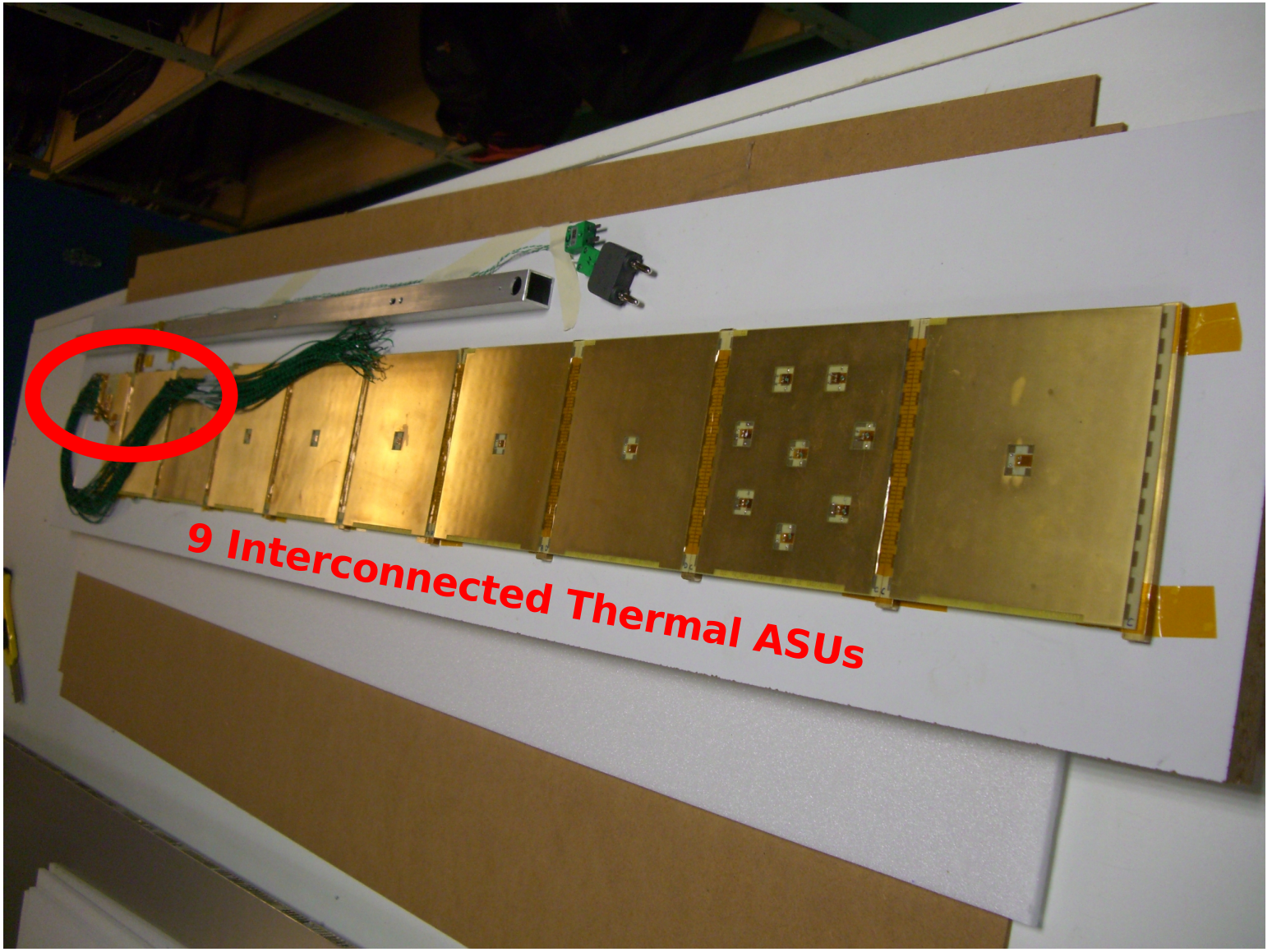


- Joint by halogen lamp heating up tin-bismuth soldering paste
  (Method developed by U. Cambridge)

- Heating Temperature ~200° C

Delicate Process for Demonstrator – Easier for EUDET Module

Thermal Layer assembled and ready for Thermal Tests

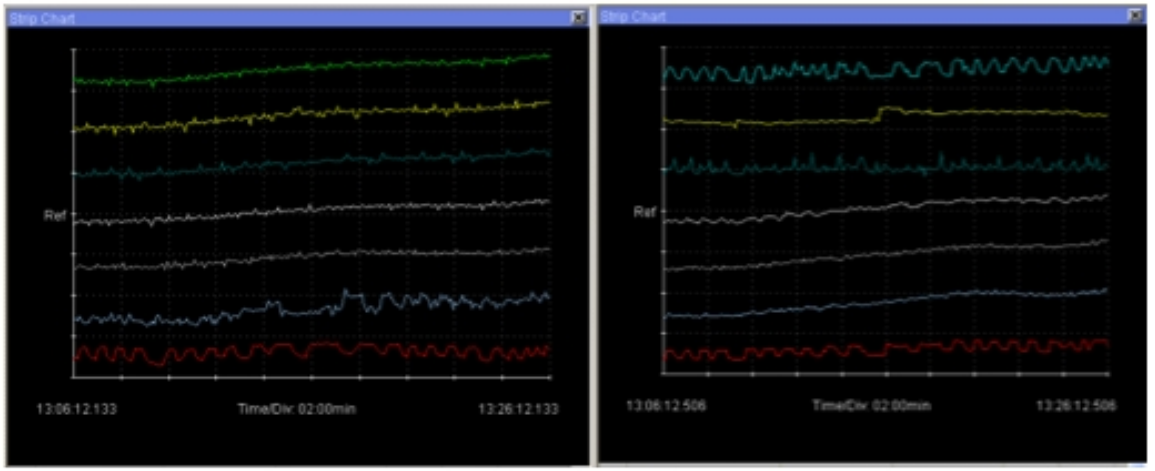


- w/o Photo: Copper Shielding and CuCe Electrical Protection manufactured at CERN in Collaboration with CALICE

First Results from Thermal Tests/ demonstrator

Cooling System: Test Program on going

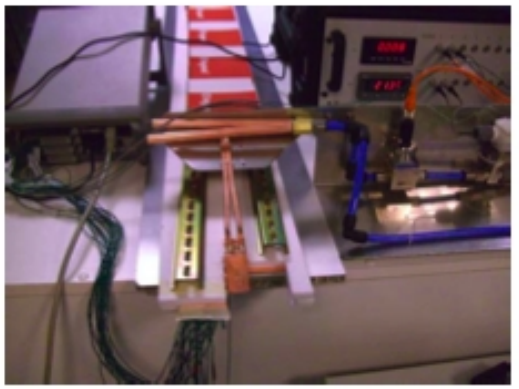
YES: ALL IS LINEAR and ΔT < 10 °C !



Evolution and correct stabilization of each thermal sensor in response to hot points implementation:

Chips:	**0 to 1 W**
Int.board:	**0 to 1 W**
DIF:	**0 to 2 W**

Extreme test: from Steady state up to cooling failure => temperature curve increasing to determine the maximal acceptable time without cooling (info for Elec…)

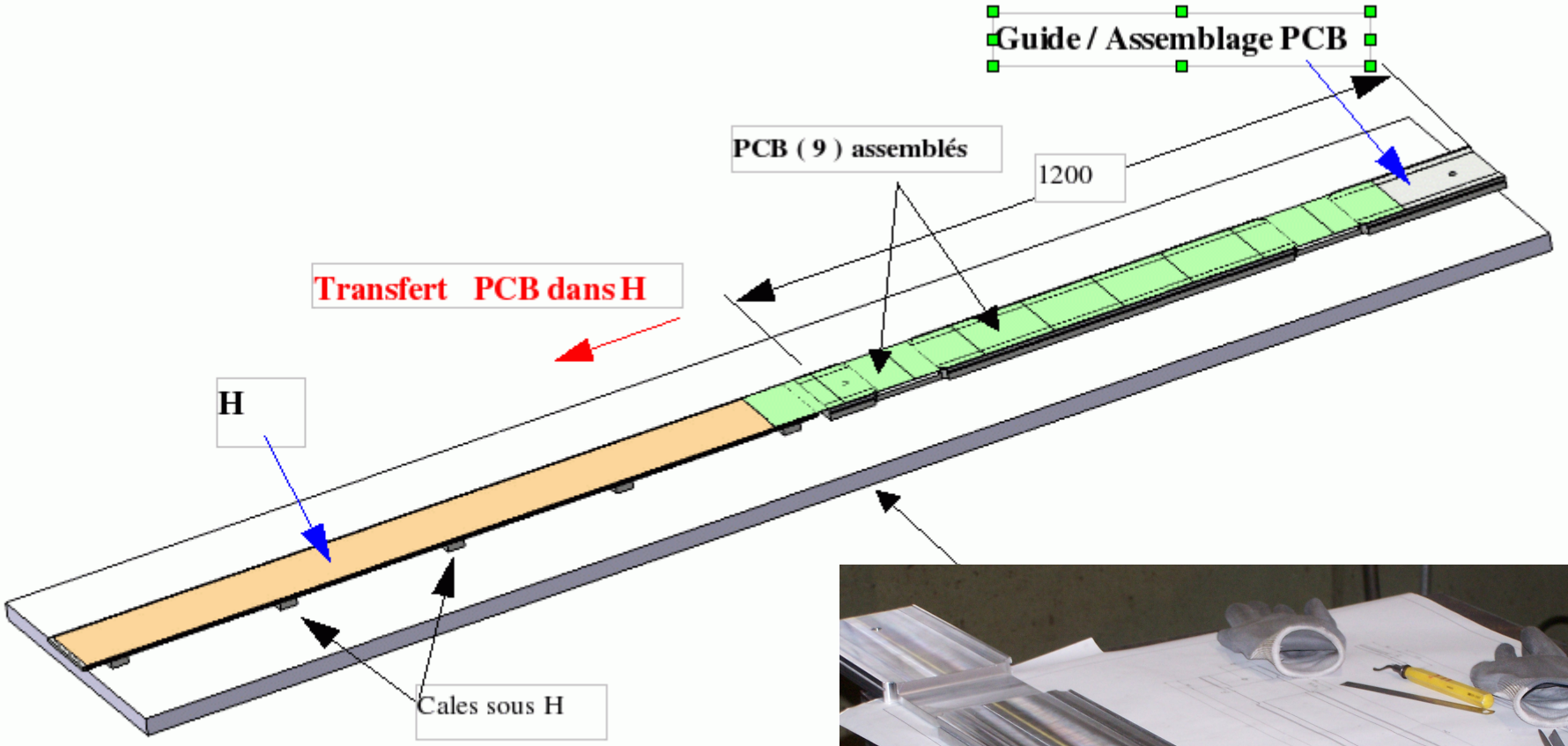


- ⇨ Design : *OK*
- ⇨ Simulations : *OK*
- ⇨ Copper plate : *OK*
- ⇨ Interconnect : *OK*
- ⇨Exp. setup : *OK*

Next tests with EUDET structure

- First test measurements did validate simulation
- However conclusions compromised by convection in workshop and not optimal thermal contacts with copper drain
- Optimisation studies ongoing – Continuation of tests Middle of May 09

Transfert PCB / H



Conclusion and Outlook

- Technical Design finished in Oct. 2008

  Preparation and conduction of Demonstrator Tests since then

- In the middle of the studies with the demonstrator
  - First measurement for thermal analysis
  - Assembly of alveolar structure finished
  - Integration cradle for long slab ready
  - Revision of thermal drain ongoing

Demonstrator studies finished by July 2009
Will cover most if not all mechanical aspects described in EUDET proposal

Conclusion and Outlook cont'd

- Towards the EUDET Module

  - Construction of H Structures and alveolar layers seems feasible
    Demonstrator can be extrapolated to full blown structure

  - “Wrapping” of Slab and Integration Cradle for 'real' slab
    - First protoype in hand - needs further study
    - needs special tools which are very expensive!!!!

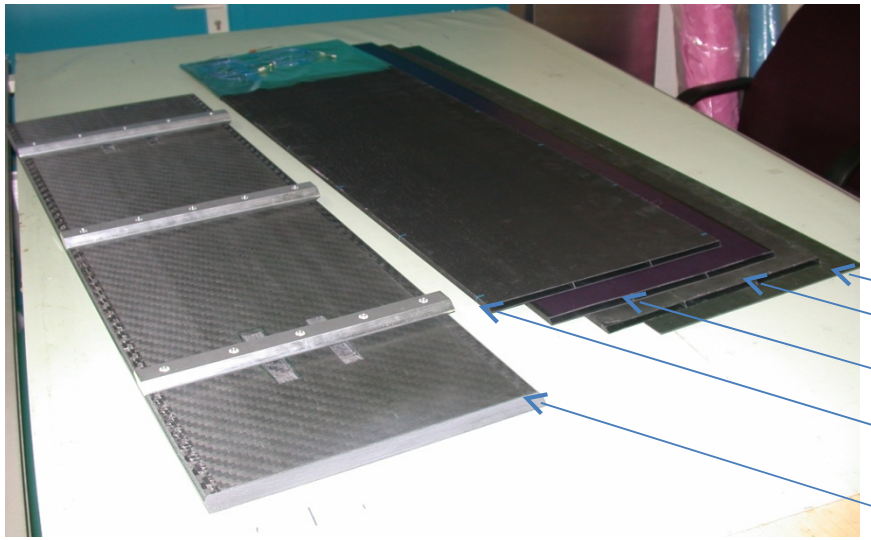
- Excellent progress concerning Si Wafers
  - Wafers according to specs available (However expensive)
  - Corss talk problem understood

- Focus of getting the VFE accomplished in (early) 2010

- “Shipping” signals out
  Interface to the DAQ and beyond will be advancing

First Assembly of the Alveolar Structure for the Demonstrator

Mechanical Structure only slightly smaller than for EUDET Module



All pieces for mechanical housing of “Demonstrator” Slabs available

SPIROC in ECAL

- Limitations :
  - Dynamic range :
    - 500 MIP/cell → same as physics prototype
  - Number of channels :
    - 36 channels instead of 64 → lower granularity