Summary on Vertex and Tracking session

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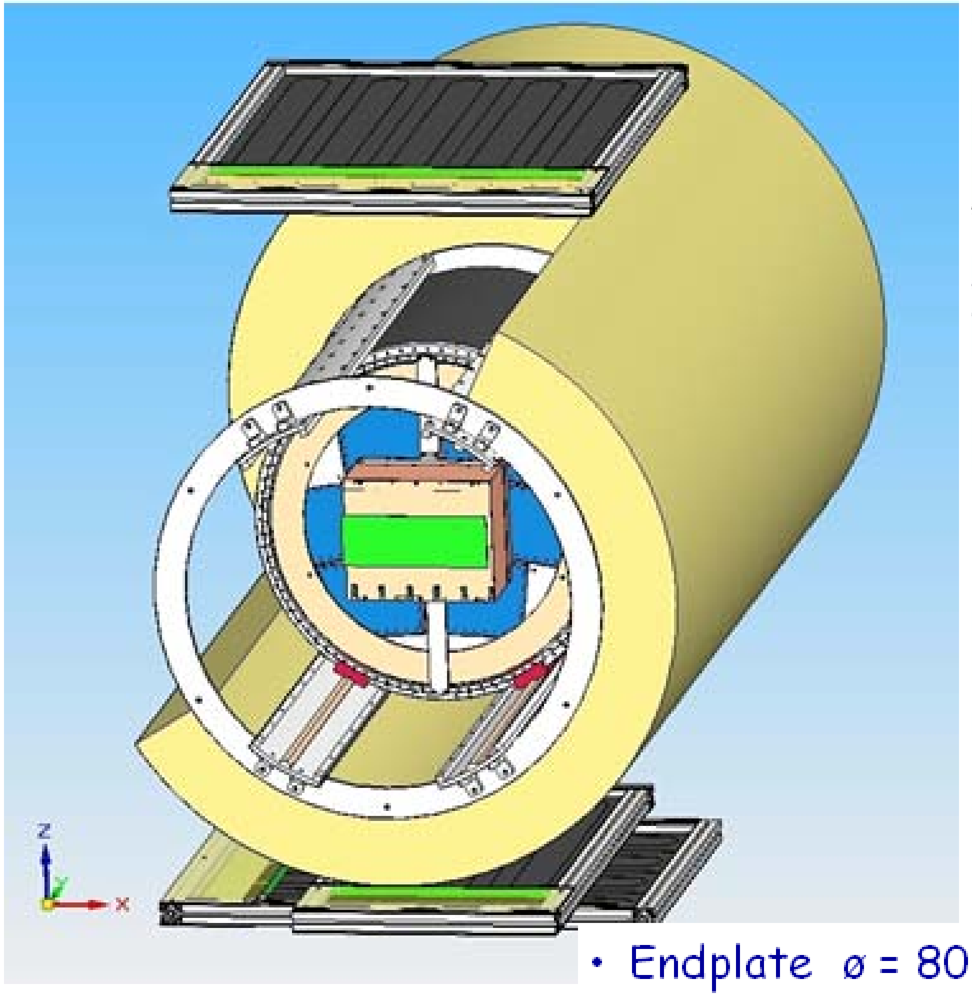
-on behalf of convenors of Vertex and Tracking session

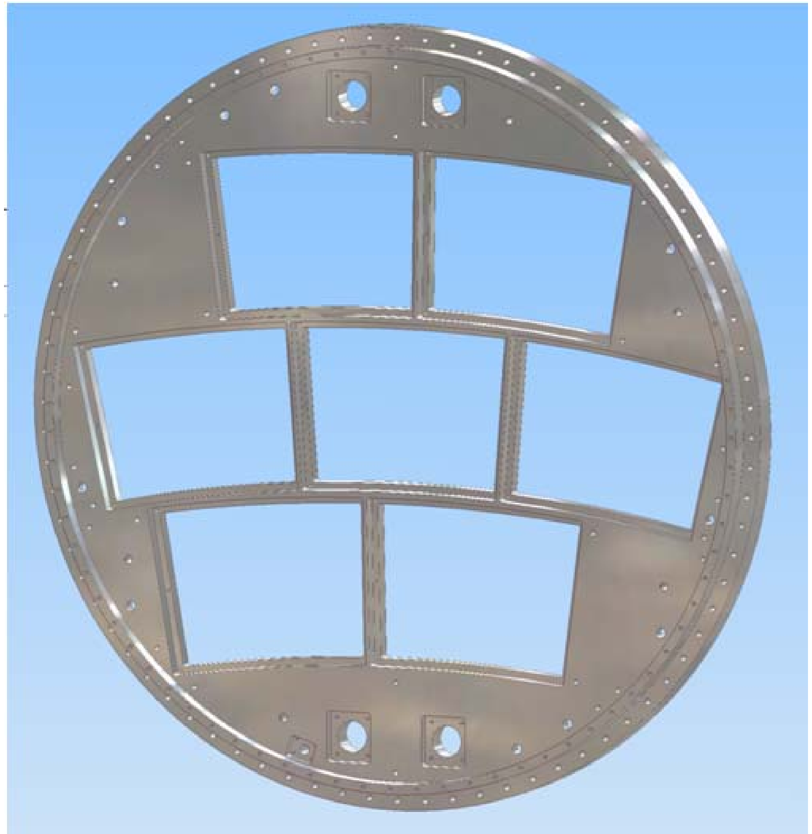
TILC09 – Tsukuba – Japan
April 17-21st, 2009

Outline

- 14 talks presented
  - TPC: 3 talks
  - Si tracking: 3 talks
  - Vertex: 4 talks
  - Software & algorithm: 2 talks
  - Performance studies for different concepts: 2 talks
    - Performance of the SiD vertex and tracking design; a status report, presented by Marcel DEMARTEAU (FNAL)
    - 4th tracker performance, presented by Franco GRANCAGNOLO (INFN Lecce)
      - Very nice talks, with a lot of information and well organized
      - More or less covered at ACFA plenary on 17th
      - Will not be covered today (too much information and too little time)

ILC-TPC Large Prototype



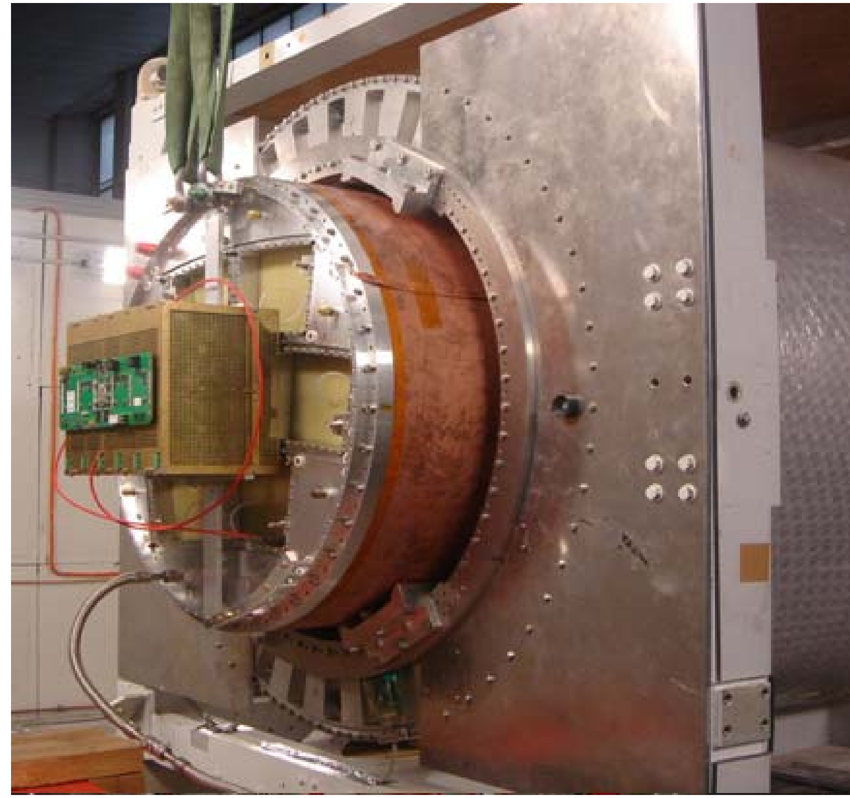


- Endplate ø = 80 cm of 7 interchangeable panels of 23 cm:
  - Micromegas
  - GEMs
  - Pixels (TimePix + GEM or Microgemgas)

Micromegas LP1 test, presented by David Attie (CEA Saclay)

- Excellent start for the Micromegas TPC tests within the EUDET facility.

  Smooth data taking.
- Two panels were successively mounted in the Large Prototype and 1T magnet
  - standard anode

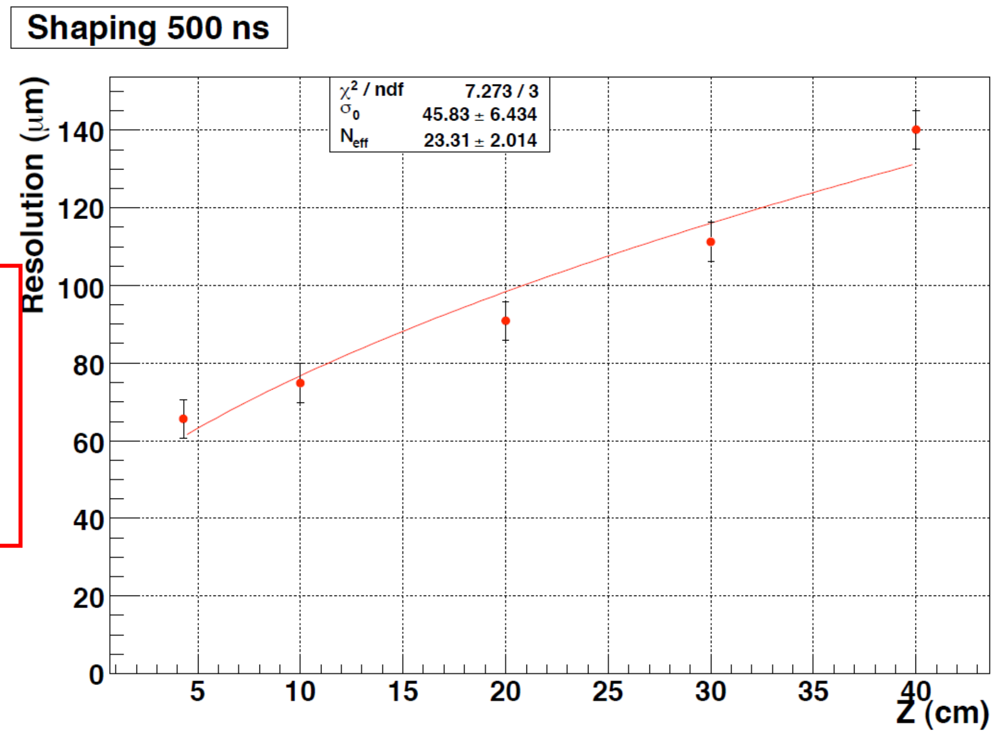


  - resistive anode (carbon loaded kapton) with a resistivity ~ 5-6 MΩ/□

Micromegas LP1 test (cont.)

- First analysis results confirm excellent resolution at small distance: 50 µm for 3mm pads

- Resolution (z=0): σ_0 = 46±6 microns with 2.7-3.2 mm pads
- Effective number of electrons: N_{eff} = 23.3±3.0 consistent with expectations

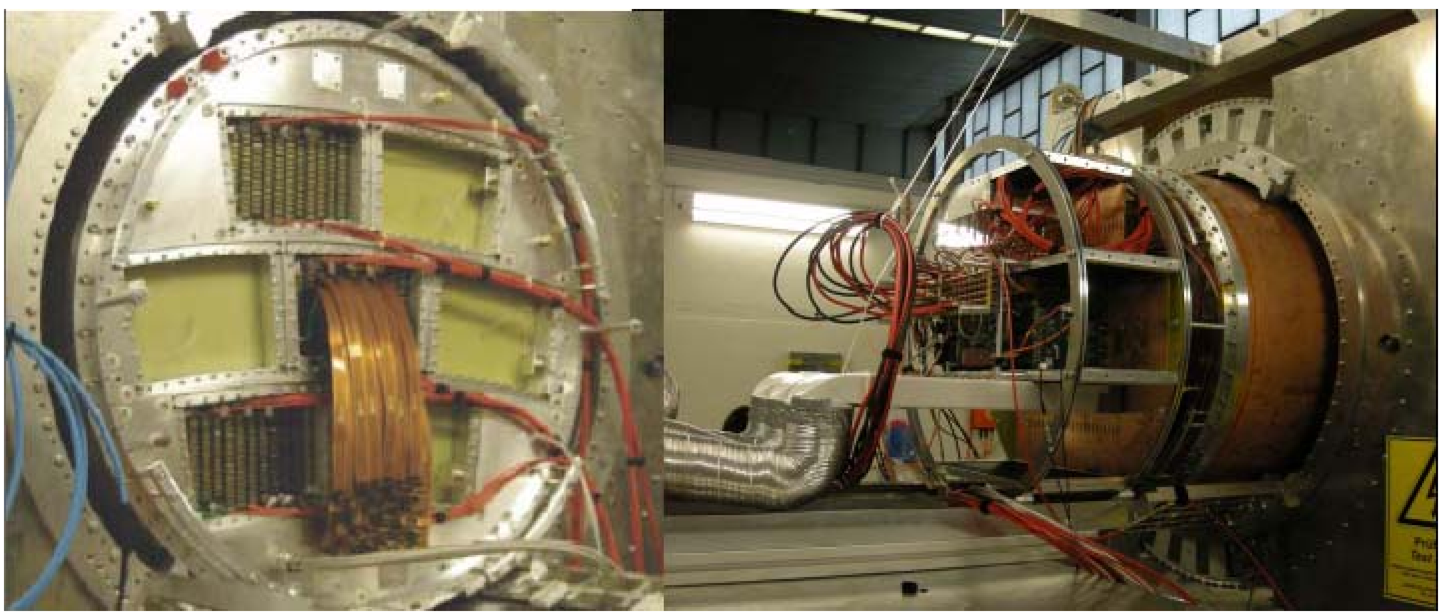


- Expect even better results with new (bypassed shaper) AFTER chips
- Plans are to test several resistive layer fabrication, then go to 7 modules with integrated electronics
- Two other resistive technology are planned to be tested:
  - resistive ink (~1-2 MΩ/□) ready for next beam tests in May
  - a-Si thin-layer deposit in preparation

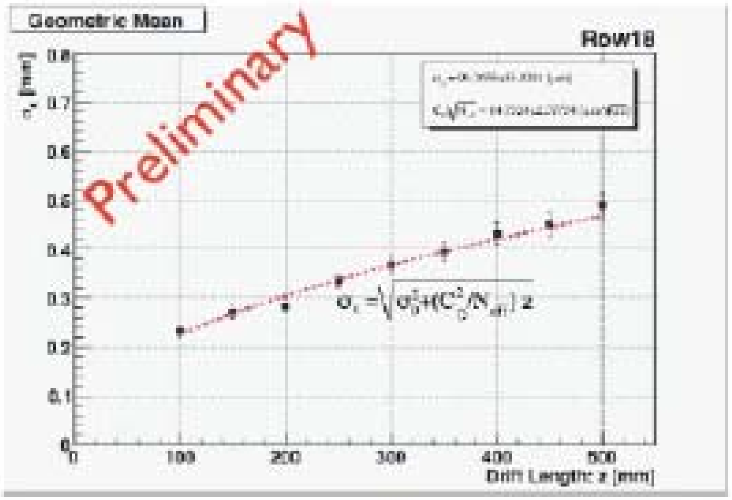
GEM LP1 test, presented by Akira SUGIYAMA (Saga Univ.)

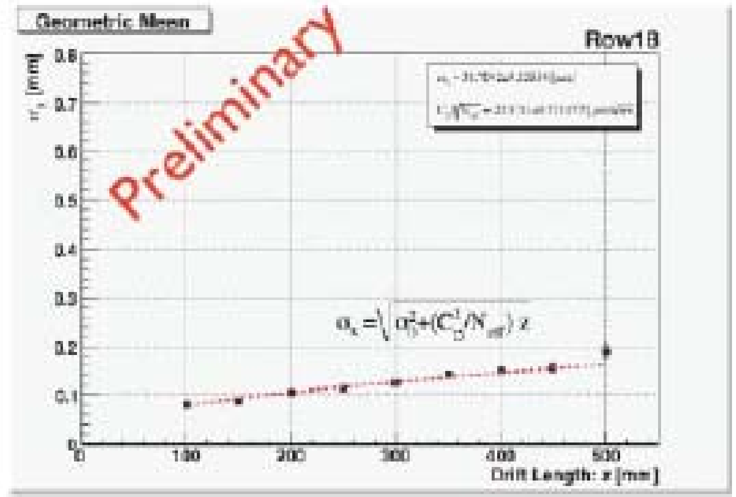
- GEM module

minimize insensitive area pointing IP between modules (limited frame)



GEM LP1 test (cont.)





B=0T

B=1T

$$\frac{C_D}{\sqrt{N_{eff}}} = 65 \pm 2[\mu m/\sqrt{cm}]$$

$$\frac{C_D}{\sqrt{N_{eff}}} = 22.6 \pm 0.7[\mu m/\sqrt{cm}]$$

Preliminary results seems to be

quite consistent with that obtained w/ small prototype

More will come (soon)

after software development and further analysis

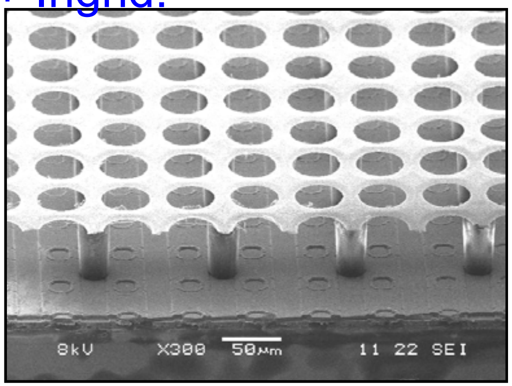
Complete test with GATE is scheduled in winter

Update on Silicon Pixel Readout for a TPC at NIKHEF,

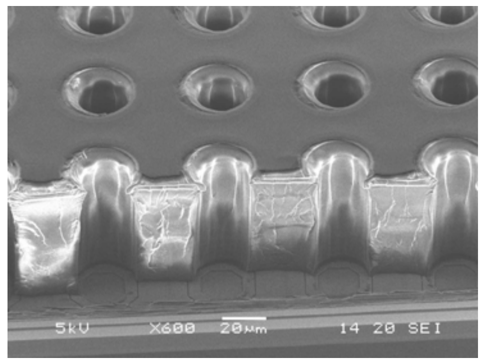
presented by Jan TIMMERMANS (NIKHEF)

- Different Grid structure and protection methods are under study

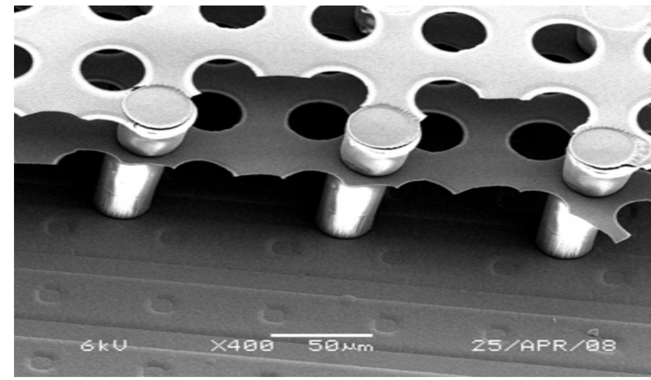
Timepix chip + SiProt + Ingrid:



GemGrids, more robust than Ingrids



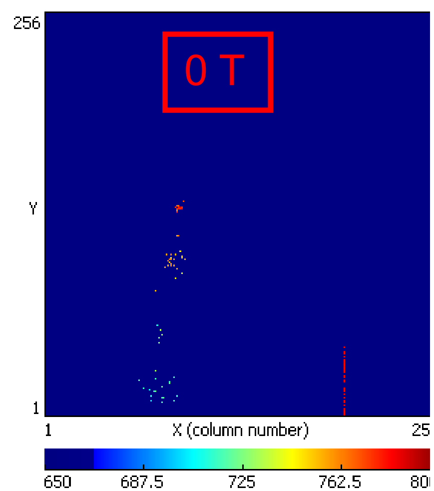
TwinGrid: reduction of discharge probability & Lower ion backflow



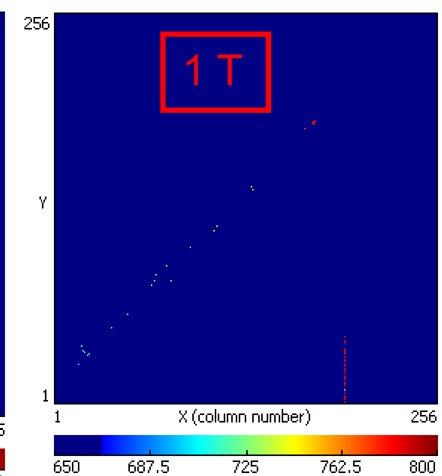
protection layer: 15 or 20 µm aSi:H, 7 µm Si3N4

- Tracks
- Scaling up.
  - 4 chip detectors (3X3 cm): soon
  - 64 chip detector (12X12 cm): later in 2009/10

"large" diffusion

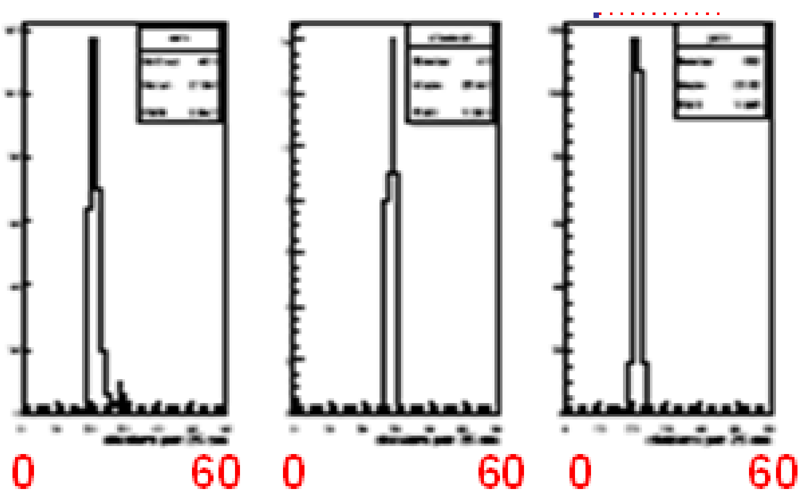


"little" diffusion



Update on Silicon Pixel Readout for a TPC at NIKHEF (cont.)

- Cluster counting with Timepix
  - Track search/reconstruction using Hough transforms
  - 2D and 3D track fits
  - Drift velocity measurements
  - Diffusion measurements
  - Cluster distances and cluster counting



- Cluster counting distribution In in He/iC4H10
- Using 25 cm tracklength

Electrons:

Avg=28.4/cm rms=1.2

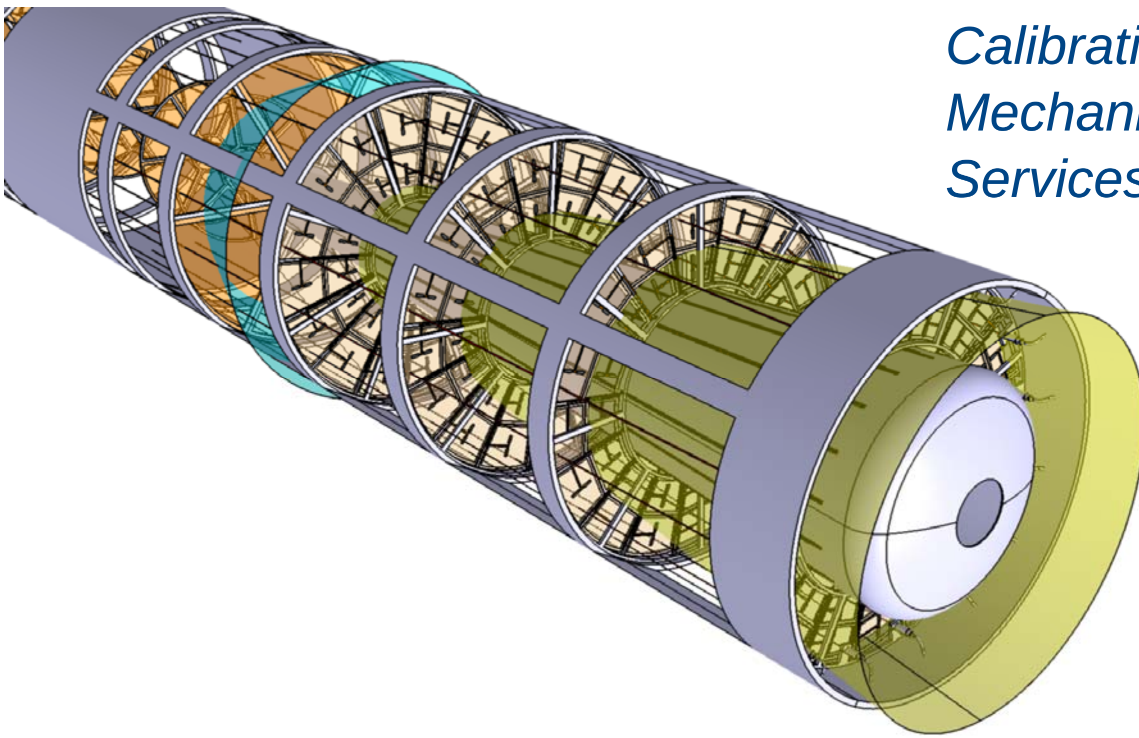
Pions: 21.0/cm 1.2

Forward Tracking at the next e+e- collider, presented by Alberto RUIZ JIMENO (Universidad de Cantabria)

- On behalf of Spanish Network for Future Linear Accelerators
  - A lot of activities in Spain on ILC detector and accelerators
- "forward physics" oriented
  - Forward tracking is very important in many physics cases;
  - Pose great challenge:
    - The material
    - Hermetic coverage
    - Significant background at smallest radii
    - The unfavorable orientation of the magnetic field
    - Abundant low momentum tracks – pattern recognition
  - For ILD, we are nowhere near the goal, and far from the performance of the central tracker

Forward Tracking at the next e+e- collider (cont.)

- R&D on Detectors, covering:
  - sensors: DEPFET pixels, 3D sensors, thinned microstrips, semitransparent microstrips.
  - FE electronics, development of DSM r/o chip.
  - mechanics: deformation and thermal analysis.
- Towards an engineering design



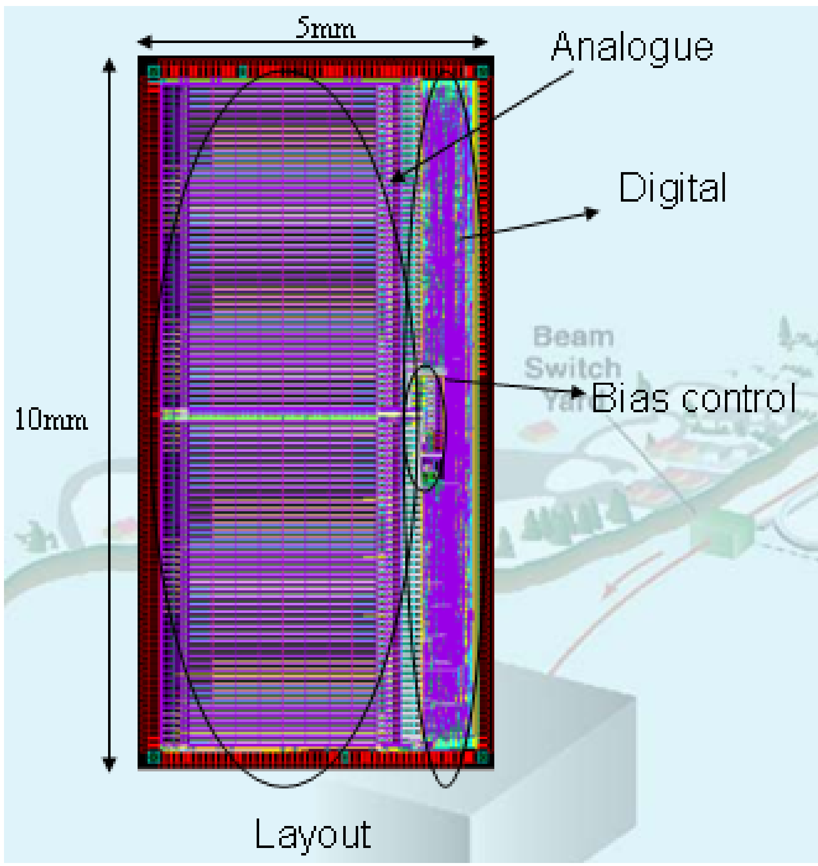
Calibration/alignment
Mechanical support
Services

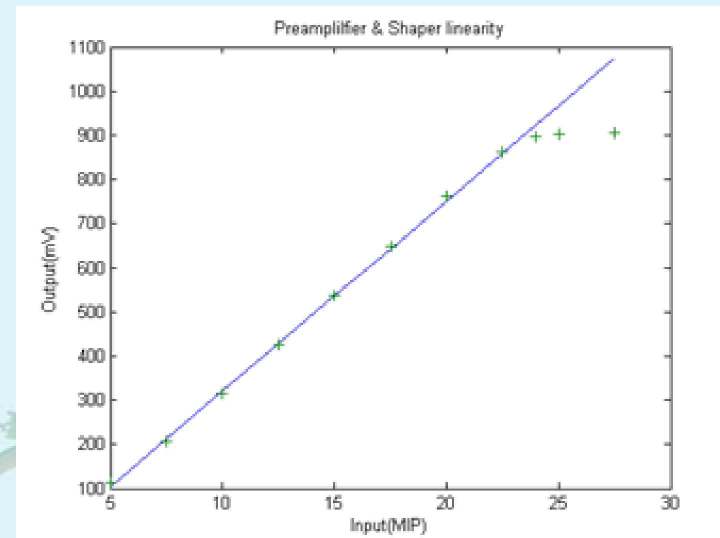
Integrating Silicon tracking in ILC detector concepts: solutions & challenges, presented by Aurore SAVOY-NAVARRO (LPNHE-Paris/CNRS-IN2P3)

- Both SiD and ILD need silicon tracking
- The LOI gave a serious boost in developing realistic scenarios for integrating the Si tracking in the various detector concepts.
- The all-Si case is much simpler for integrating than the hybrid or combined case (ILD)
  - ILD need: FTD, SIT, SET, ETD
- But there are many common issues and challenges with often similar solutions in both schemes.
- This reinforces the interest of having an horizontal R&D
  - addresses these issues on common basis
  - gather the efforts of many teams to work on the best possible solutions.
- Moreover the test beams and prototypes developments are instrumental as well as the combined tests with other sub-detectors. There also an horizontal R&D helps in merging the efforts.
- The dynamics created with the LOIs should not be lost!!

A mixed mode chip in 130nm for Silicon Strip readout at the ILC, presented by Aurore SAVOY-NAVARRO (LPNHE-Paris/CNRS-IN2P3)

- Fully take advantages of ILC machine cycle:
  - Long shaping time





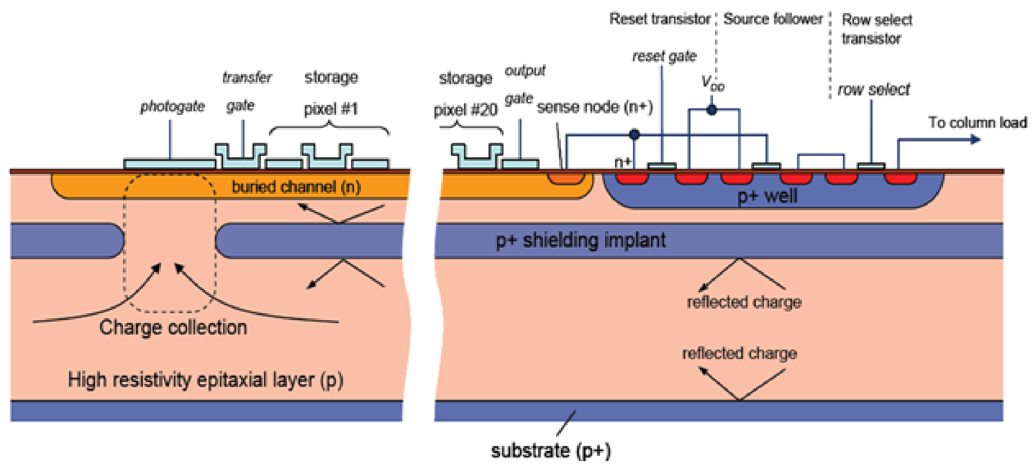
Linearity of the preamplifier and the shaper

Measured power dissipation per ch
(all the analog chain up & A/D included):
~1.35mW/channel

Measured gain ~ 43mV/MIP
@ 2.6% of nonlinearity up to 24MIP

First results with prototype ISIS-2 devices for ILC vertex detector, presented by Chris DAMERELL (Rutherford)

- Due to the funding situation in the UK, spare time work with small budget
- ISIS: In-situ Storage Image Sensor
- Operating principle:
  - Signal charge collected by an array of photogates
  - Charge is transferred to an 'in-pixel' register, 20 times during the 1 ms-long train
  - Output for each bunch train thus comprises 20 frames of low-noise time-sliced data



- ISIS-1 was designed, manufactured and tested successfully
- Prototype ISIS-2 with 0.18 μm CMOS process: works
- Then
  - Full-scale ISIS-2 array test
  - ISIS-3 and beyond
- Funding situation in UK may get better
- Looking for: new partner and experts working on it

Towards CMOS pixel sensors fully adapted to the inner and outer layers of the ILC vertex detector, presented by Marc WINTER (IReS)

Sensor r.o. architecture :

- final sensor for EUDET telescope (MIMOSA-26) fabricated
  (0.7 Mpix, $t_{int} \sim 110\ \mu s$, binary output with integrated $\emptyset$, $\sigma_{sp} \gtrsim 3.5\ \mu m$)
- preliminary lab test results confirm functionning with expected noise performances
- if beam test results satisfactory (Summer), the design will be adapted to required VTX performances
  $\hookrightarrow$ $t_{int} \sim$ 25–50 μs (2-sided r.o. for inner layers) & $\sim$ 100 μs (1-sided r.o. for outer layers)
- Plan : move to 0.18 μm technology (6 metal layers, more compact circuitry, faster, etc.)

Sensor integration $\rightarrowtail$ PLUME project :

- by 2012 : double-sided ladder equipped with 2 x 6 MIMOSA-26 sensors
  (active area $\sim$ 2 x 12.5x1 cm^2, mat. budget $\gtrsim$ 0.2 % X_0)
- 2009 : 1st proto. with 2x2 MIMOSA-20 sensors mounted on flex cable and SiC ($\sim$ 0.5 % X_0 in total)
  $\rightarrowtail$ tests at CERN-SPS in Novembre

3D sensors (Chartered-Tezzaron) :

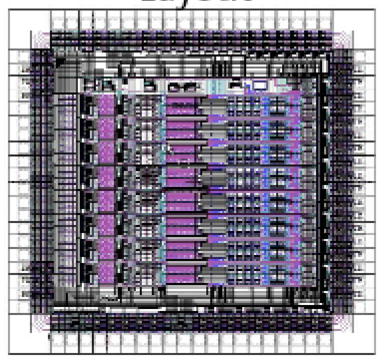
- 3 different sensors under devt : delayed r.o. with latch, fast rolling shutter, 3-Tier mixed CMOS
- submission within $\sim$ 2 weeks $\Rrightarrow$ test results in Autumn

Development of Readout ASIC for FPCCD Vertex Detector,

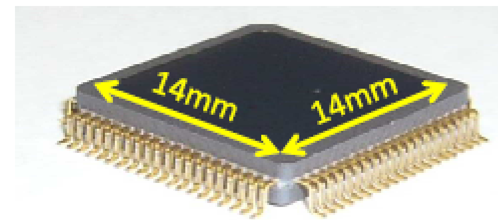
presented by Kennousuke ITAGAKI (Tohoku Univ.)

- A readout ASIC for FPCCD has been developed.
  - Delivered in January 2008
  - 0.35μm TSMC process
  - Chip size : 2.85 mm × 2.85 mm
  - # of pad : 80
  - # of readout channel : 8

Layout

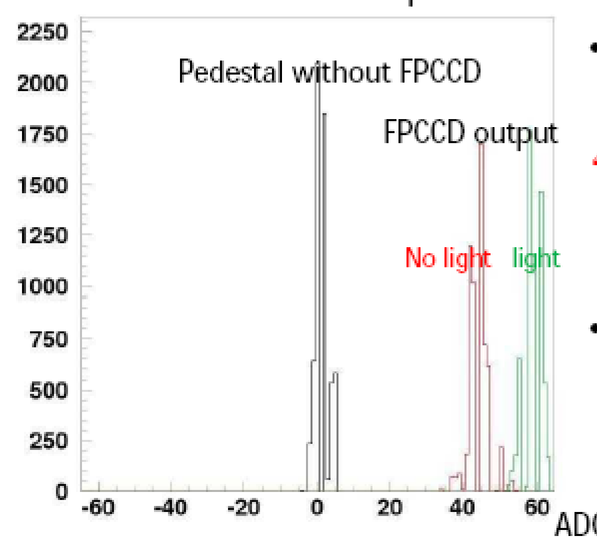


Prototype ASIC with a package



- The performance of the test sample was checked
  - ➢ conversion rate : ～1.5Mpix/sec
  - ➢ Noise level : ～70e
  - ➢ ADC linearity : ±80e

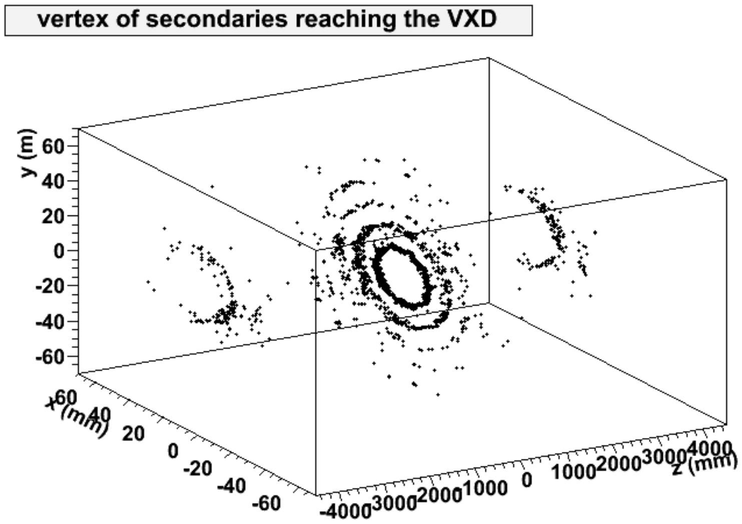
ADC distribution
Conversion rate ~300kpix/sec



- Further plan
  - High speed readout
  - FPCCD readout
  - Noise level

Incoherent pair background studies for the ILD vertex detector, presented by Rita DE-MASI (IPHC-Strasbourg)

- Secondary particles reaching the VXD are originated mostly by the interaction of beamstrahlung e± with the BeamCal, the beam tube or the VXD itself.

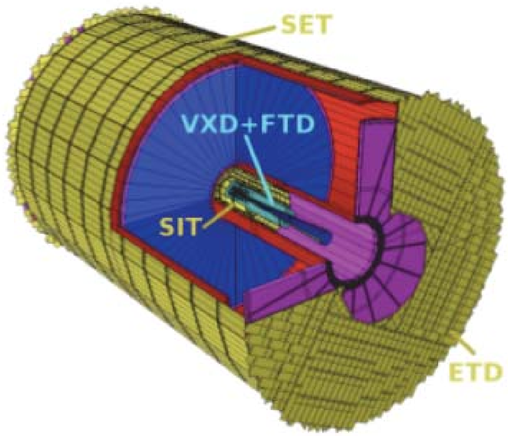


- The occupancy in the two innermost layers is several % (anti-DID included, no safety factor).
- The occupancy grows by a factor >2 for the low-P option.
- A reduction by a factor 4 to 5 follows from different sensor parameters: thinner sensitive volume, faster readout, …

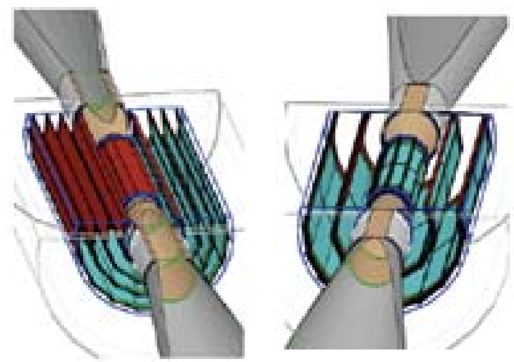
Current status of Tracking Software used for ILD Mass Simulation, presented by Steve APLIN (DESY)

- Detector simulation

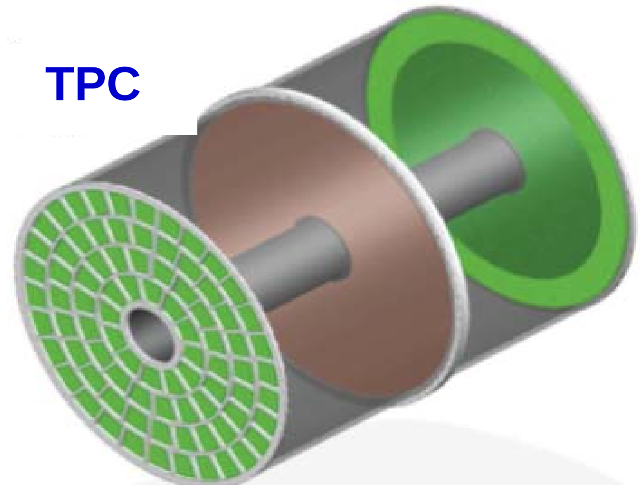
FTD-SIT-ETD-SET



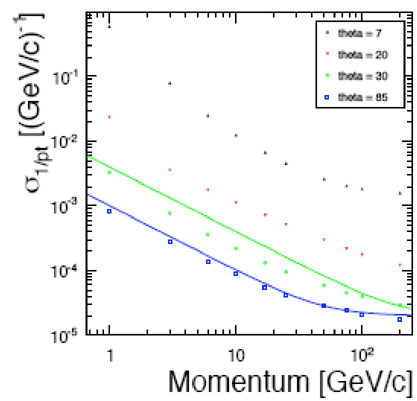
VXD

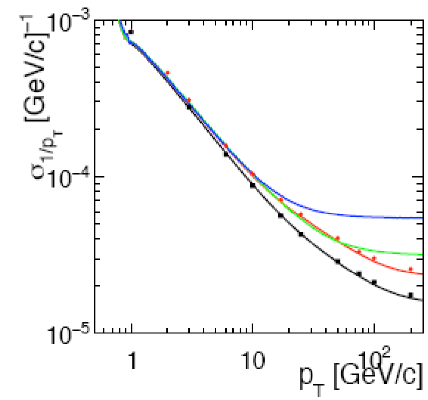


TPC



- Coverage and material cost are given
- Reconstruction software code is very stable
  - Impact parameter resolution
  - Momentum resolution





- Further plan: BKG studies, Track mode, Marlin soft

Vertex reconstruction with tracks described by a Gaussian mixture, presented by Winni Mitaroff (HEPHY Vienna)

- An e^-/e^+ track, reconstructed with a stochastic model for e-loss by bremsstrahlung (Bethe-Heitler), can be described by mixture of M_k Gaussians:

Virtual measurement's p.d.f. $\wp(\mathrm{p}_k) = \sum_{i=1}^{M_k} \gamma_k^i \cdot \Gamma\left(\mathrm{p}_k; \mathrm{p}_k^i, \mathrm{V}_k^i\right)$, $\quad \sum_{i=1}^{M_k} \gamma_k^i = 1$, $\quad k$ = track index.

- Subsequent vertex reconstruction requires a **Gaussian sum filter** (GSF):

Prior vertex position's p.d.f. $\wp(\mathrm{x}_{k-1})$, based upon tracks $\{\mathrm{p}_1, \ldots \mathrm{p}_{k-1}\}$, is a Gaussian mixture of components $j = 1 \ldots N_{k-1}$. Adding track p_k yields the posterior p.d.f. of vertex position and track params at vertex

$$\wp(\mathrm{x}_k, \mathrm{q}_k) = \sum_{i=1}^{M_k} \sum_{j=1}^{N_{k-1}} \gamma_k^i \, \omega_k^{ij} \cdot \Gamma\left((\mathrm{x}_k, \mathrm{q}_k); (\mathrm{x}_k^{ij}, \mathrm{q}_k^{ij}), \begin{pmatrix} \mathrm{C}_k^{ij} & \mathrm{E}_k^{ij} \\ \mathrm{E}_k^{ij\mathrm{T}} & \mathrm{D}_k^{ij} \end{pmatrix} \right), \quad \sum_{j=1}^{N_{k-1}} \omega_k^{ij} = 1$$

by **component-wise Kalman filters**, resulting in a Gaussian mixture of $N_k = M_k \cdot N_{k-1}$ components. This exponential growth of N_k can be limited by repeatedly collapsing a "similar" pair of components into one.

- After iteration over all tracks, a **Gaussian sum smoother** will be applied:

Each estimate $\wp(\mathrm{q}_k)$ of track params at vertex contains information from tracks $\ell = 1 \ldots k$, thus only the last one ($k = n$) contains it all. Running two GSFs in ascending and descending order, respectively, allows each track p_k being formally added as the last one, yielding the smoothed estimate $\wp(\mathrm{q}_k^*)$ with full information.

- The GSF will be implemented into our vertex reconstruction toolkit RAVE.

Thanks to all the speakers in this session!

Thanks to those from whom I "borrowed or took" slices from!

Thank you for your attention!