

# ***Silicon tracking for the ILD***

A. Savoy-Navarro , LPNHE, UPMC/IN2P3-CNRS  
*for the SiLC collaboration members participating to ILD:*

IMB-CNM/CSIC in Barcelona, University of Barcelona, IEKP Karlsruhe University,  
Korean group (Kyungpook Nat. University in Daegu, Yonsei University, Korea National University  
and Seoul National University all in Seoul), Moscow State University, Obninsk State  
University, LPNHE-UPMC & CNRS-IN2P3 Paris,  
Charles University in Prague, SCIPP & UC Santa Cruz,  
IFCA/CSIC & University Santander, Santiago de Compostela University,  
Torino University & INFN,  
IFIC/CSIC & University Valencia, HEPHY-Academy of Sciences Vienna  
and a few more to be convinced...

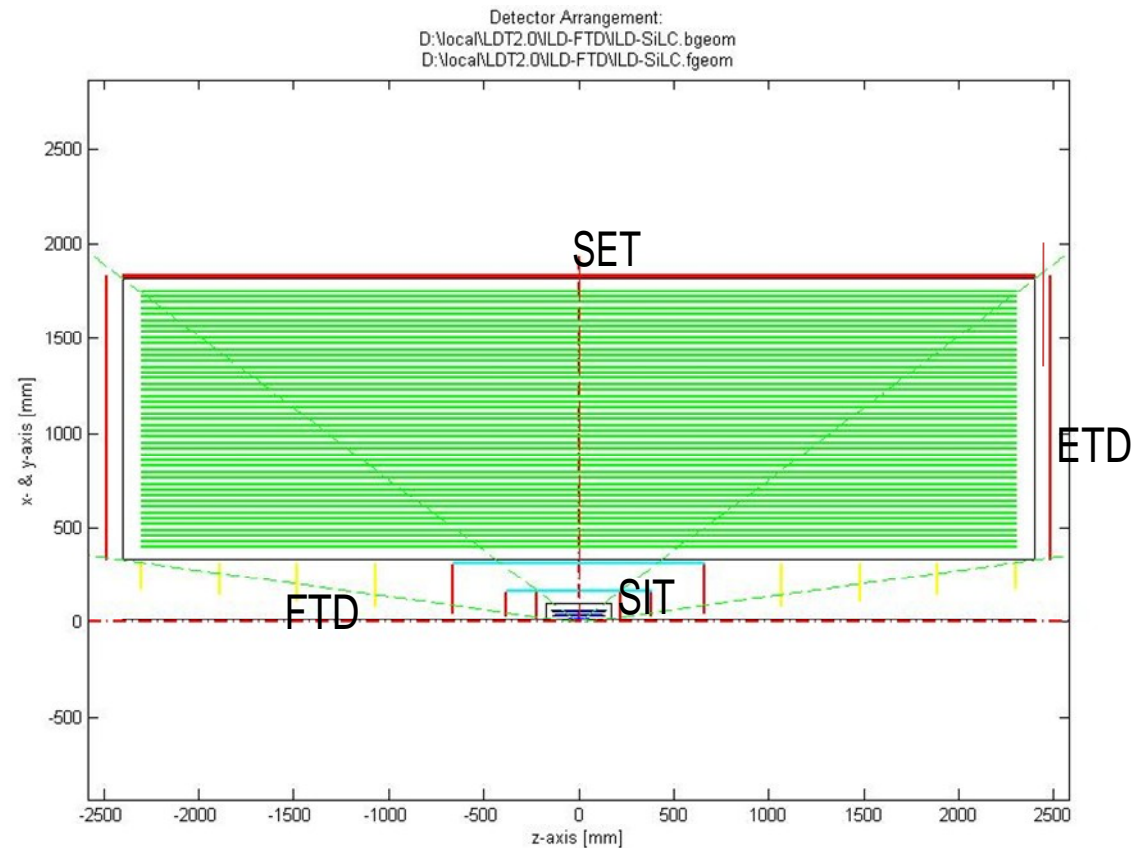
***Third ILD Collaboration Meeting, Ewha Womans University,  
Seoul, February 16-18, 2009***

# Topics

- Role of Silicon tracking in ILD
- Silicon system performances
- Calibrations
- Construction and integration issues
- Dedicated R&D on advanced technologies
- Concluding remarks, pending issues

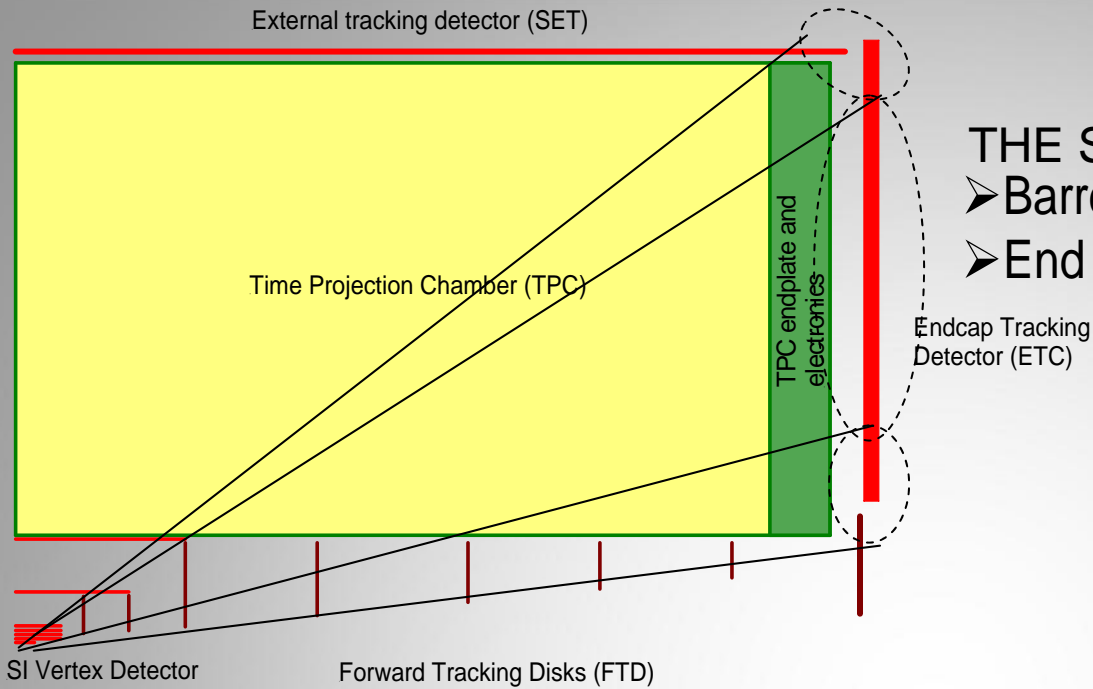
- **Role of Silicon tracking in ILD (brief reminder)**
- Silicon system performances
- Calibrations
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# The Silicon envelope



(by M. Valentan, LicToy)

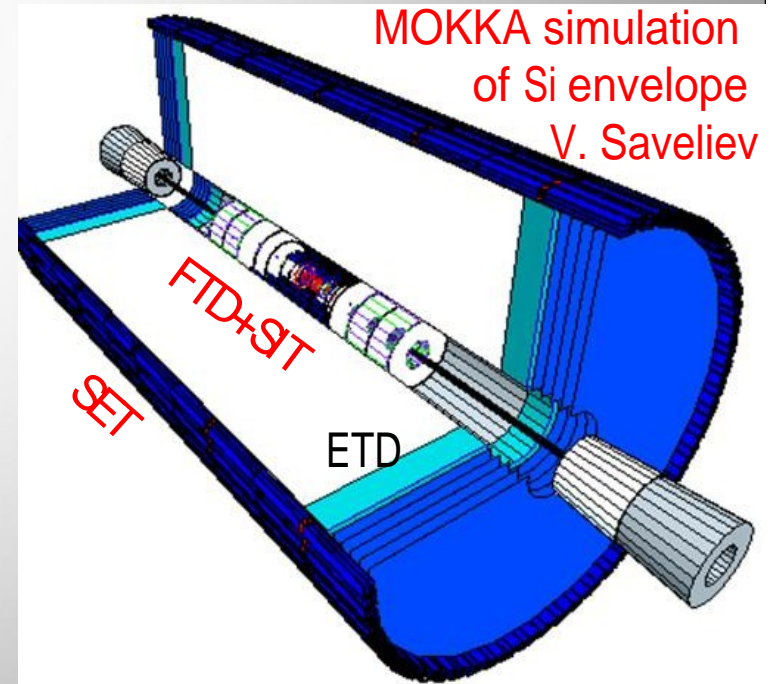
ILD Tracking system is an hybrid system that combines both a central gaseous device with an ensemble of Silicon tracking components all around the TPC.



**THE SILICON TRACKING SYSTEM:**

- Barrel: SIT+SET (3 2D-layers total)
- End Cap/FWD: FTD(7 disks)+ETD (XUV)

higher tracking performances  
 tracking hermeticity  
 alignment  
 distorsion handling  
 time stamping  
 robustness & redundancy

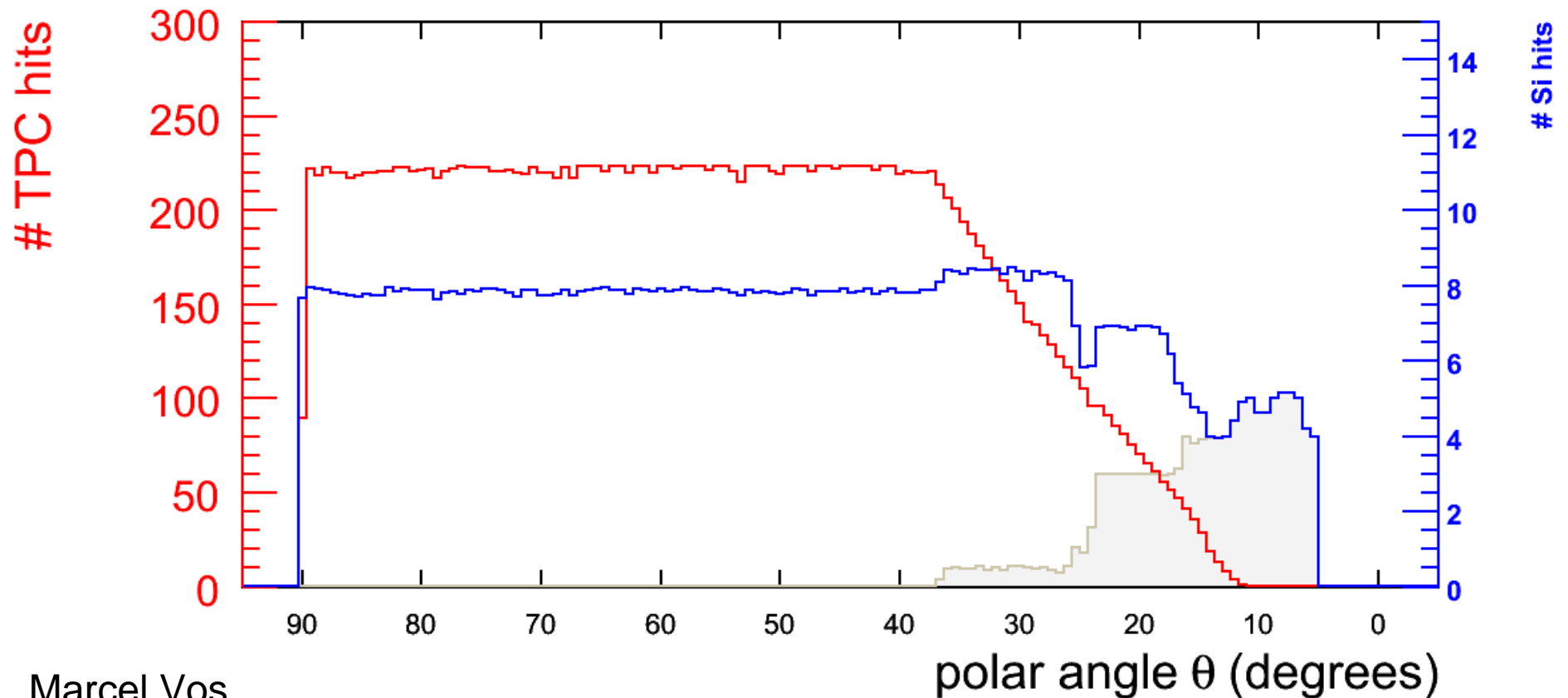


- Role of Silicon tracking in ILD
- **Silicon system performances (some examples)**
- Calibrations
- Construction and integration issues
- Dedicated R&D on advanced technologies
- Concluding remarks, pending issues

M. Vos, J. Duarte, C. Iglesias (Spain), M. Valentan, W. Mitarof, M. Regler (Vienna),  
V. Saveliev (OSU), Z. Drasal (CU Prague), A. Charpy (LPNHE):

***All are focusing on performances and even detailed description of the Si system***

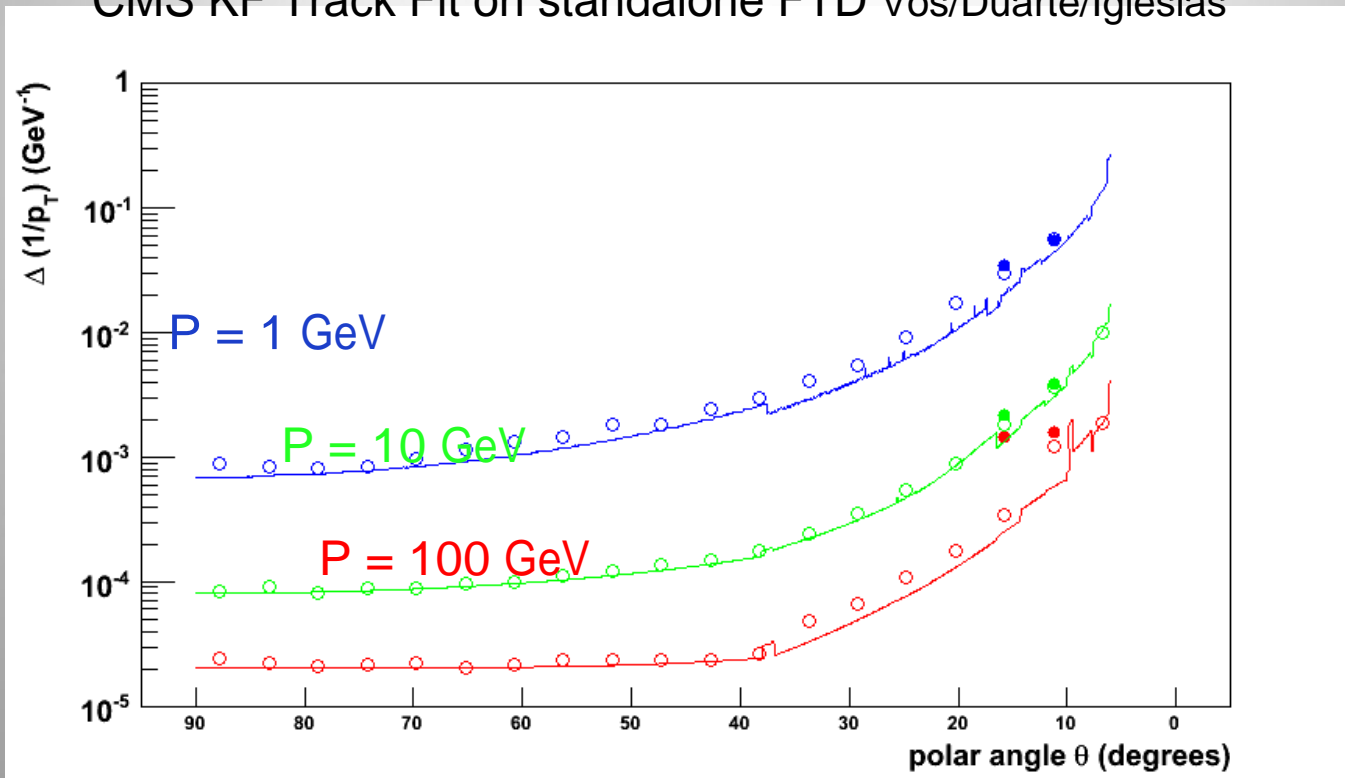
# Angular coverage Silicon vs TPC



Marcel Vos

# Transverse momentum resolution versus polar angle Measured on three single-muon samples with fixed $|p|$

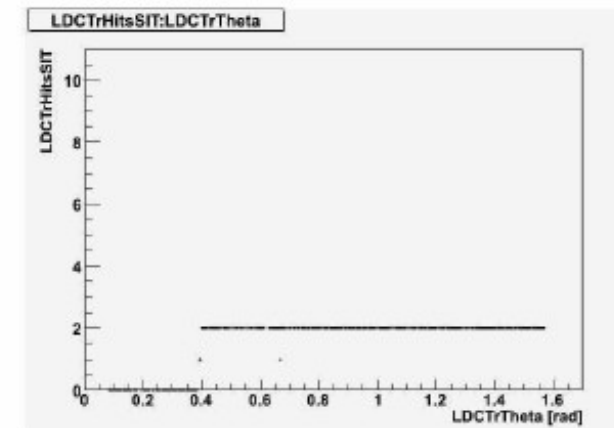
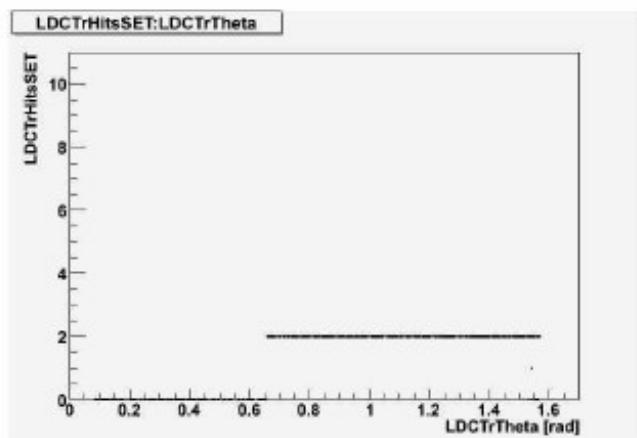
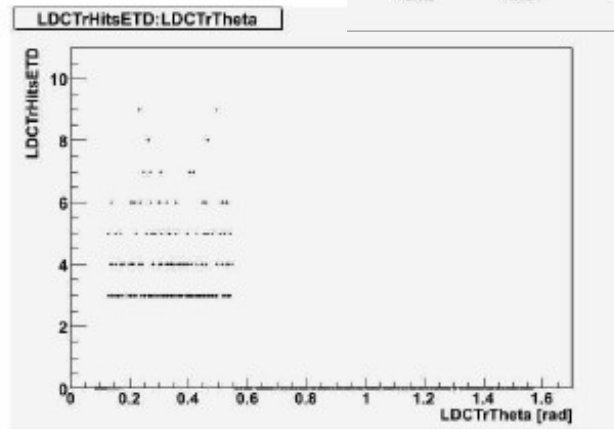
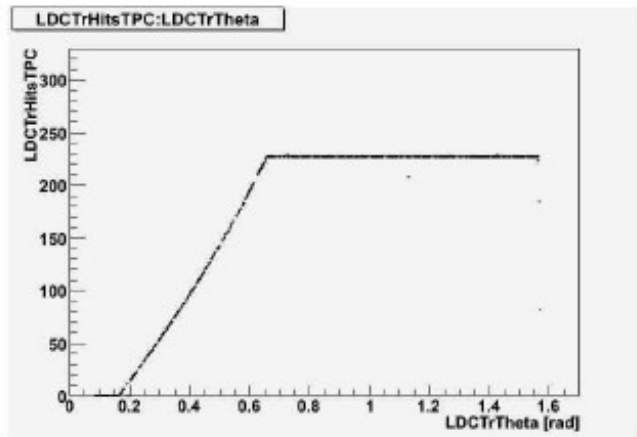
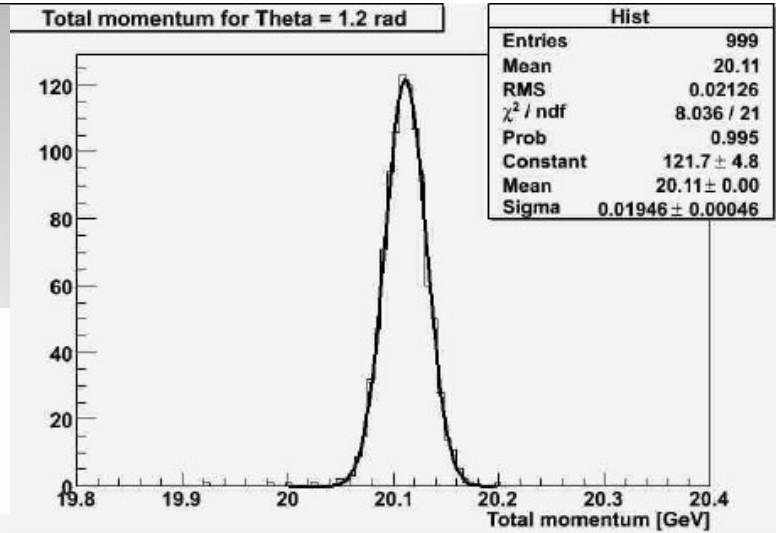
- LiCToy on ILD00 (full KF fit), M. Valentan, HEPHY Vienna
- FullLDCTracking on ILD00 (Mokka/MarlinReco) Vos/Duarte/Iglesias
- CMS KF Track Fit on standalone FTD Vos/Duarte/Iglesias





# Full MOKA ILD00 Reconstruction (V. Saveliev)

# of Hits on TPC, ETD, SIT, SET

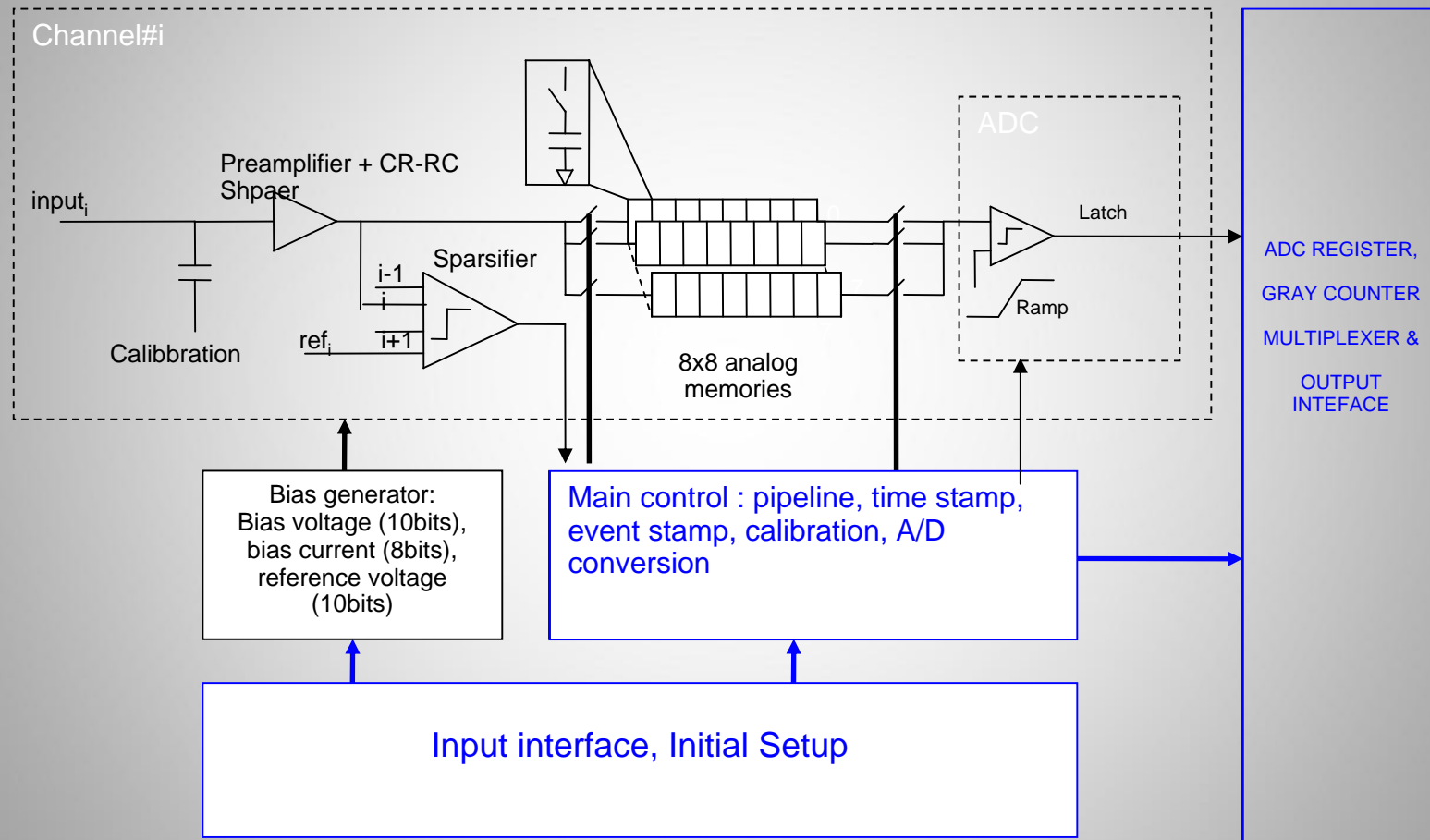


Tracking reconstruction  
of 20 GeV muons at  
1.2 rad

- Role of Silicon tracking in ILD
- Silicon system performances
- **Calibrations**
- Construction and integration issues
- Dedicated R&D on advanced technologies
- Concluding remarks, pending issues

# Calibration of the electronic chain

The FE and readout chain includes in its own design a full calibration system fully automatic/programmable through the digital part:

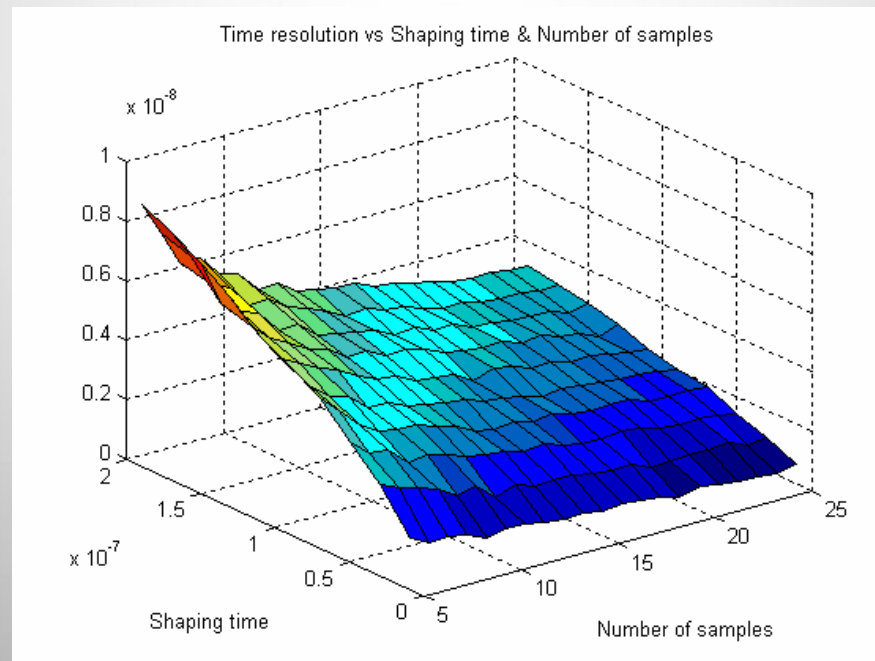


88-channel chip block diagram (Barcelona U. & LPNHE-Paris)

# Time stamping

The electronic chain as presently designed and built allows to time stamp with a **precision of 80 nsec.**

Moreover a more detailed estimate is being re-done taking into account the Shaping time, the number of samples in the analogue pipeline. This is based on the algorithm of Cleland and Stern (see here below).



# ALIGNMENT (IFCA & IMB-CNM)

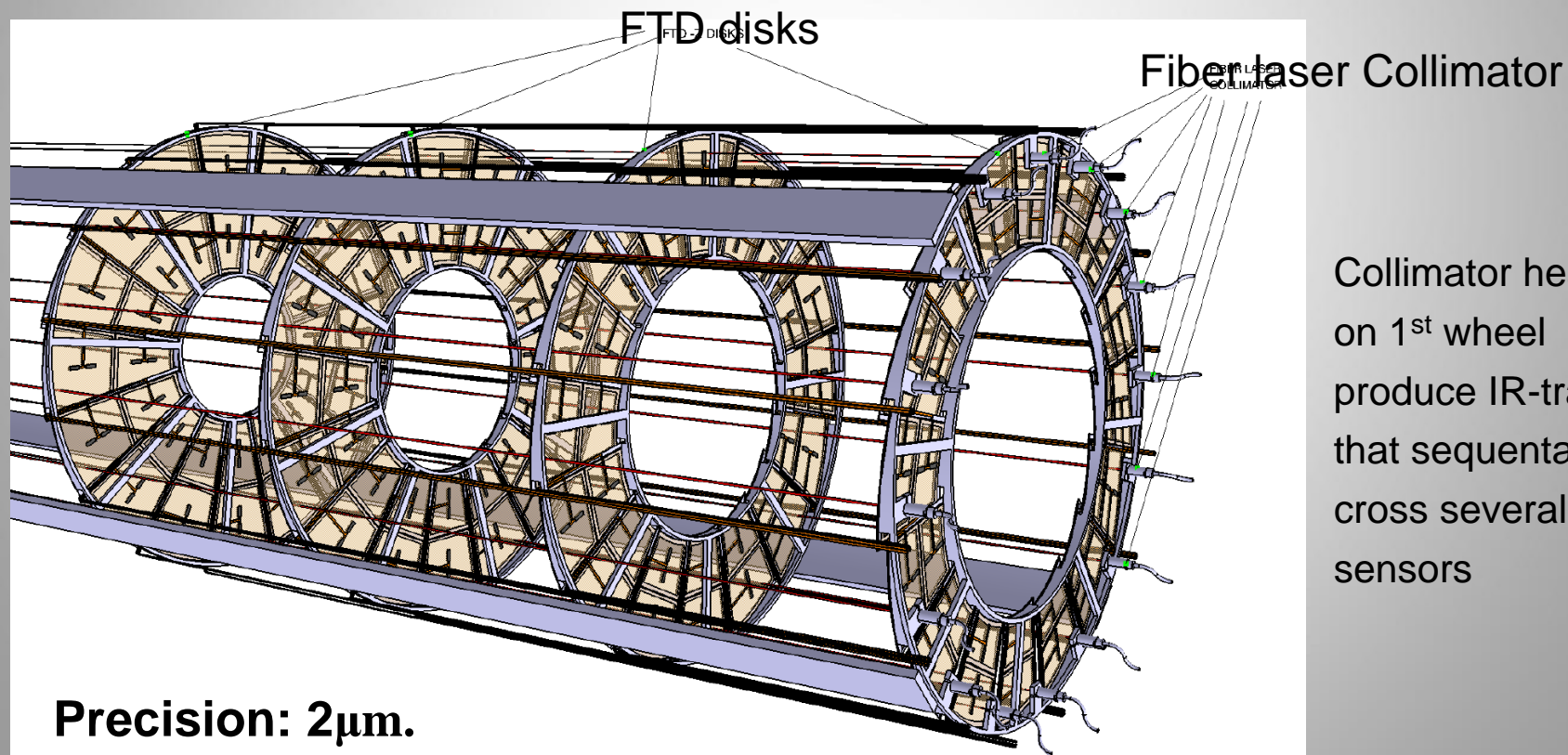
*R. Jaramillo, M. Fernandez, M. Lozano, A. Ruiz, I. Vila*

**Concept of IR alignment system: use IR beams as infinite momentum tracks.(AMS, CMS)**

Selected sensors are traversed by IR beams.

These beams are then measured as particle tracks and a first order alignment scenario is obtained.

The rest of sensors are aligned using particle tracks. The transference of coordinates from optical aligned to track aligned modules is done via sensor overlap.



Collimator heads on 1<sup>st</sup> wheel produce IR-tracks that sequentially cross several Si sensors

**Precision: 2 $\mu$ m.**

*Slide from Marcos Fernandez Garcia (IFCA)*

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***Teams presently involved:***

***HEPHY(simus), IFCA, IFIC, SCU (FTD), LPNHE and Torino Univ.& INFN (SIT, SET and ETD), Obninsk (simus).***

***Collaborative efforts with M. Jore and french integration team, MDI and members from LCTPC.***

# Construction and Integration of a Silicon system into the ILD detector: preliminary ad

The construction and the integration of a Silicon tracking system, part of an hybrid tracking ensemble is much more challenging than an all-Silicon fully integrated system (CMS, SiD and futur s-ATLAS). Among the main challenging issues:

## ➤ **THE SPACE ALLOCATED:**

All Silicon system has all the tracking space for it alone (1.2m radius or so)

Hybrid: only 2cm for the SET, 4cm for the ETD, 20-25cm for SIT+FTD

## ➤ **THE FIXATION and SUPPORT STRUCTURE:**

All Si can build the support structure as desired as well as its own fixing system.

Hybrid: the Si device fully depends on the restricted space and the surroundings.

## ➤ **THE ROLE:**

All Silicon system must primarily satisfies the role of the tracker high performance momentum and spatial resolution measurements.

Hybrid case: the Si component must provide additional functions: alignment, time stamping, handling of distortions of the gaseous detector etc....

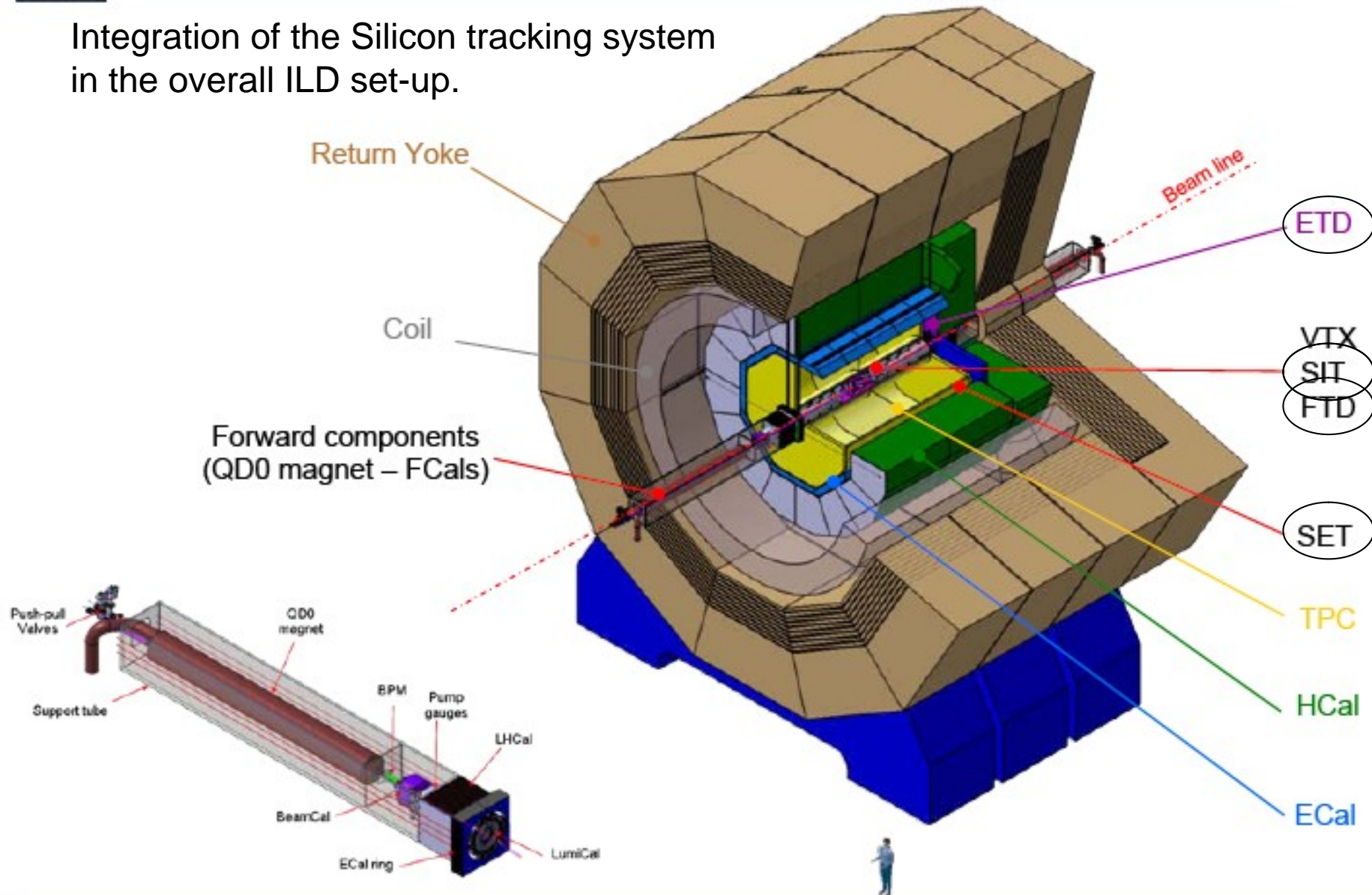
➤ **COOLING:** here also much more constraining in the hybrid case (much more dependant of the neighbours





# ILD0 overview

Integration of the Silicon tracking system  
in the overall ILD set-up.





# Construction and Integration of a Silicon system into the ILD detector: general philosophy

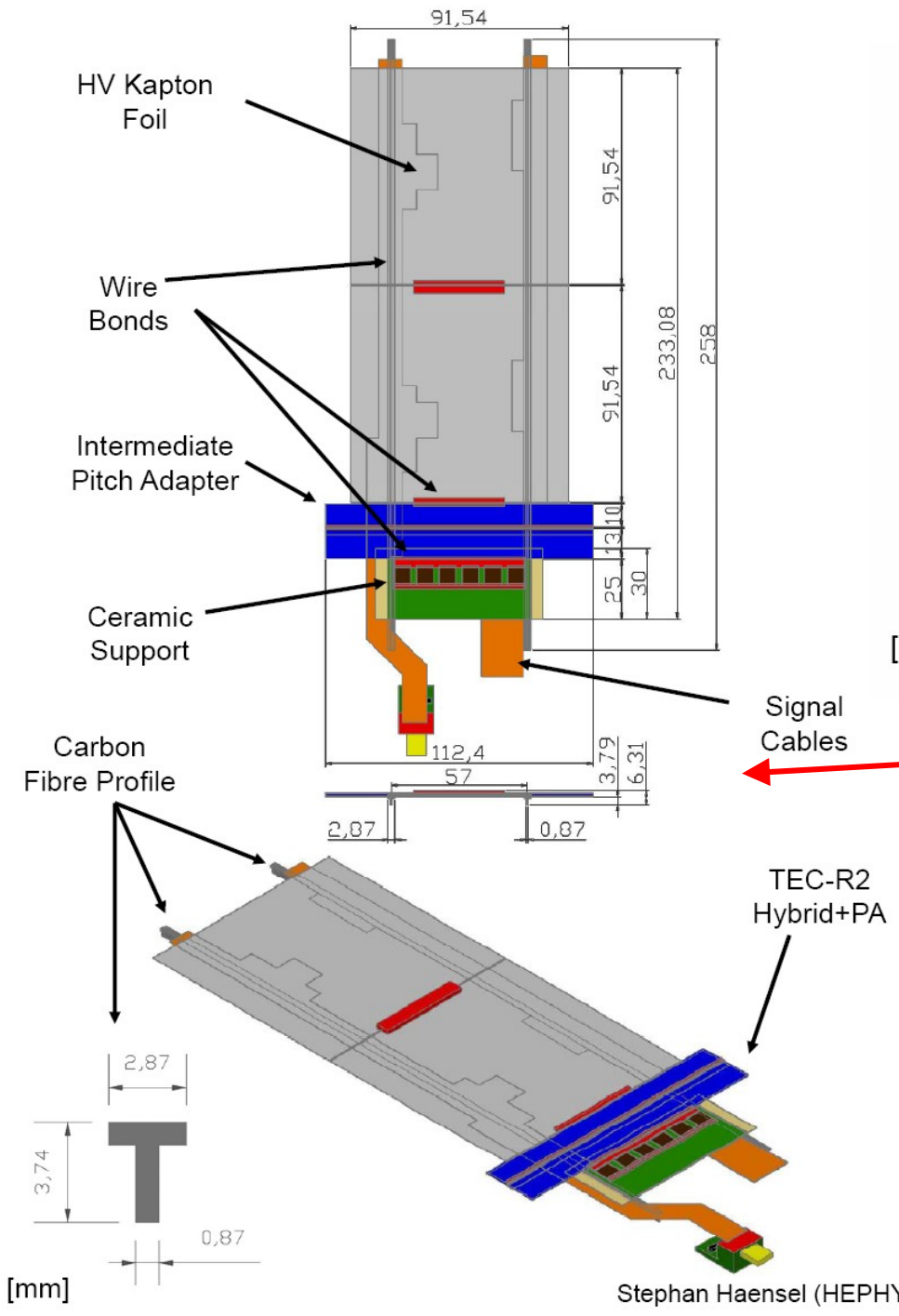
A big step forward has been made by the SiLC collaboration in order to design and build this overall ensemble. Apart from the small FTD disks, the SET, SIT and ETD large Silicon tracking components will be fabricated in the same way:

- A **unique sensor**, currently 10x10cm<sup>2</sup>, edgeless, planar, 200μm thick, 50 μm pitch will be the elementary tile of this ensemble.
- False double sided modules will be fabricated: **elementary modules**, and
- Assemble into **super-modules** which are modular elements of each main tracking component.
- The **related electronics and DAQ chain** is being developed consequently as well as the cabling.

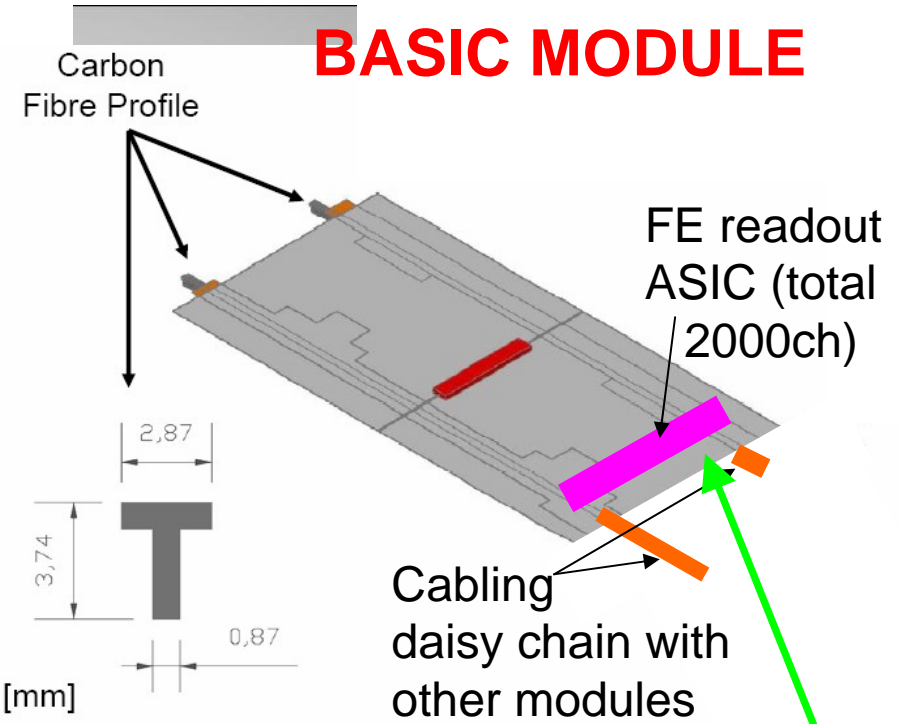
***This will represent a huge effort and need for further R&D and innovative ideas and novel technologies.***

The design studies are currently undergoing (LPNHE and Torino) in collaboration also with

M. Jore, P. Anduze , calorimetry , TPC and MDI teams and with the collaborative efforts of other SiLC teams. This effort is under development.



# BASIC MODULE



Present status (left) vs next step

- DSM-FE readout into one single unit:
- 8-256ch chips
- Total size: 8x0.5 cm<sup>2</sup>
- Thinned: 50μm
- Directly connected onto the sensor
- ⇒ No more pitch adapter,
- ⇒ No more hybrid board
- ⇒ Change in the cabling technology

# *THE SILICON EXTERNAL TRACKER: SET*

*Diego Gamba and Paolo Mereu (Torino)*

The mechanical structure of the SET is studied in details by the Torino team a real progress was made these last few months.

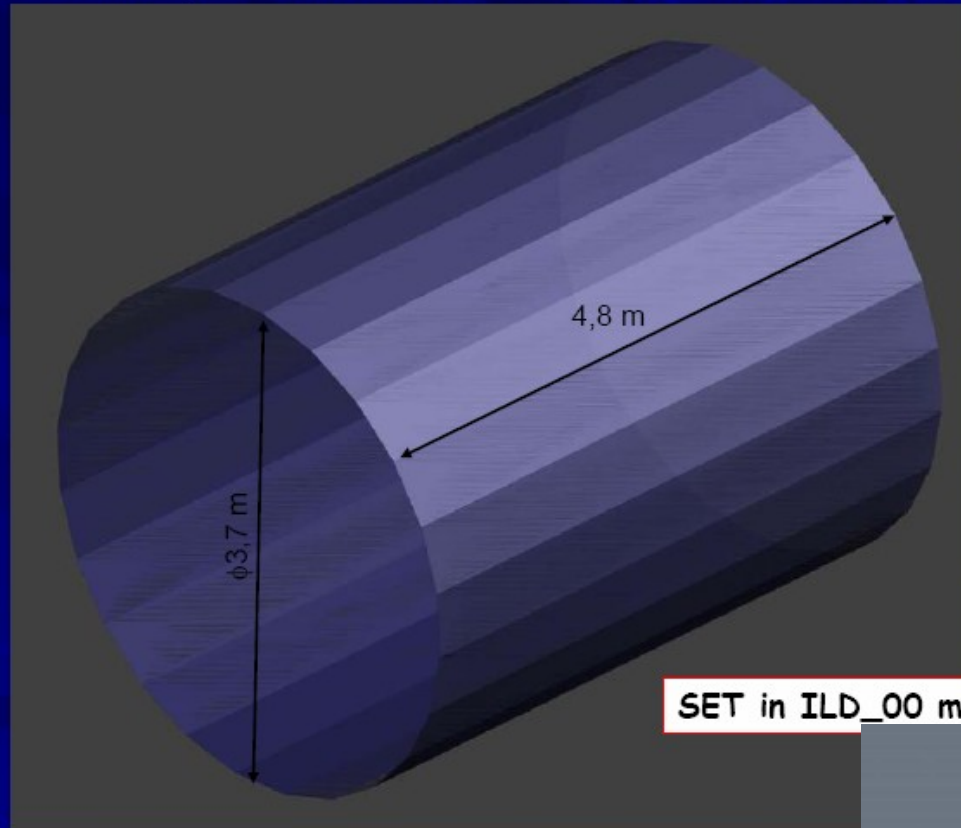
After a certain number of preliminary designs and studies, P. Mereu and D. Gamba have come to the following basic design:

The mechanical structure of the SET is made by 2 halves composed of 24 panels 2,4x0,48m. Each panel is independently fixed at both short sides to the outer surface of the TPC structure, thus avoiding an additional outer frame and therefore keeping the material budget at its minimum.

Static deflection with a payload of 1kg/sqm is given in the following slide.

Silicon detectors are fixed on the surface of each panel; details of this fixation have still to be defined....

## Preliminary Mechanical Structure of the SET Detector



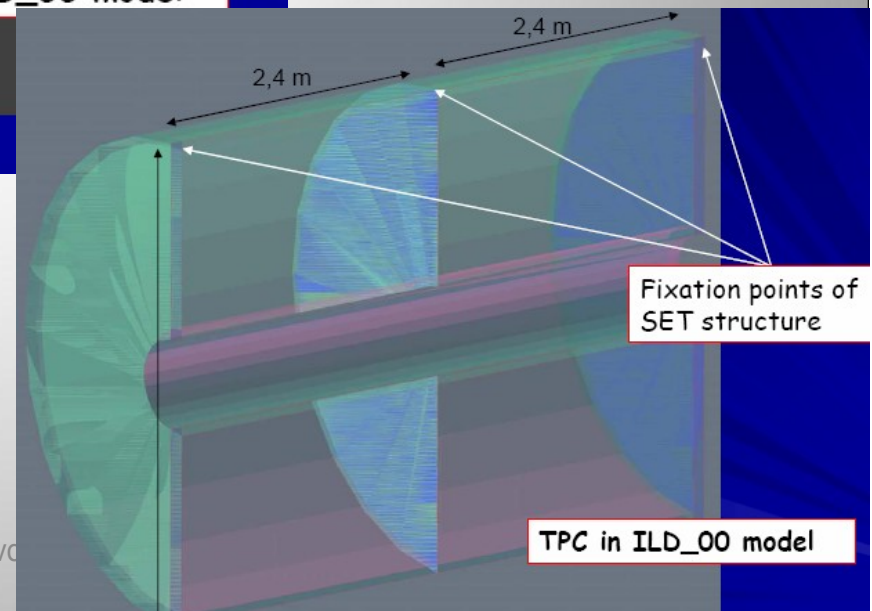
SET in ILD\_00 model

2 halves composed of  
24 panels 2,4x0,48m.  
*Torino will built such a  
panel as demonstrator  
and to study all related  
issues*

paolo.mereu@to.infn.it

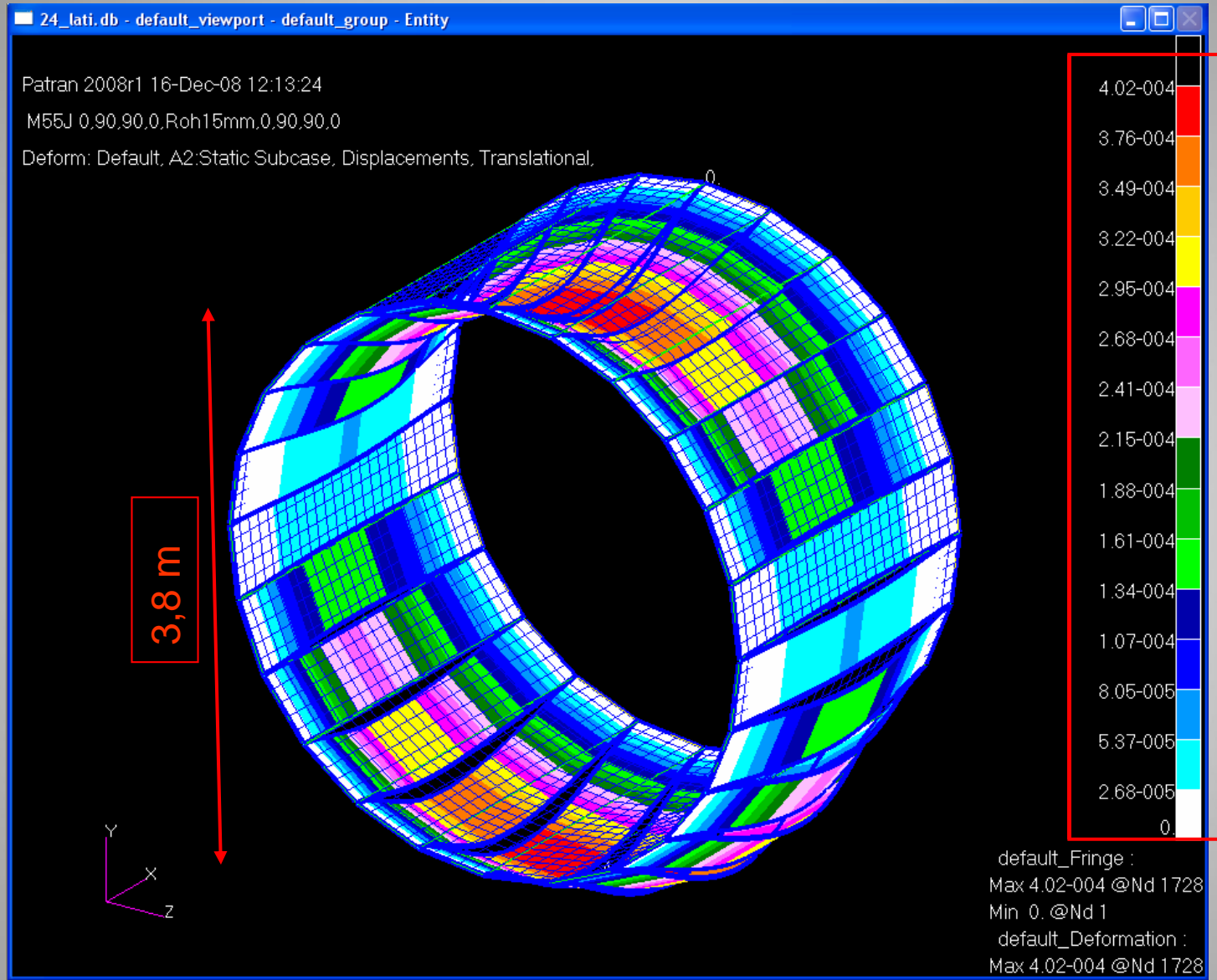
8th SILC Meeting – IFCA Santander  
17-19 December 2008

Each panel is independently fixed at both short  
sides to the outer surface of the TPC structure



TPC in ILD\_00 model

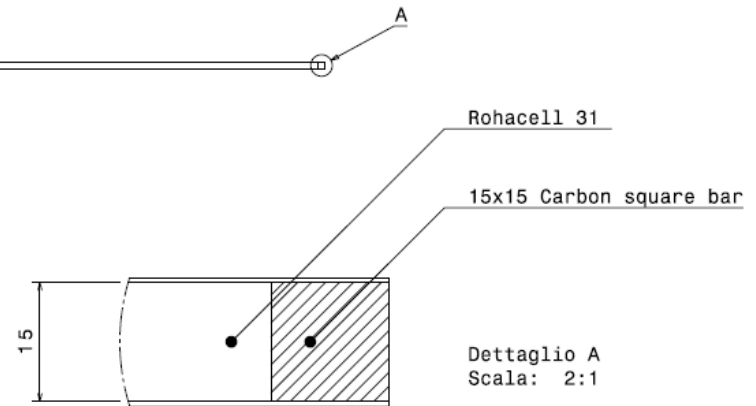




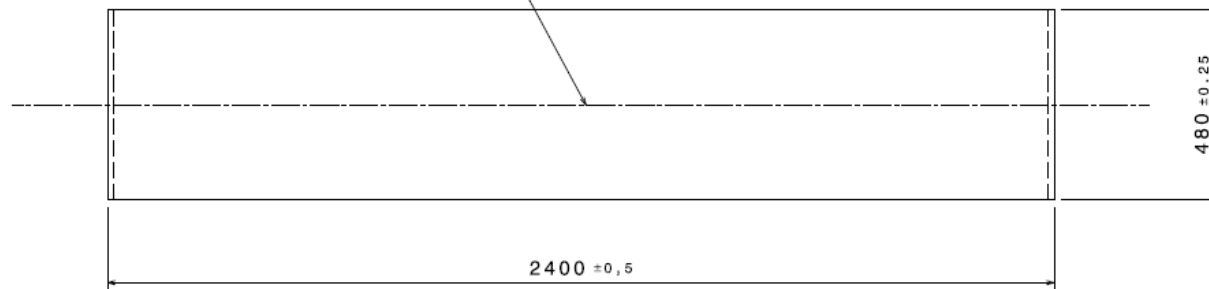
Courtesy of Paolo Mereu (Torino)



ply: Carbon Unidirectional Prepreg MTM49/M55J(6K)-150-36%RW  
Advanced Composites Group

Lay-up definition: [0/90/90/0/Roh31/0/90/90/0]



Ref. direction for lay-up definition



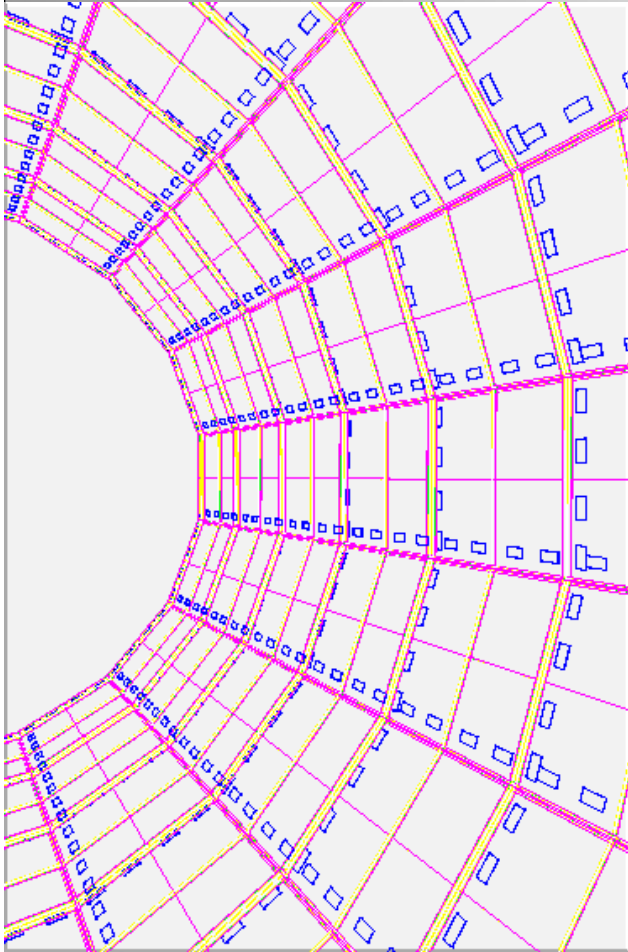
DENOMINAZIONE <i>Panel</i>		SUPERFICI 		SPIGOLI NON QUATRI SM 0.5x45°	
MATERIALE <i>Carbon UD - Rohacell31</i>		0,TA°		NOTE	
<b>SILICON EXTERNAL TRACKER</b>					
SCALA <i>1:10</i>		DATA <i>12/01/09</i>		GRADO DI PRECISIONE METRO UNI 5307-63	
DIS. <i>MEREU</i>		VISTO <i>MEREU</i>			
FORMATO <i>A3</i>		ESPERIMENTO <i>SILC</i>		DISEGNO N. <i>850/1</i>	
 ISTITUTO NAZIONALE di FISICA NUCLEARE Sezione di TORINO					

MODIFICHE	RIF.	DESCRIZIONE	DATA	FIRMA

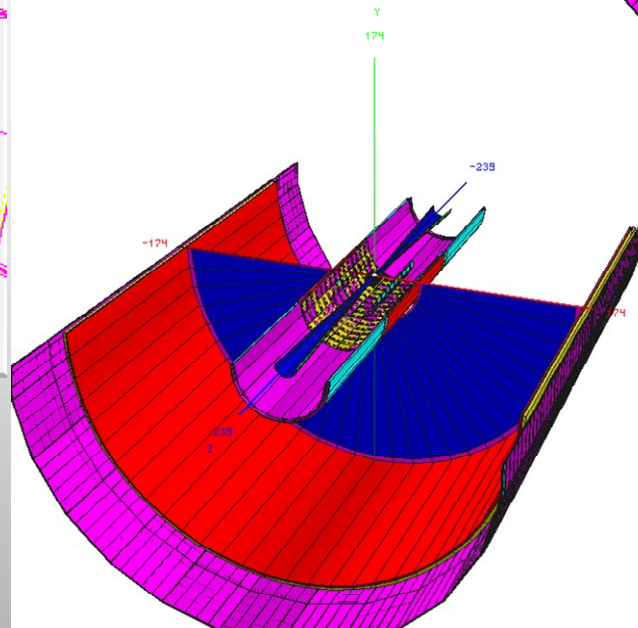
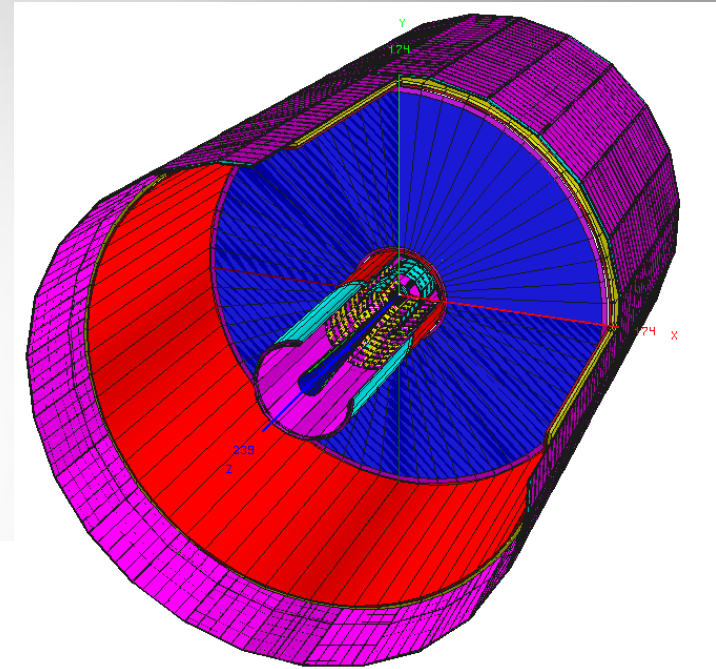
Material  
budget

- 8 Unidirectional Carbon-Epoxy Prepreg 0,15mm each: 0,45 %  $X_0$
- 15 mm-thick Rohacell31: 0,135 %  $X_0$
- each panel has 0,585 %  $X_0$

# SET: Study of design implementation with detailed simulation (A. Charpy, LPNHE)

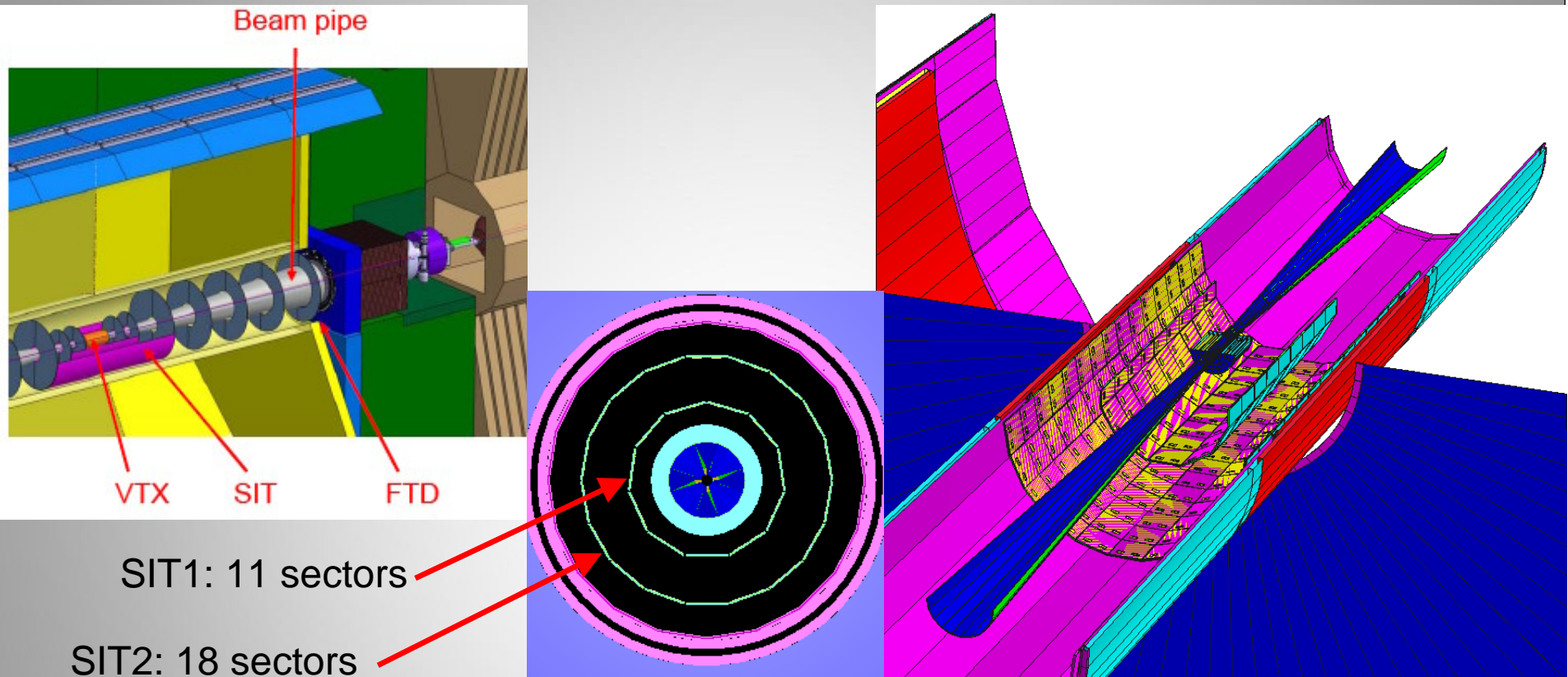


Presently SET is made of false double sided Silicon layers equipped with basic modules made of 5 sensors on both X,Y directions



ILCROOT simulation

# SIT: Silicon Internal Tracker

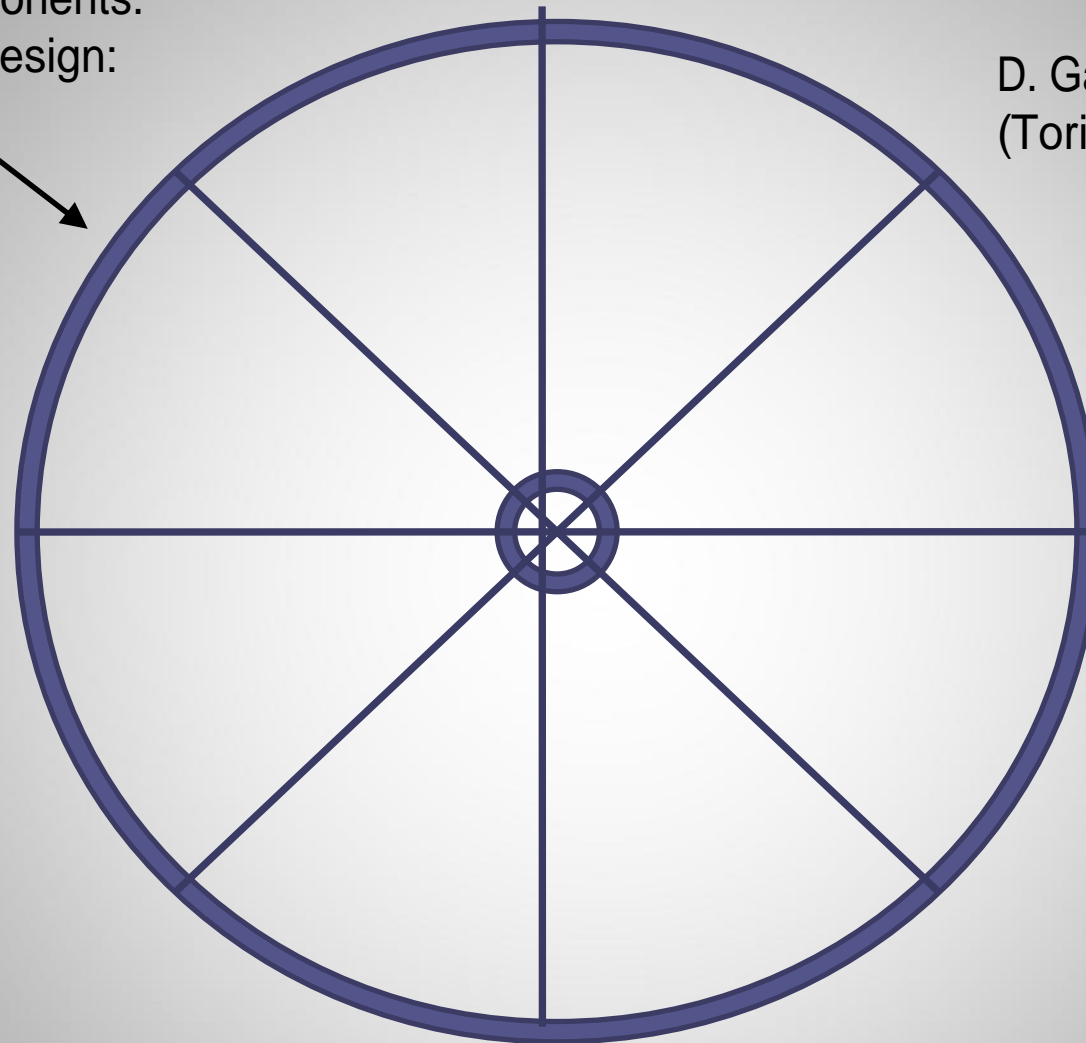


SIT is made of 2 false double sided X,Y layers (built in the same way than SET)  
The SIT design as described by A. Charpy with ILCROOT simulation includes:  
SIT1: 99 modules made each of a single sensor and 33 modules of 3 sensors each.  
SIT2: 270 modules made each of a single sensor and 90 modules of 3 sensors each.



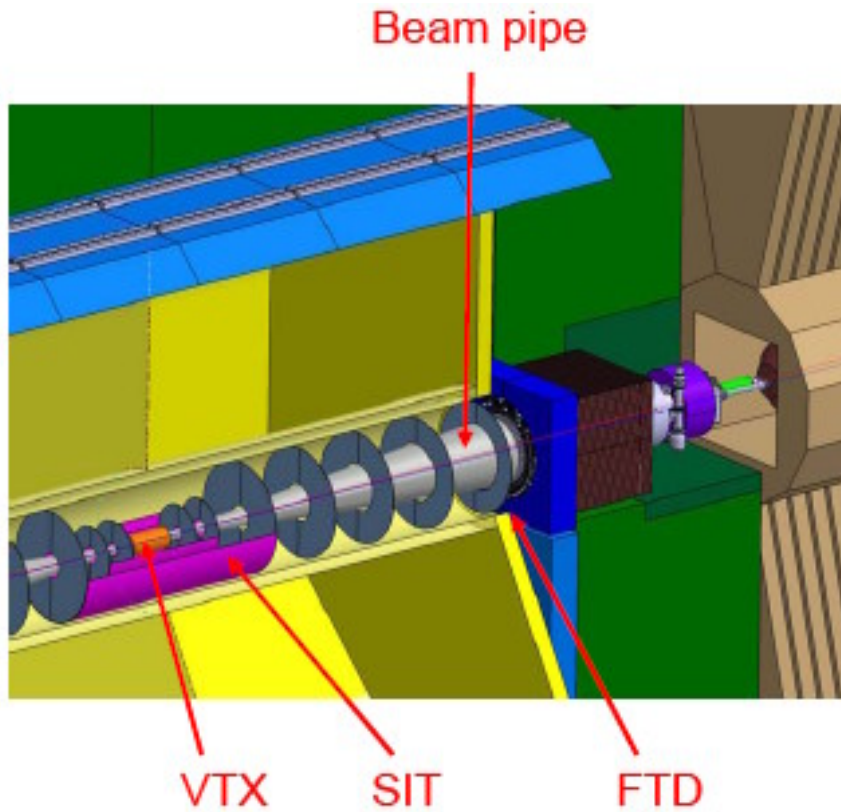
Material budget versus alignment: two options are studied for fixing the central barrel Silicon components.

Alternative design:



D. Gamba & P.Mereu  
(Torino U+INFN)

The “bicycle wheel” on each side of the barrel to fix both the SET and (SIT +FTD) envelope independently of the TPC and of other sub-detectors



## SUPPORT STRUCTURE OF SIT+FTD

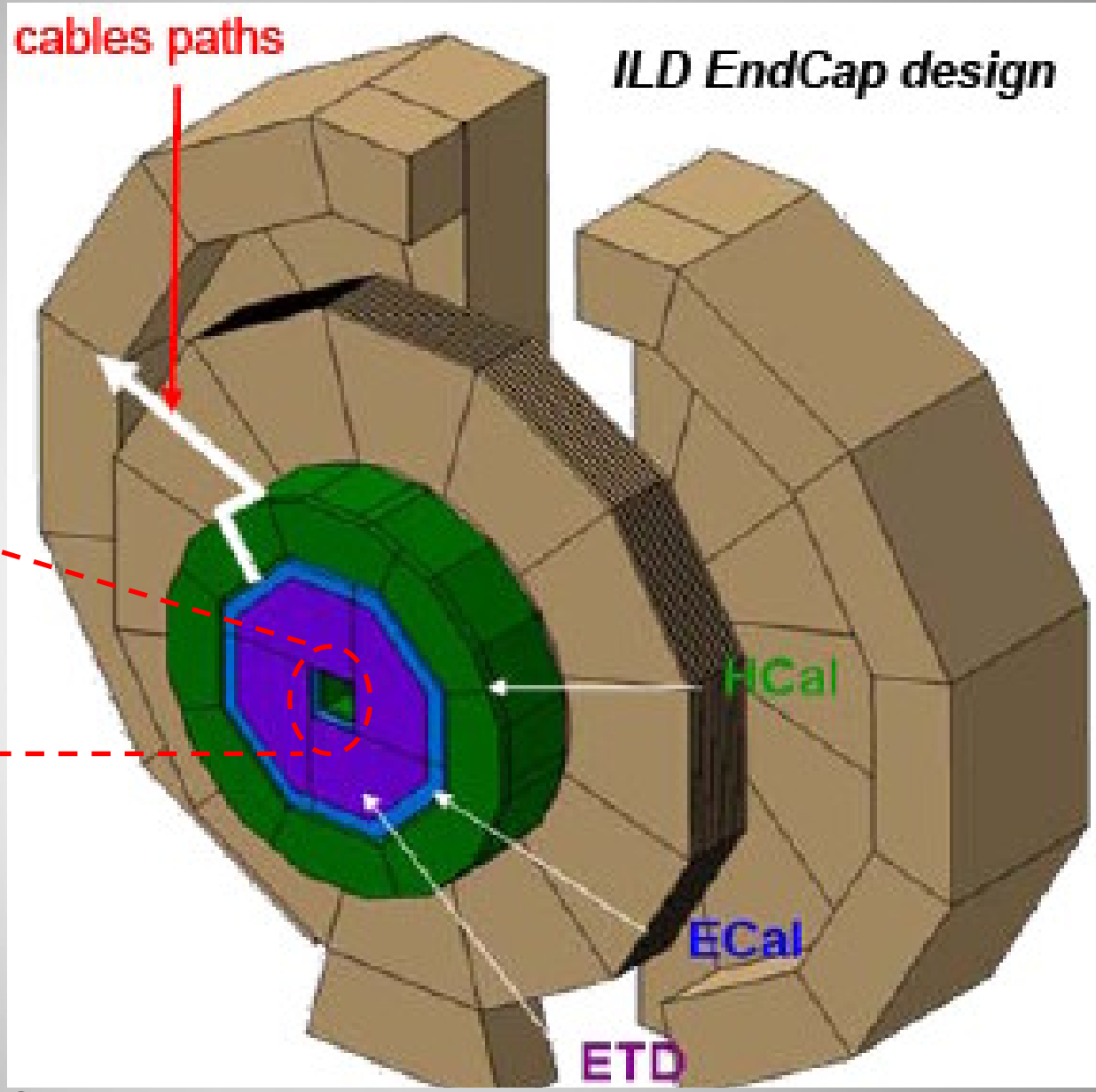
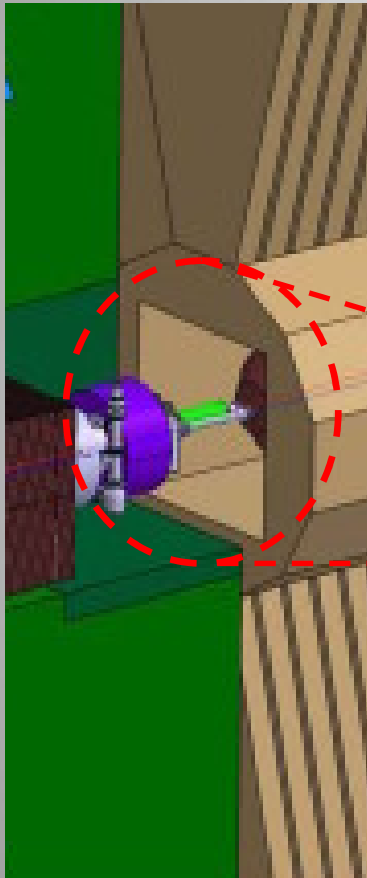
The VTX is fixed to the beam pipe and includes its own envelope  
 The SIT and FTD are fixed to the support structure which itself will be fixed to the TPC: middle plan and on the two edges (unless “bicycle wheel” solution)

There is for ALL the Silicon components only one cable path, i.e. the one along the beam pipe as sketched here below



Courtesy of M. Jore

ETD integration  
In the end cap  
and Very Forward  
calorimeter region

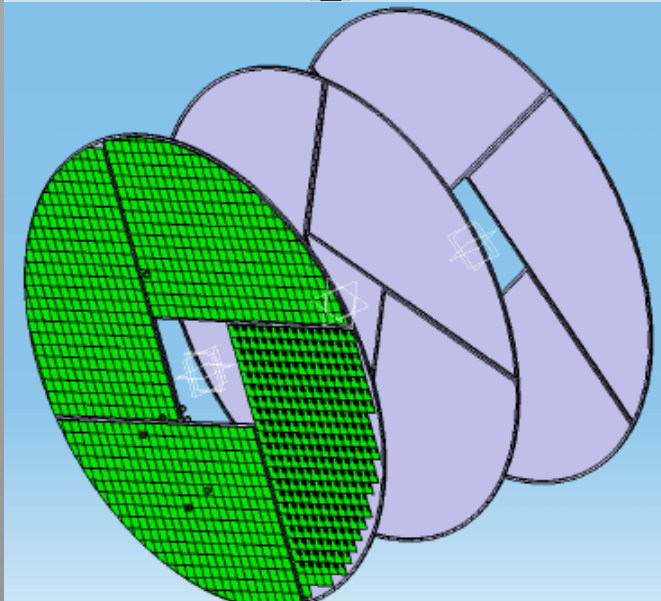
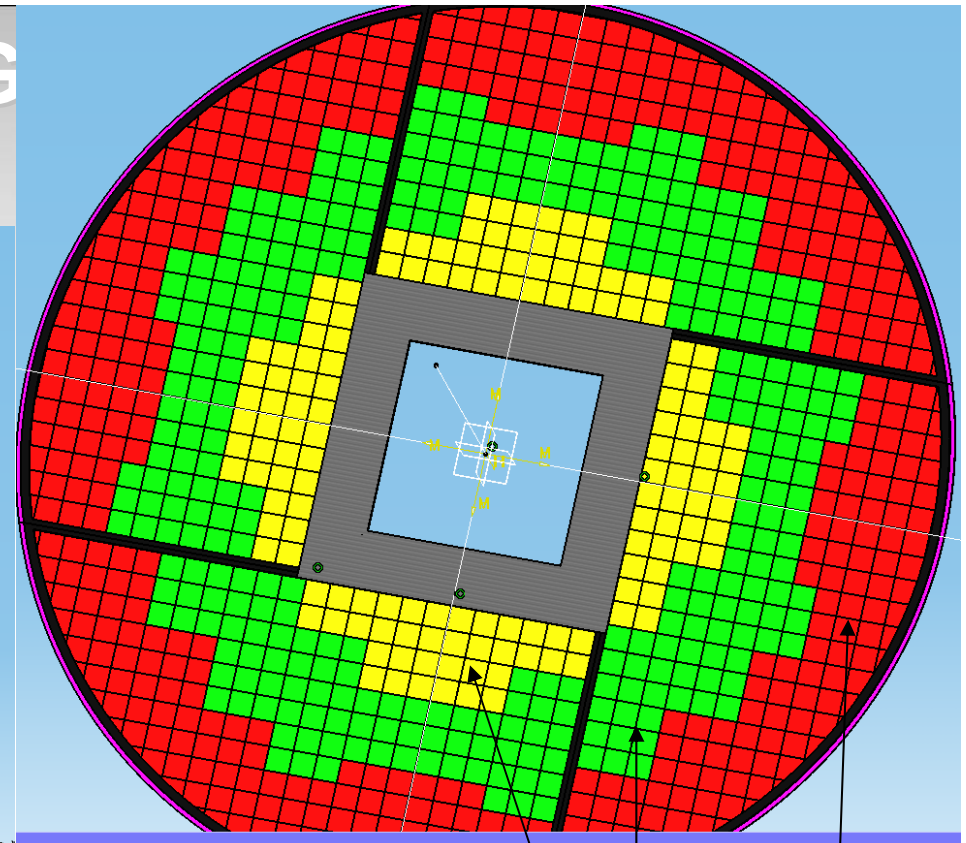
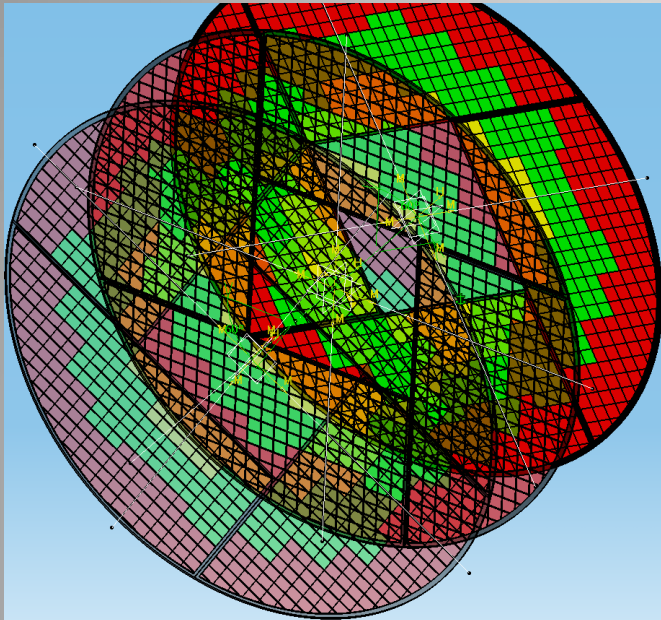


ETD is studied at LPNHE:  
A. Charpy, G. Daubard, P. Ghislain,  
D. Imbault, ASN.

Silicon ILD Tracking A. Savoy-Navarro

*Design courtesy of M. Jore*

# ETD: EXTERNAL TRACKING DETECTOR (LPNHE-Paris)

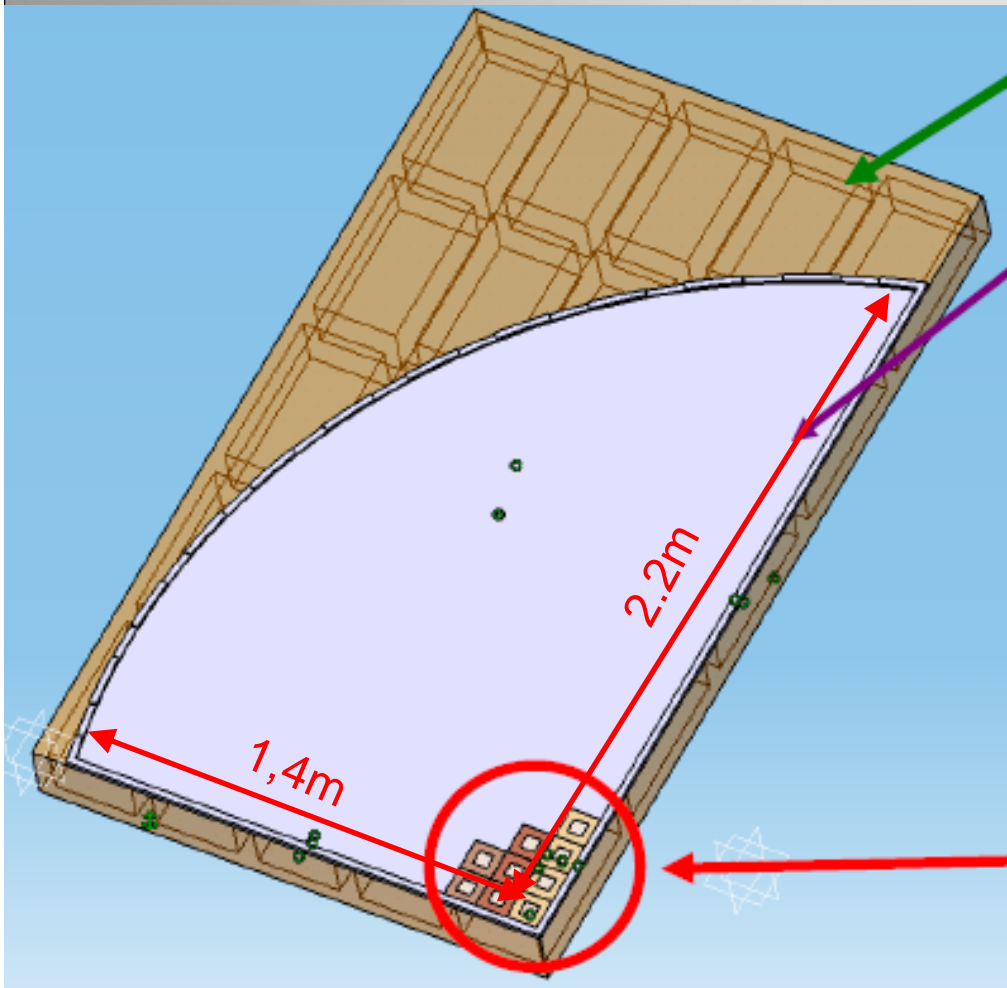


Each ETD is made of 3 single sided XUV plans made each of 4 parts.  
Each quadrant is made of modules of 2, 3 or eventually up to 4 sensors (optimization under study)  
In the center in order to recover from non squared frame when rotating by 60 degrees each plan a layer of pixels (grey) will be implemented. This pixel area will be just surrounding the square hole of the V.F.

(under study) Savoy-Navarro



# Manufacturing the ETD components (LPNHE Paris)



Quadrant support to mount the overall structure with high spatial precision

Quadrant support structure made in the same way as the SET support structure (C Fiber/Rohacell foam/C fiber). *Paris will build such a quadrant and the related quadrant mounting support as demonstrator and to study all related issues (precise positioning, module integration, cabling, how to proceed to manipulate this large piece from horizontal to vertical, tooling to be developed etc..)*

Modules with 2, 3 or eventually up to 4 sensors (to be studied)

Within this present design the ETDs are made each of  $4 \times 3 = 12$  thus total of 24 quadrants

## *The S components in numbers: preliminary*

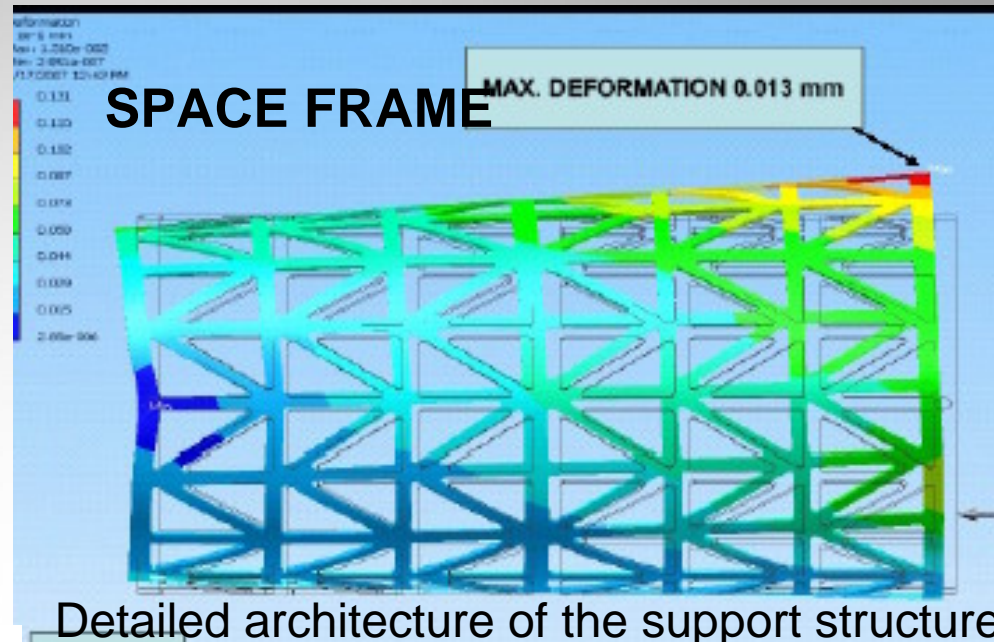
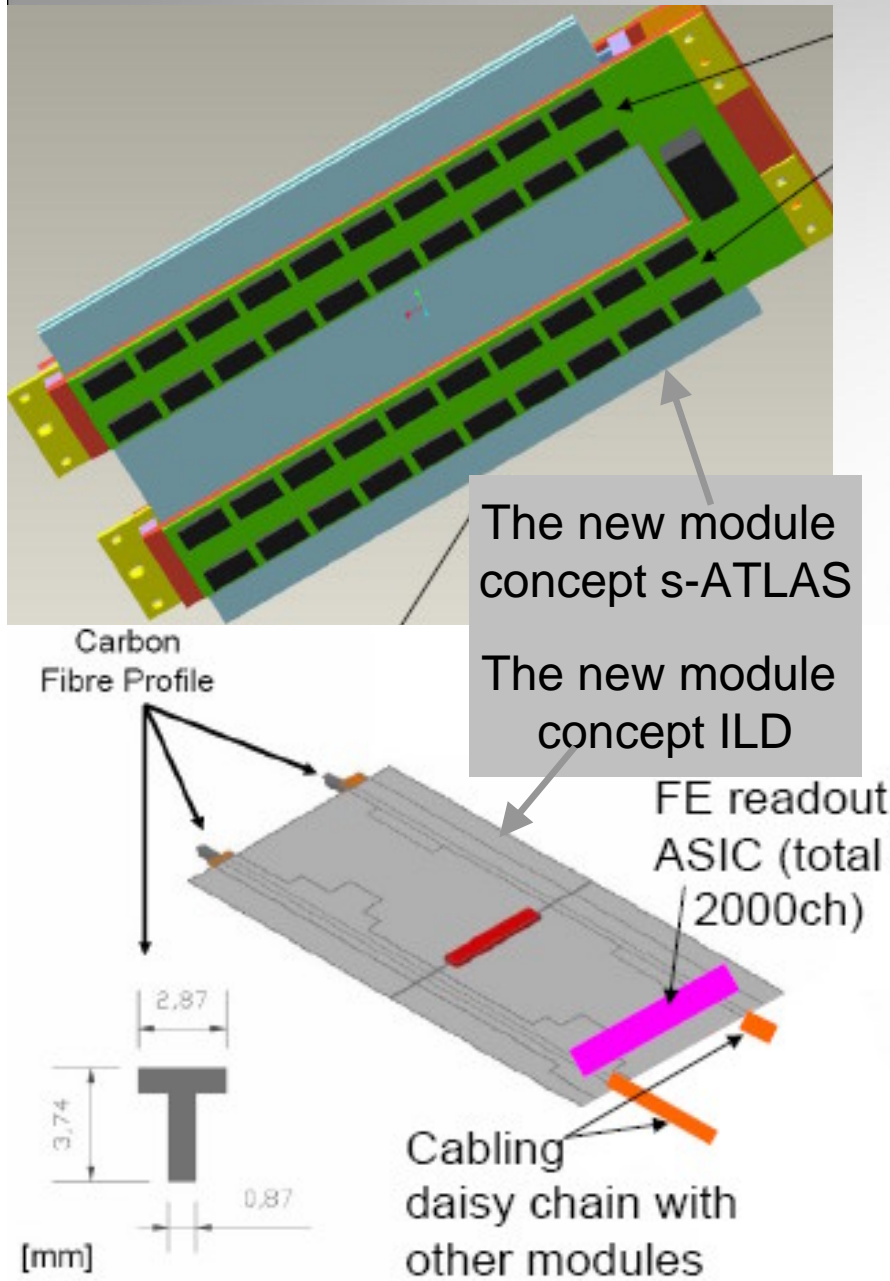
Component	Layer #	# modules	# sensors/ module	# channels	Total surface m2
SIT1	1 <sup>st</sup> layer	33	3	66.000	0.9
	2 <sup>nd</sup> layer	99	1	198.000	0.9
SIT2	1 <sup>st</sup> layer	90	3	180.000	2.7
	2 <sup>nd</sup> layer	270	1	540.000	2.7
SET	1 <sup>st</sup> layer	1260	5	2.520.000	55.2
	2 <sup>nd</sup> layer	1260	5	2.520.000	55.2
ETD_F	X or U or V	82/quad =328/layer =984/ETD	2 or 3 or possibly 4	2.000.000	30
ETD_B	idem	idem	idem	idem	30

**TOTAL: 1.000.000(SIT)+5.000.000(SET)+4.000.000(ETDs)≈10M channels**

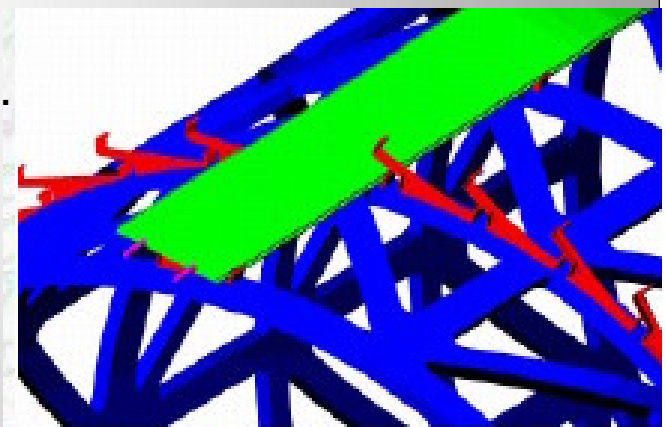
**7 (SIT) + 110 (SET) + 60 (ETDs) ≈ 180 m2 (present SiD: 135m2)**

**500 (SIT) + 2500 (SET) + 2000 (ETDs) ≈ 5000 modules with unique size sensor**

# SIT, SET, ETD: Detailed work on structure & modules started



SuperModule to be built by Torino (SET) & Paris(ETD) for studying all pending issues



*s-ATLAS designs by courtesy of Ph. Allport (synergy with LC)*

## Rapport de stage

Etude thermique du système de refroidissement d'un détecteur de traces en silicium



Stage effectué au sein du LPNHE de paris  
(Laboratoire de Physique Nucléaire et de Hautes Energies)  
Du 5 décembre 2005 au 24 février 2006

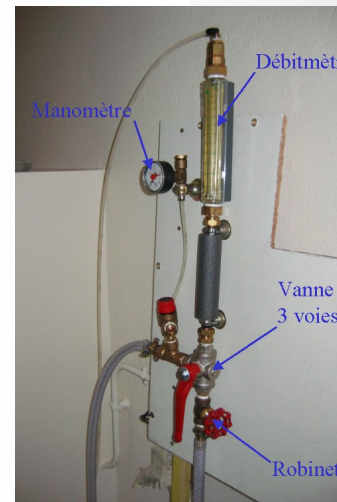
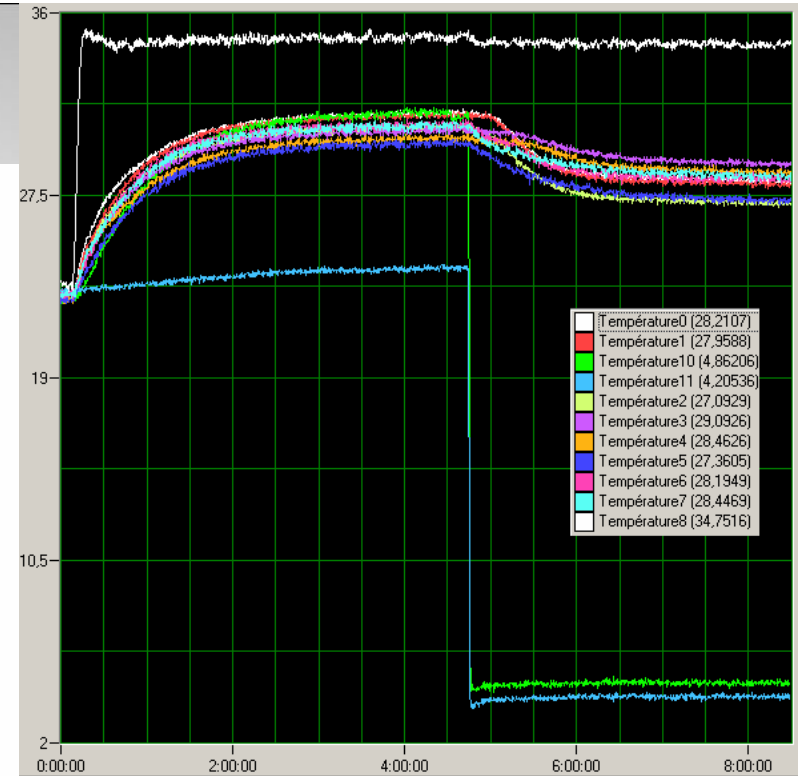
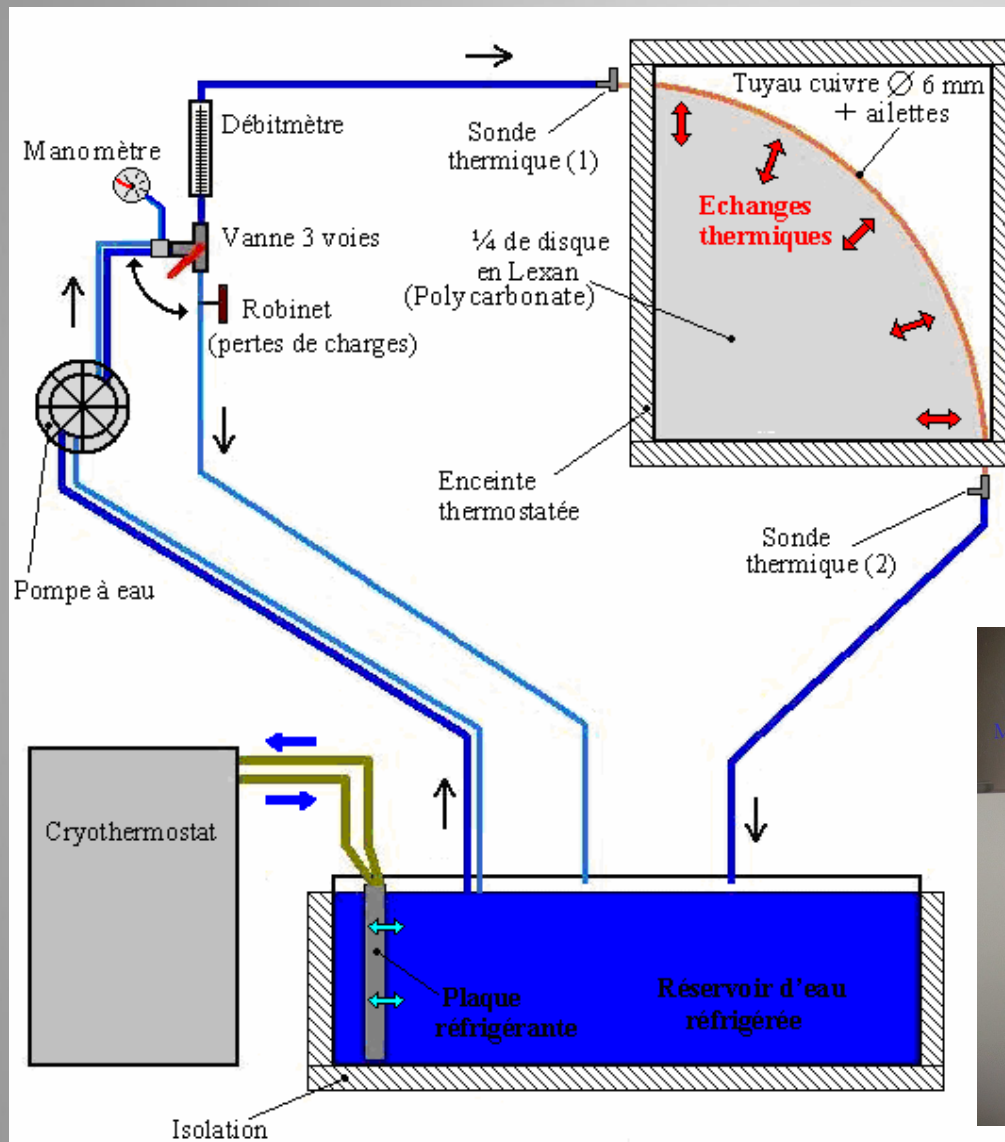
Stagiaire : Guillaume Davée  
Maître de stage : Guillaume Daubard  
Enseignant responsable : Jay Amrit

# Cooling Studies conducted at LPNHE Here for the ETD

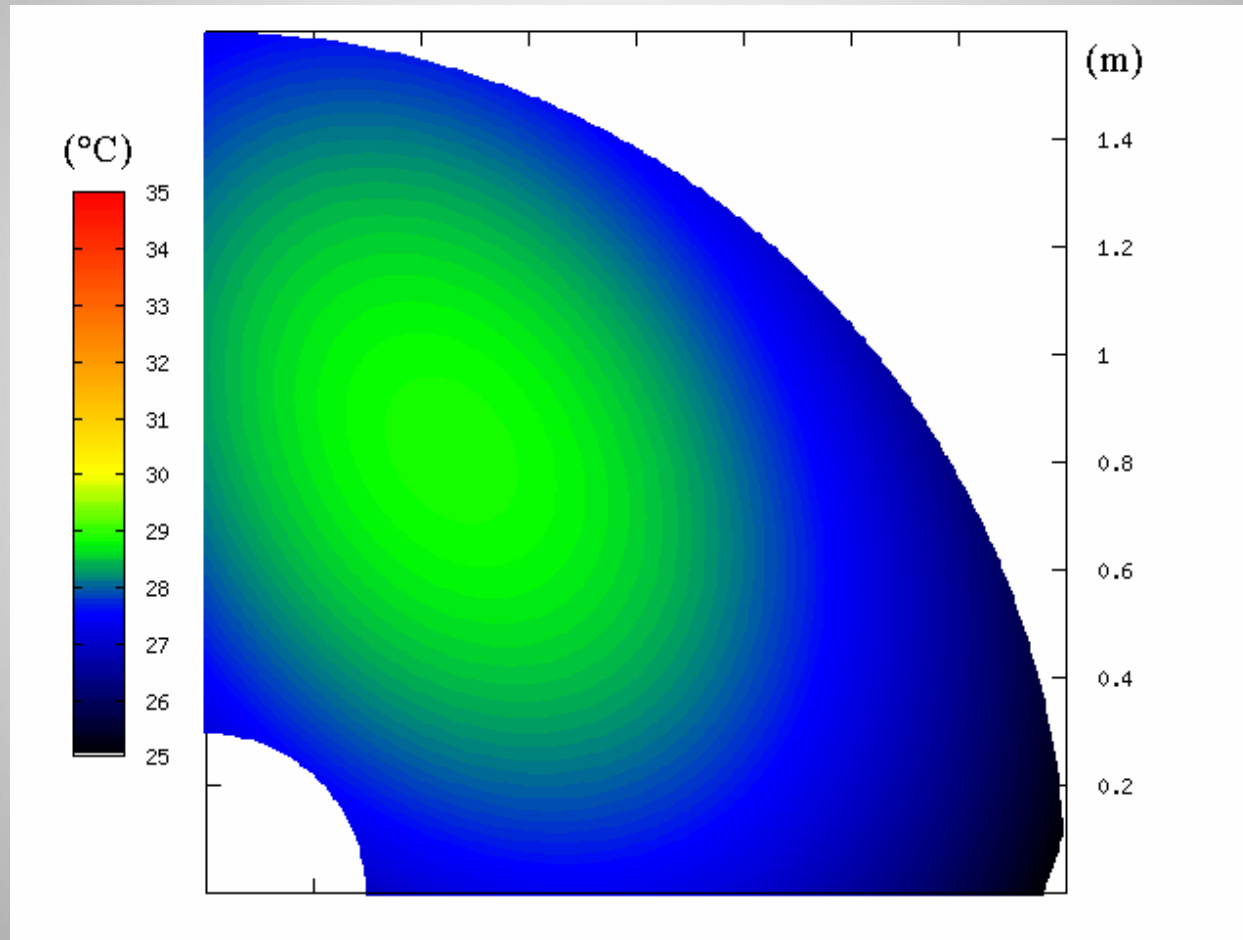
Current FE electronics dissipate  
**Max 1mWatt/channel.**  
In addition power cycling is  
Included in the last version:  
SiTR\_130-88



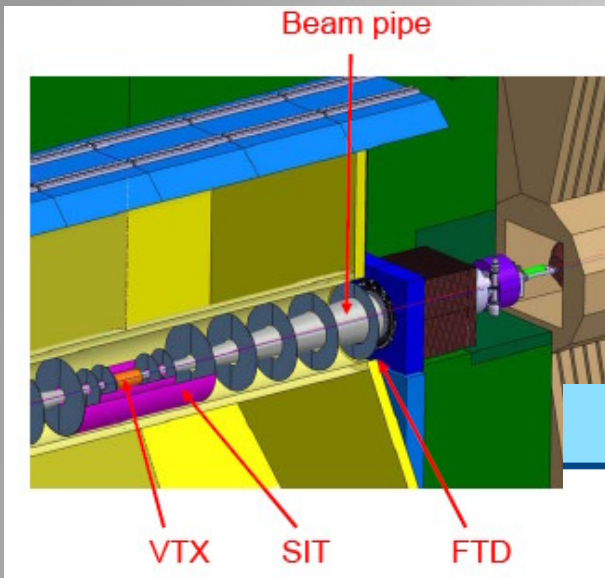
# COOLING TEST SET-UP at THE LAB



# Result of cooling test on ETD quadrant prototype (LPNHE-Paris)



# FTD disks: the Spanish team (IFCA, IFC, USC)



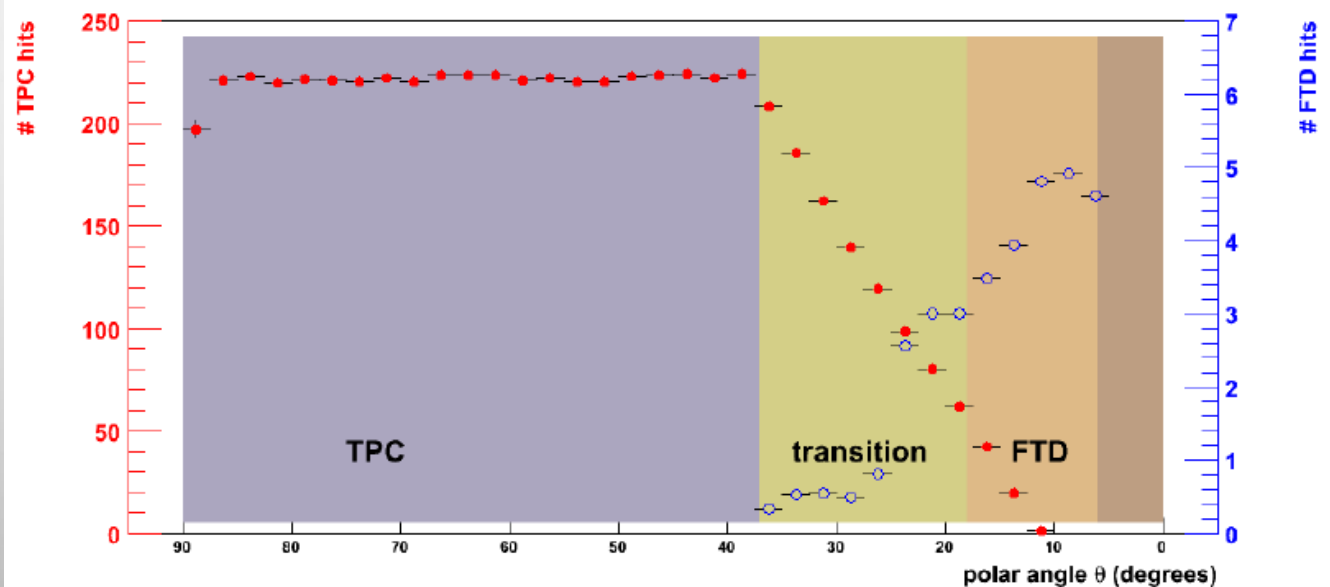
They are performing a complete the FTD disks: detailed simulation studies; development of pixels (first 3 disks): strip detectors (last 4 disks in false DS small angle stereo petals); alignment system (IFCA) including developing new sensors (IMB-CNM), plus engineering to build these disks.

## The challenges of forward tracking

Hermetic coverage of full polar angle range

*Marcel Vos*

TPC gradually loses coverage below 38 degrees



# The FTD 4-7 petals design: IFCA+IFC

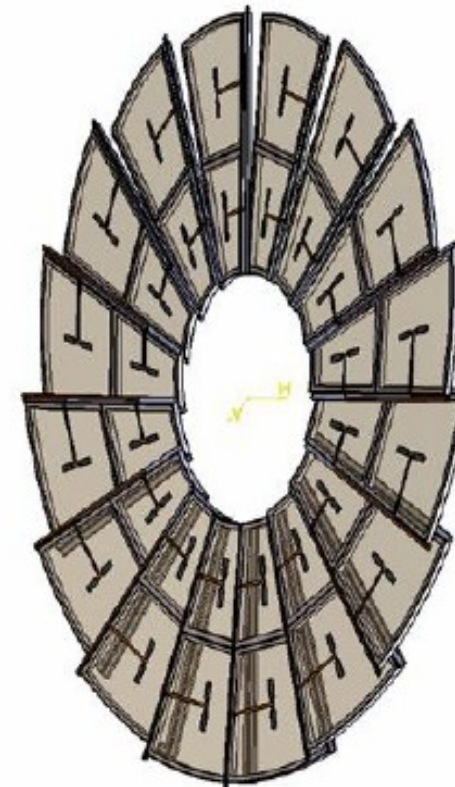
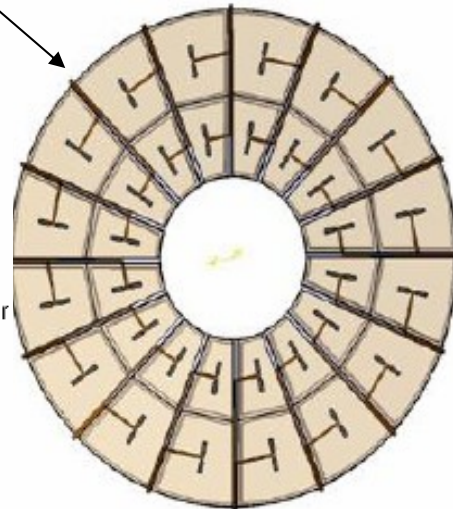
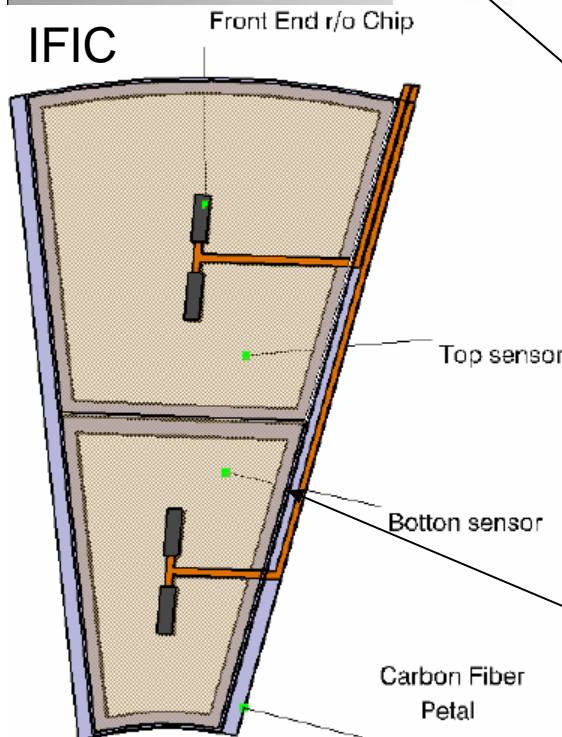
16-petals false double-sided small stereo-angle

## FTD 4: 16 PETALS GEOMETRY

*David Moya (IFCA)*



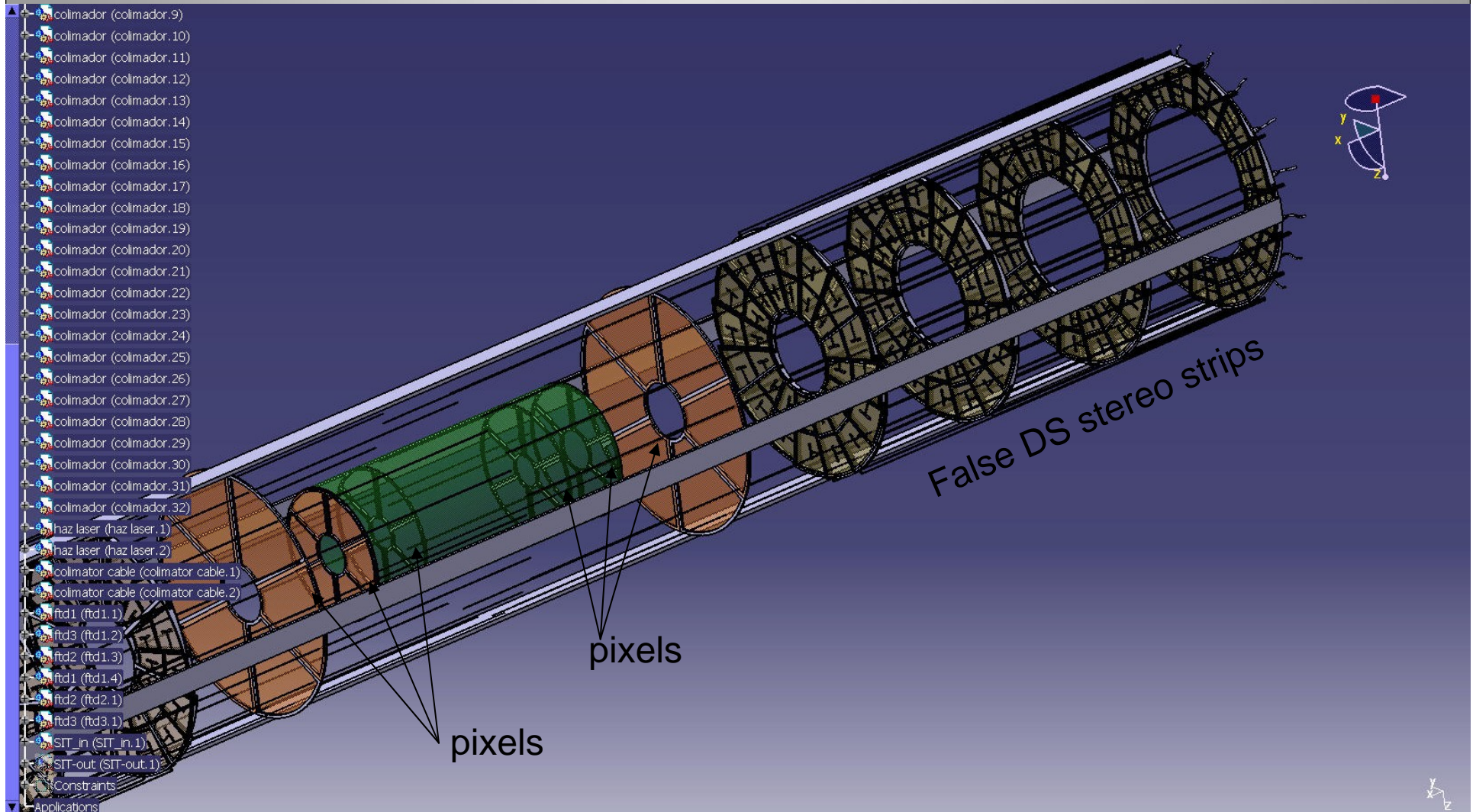
- Applying the design to all the petals of the FTD
- In the right picture we can see the rotation of the petal respect to the beam pipe axis
- In the bottom picture we can see the 4th FTD perpendicular projection to the beam pipe.



*Petal designed by IFIC derived from ATLAS Si End Cap tracker but with new SiLC electronics concept*



# The FTD system *(The spanish team)*



# Study of the hits density in FTD

The idea is to analyse the hits density in FTD disks dividing them in sections (petals).

*Carmen Iglesias,*

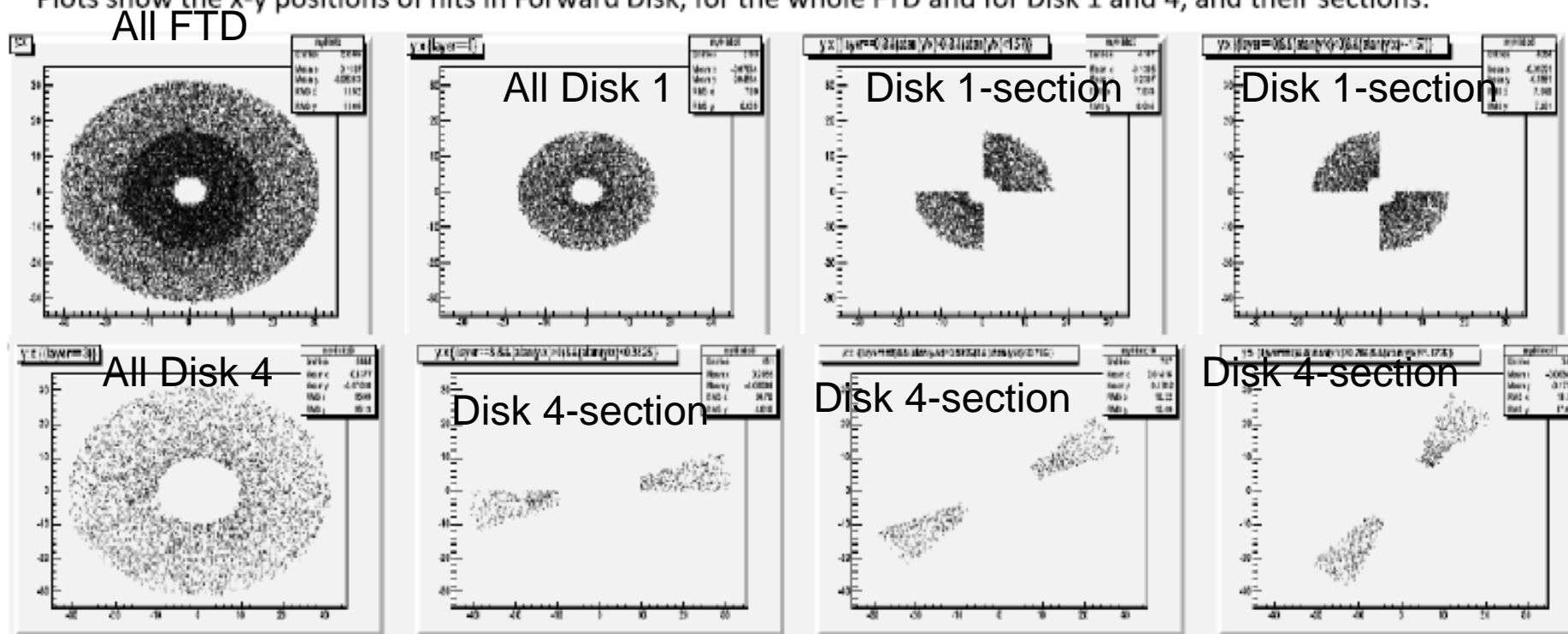
In principle, Disks 1-3 in 4 sections and Disks 4-7 in 16 sections (similar to IFCA design), but...

*Bernardo Adeva: USC*

	R_inner (mm)	R_outer(mm)	Z(mm)	Area_disk(cm <sup>2</sup> )	Area_Section(cm <sup>2</sup> )
FTD_1	39	164	220	797.17	199.29 (1/4)
FTD_2	40.6308	164	371.309	793.09	198.27 (1/4)
FTD_3	70.1393	308	644.906	3318.57	<b>829.64 (1/4) o 207.41 (1/16)</b>
FTD_4	100.298	309	1046.12	2683.58	167.72 (1/16)
FTD_5	130.372	309	1447.33	2466.07	154.12 (1/16)
FTD_6	160.447	309	1848.54	2190.87	136.92(1/16)
FTD_7	190.54	309	2250	1859.05	116.19 (1/16)

....It's seems better divide the 3 Disk in 16 sections instead of only 4.

Plots show the x-y positions of hits in Forward Disk, for the whole FTD and for Disk 1 and 4, and their sections:



- Role of Silicon tracking in ILD
- Silicon system and performances
- Calibrations
- Construction and integration issues
- **Dedicated R&D on advanced technologies**
- Concluding remarks, pending issues

In order to make adequately the elementary modules a series of related R&Ds are undertaken on:

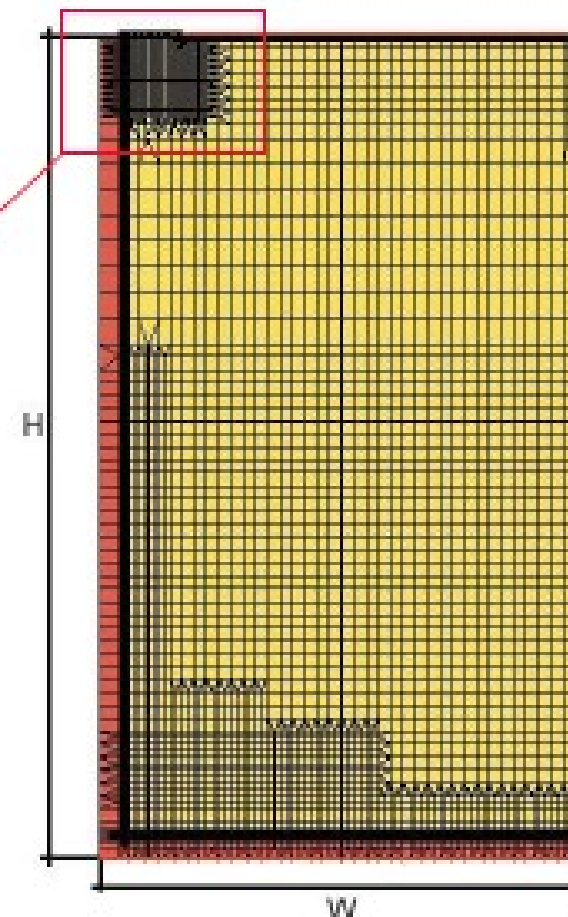
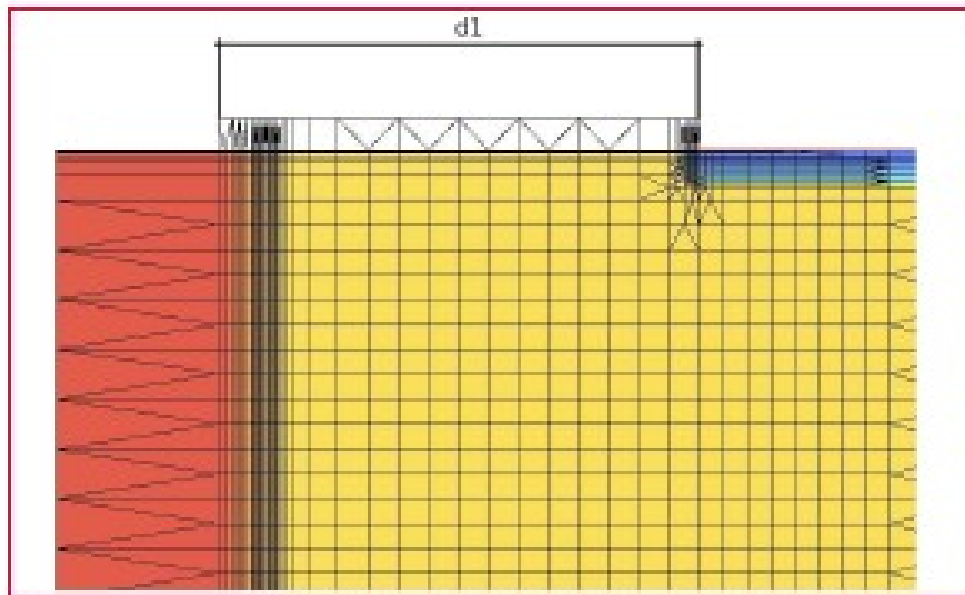
- Novel sensors: edgeless planar microstrip sensors  
Go to 3D planar microstrips (?)  
Purpose: go to thinner, lower voltage sensors, lower power dissipation, radhard
- VDSM FE readout electronics
- Direct connection of electronics on sensor:  
bump bonding (underway with present ASIC)  
3D interconnection
- Cabling and transmission of data out of the detector
- A lot of challenges also on the mechanics side in order to have 1) the lightest possible modules  
2) the lightest possible structure





# Simulation of planar detectors with active edge

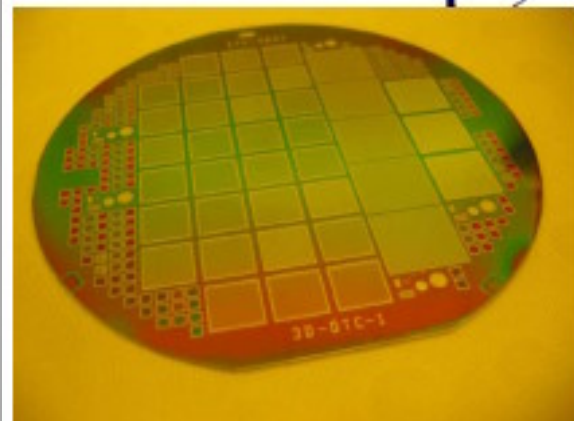
ISE-TCAD simulations aimed at investigating detector operation (mainly breakdown problems)



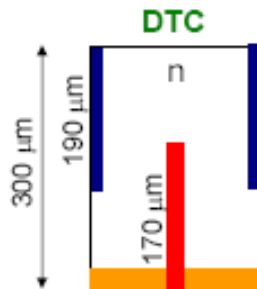


## 3D-DTC-1 batch

- N-type substrate
- (Mostly) microstrip detectors  
*useful to ease characterization and investigate process yield*



Column overlap not optimized:  
about 60um



Courtesy G. F. Dalla Betta

Silicon ILD T



## Fabrication

- 2 batches under fabrication at FBK

1) Recycle of 3D-DTC-2: n-on-p, 200- $\mu\text{m}$  thick substrate, non-passing-through columns (180  $\mu\text{m}$ )

Currently at 2<sup>nd</sup> DRIE etching, to be completed by 02/09.

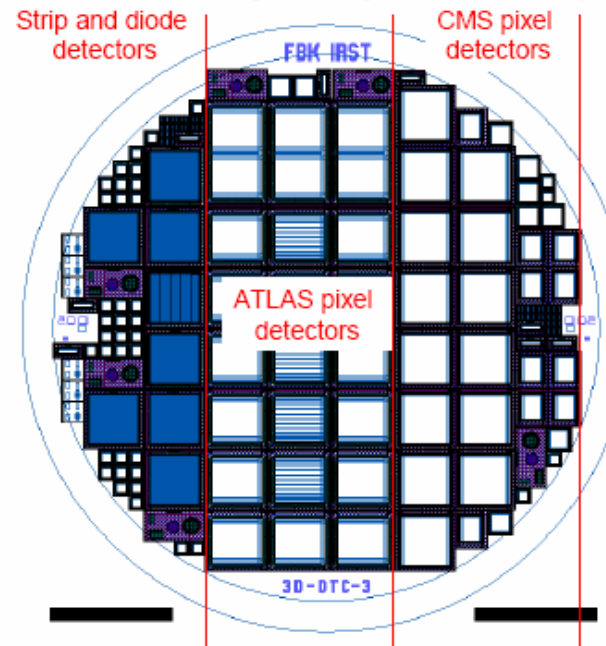
2) 3D-DTC-3: n-on-p, 250- $\mu\text{m}$  thick substrate, full 3D detectors (passing-through) columns.

New double-sided process defined, no need for support wafer, also suitable for dual read-out pixel/strip.

Just started, to be completed by 04/09



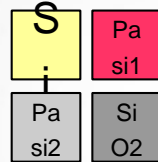
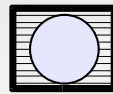
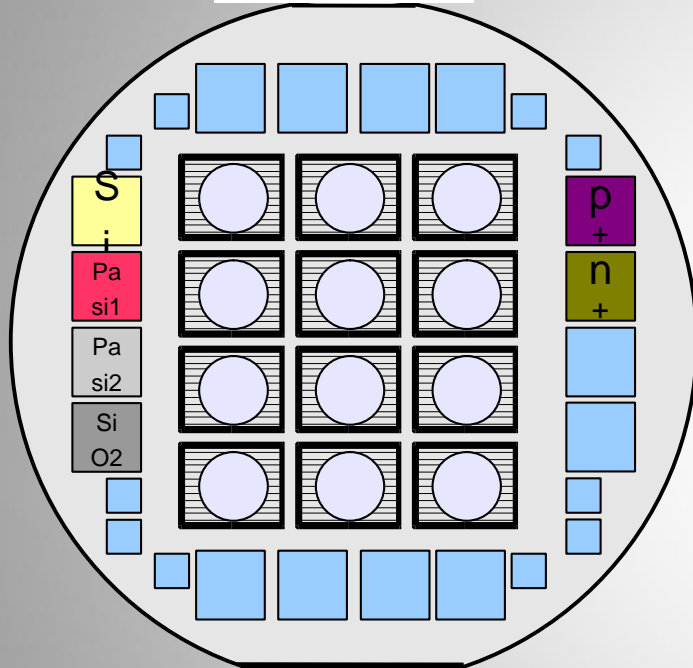
## New layout (3D-DTC-3)



# NOVEL SENSORS SPECIAL FOR ALIGNMENT

IMB-CNM (Barcelona) is producing the first sensor prototypes with multigeometry and optimum thickness.

(Pictorial view)



Alignment sensor  $1.5 \times 1.28 \text{ cm}^2$  (256 strips  $\approx$  2 Alibava)  
(Likely to become  $1.5 \times 1.5 \text{ cm}^2$  with guard rings...)

Al hole in the back  $\approx 1 \text{ cm}$

Strip width is the same along the full strip

Slightly larger area to mount on PCB

Optical test structure (TS)

**No Al in the back**

1 per layer of material

Ellipsometry?

Electrical TS

See poster by M. Dragicevic at INSTR08, Novosibirsk

**All SiLC TS are valid here**

Pitch =  $50 \mu\text{m}$

Metal width = 3, 5, 10, 15  $\mu\text{m}$

Granted by GICSERV08

AC sensors

– Al strips

(3 wafers)

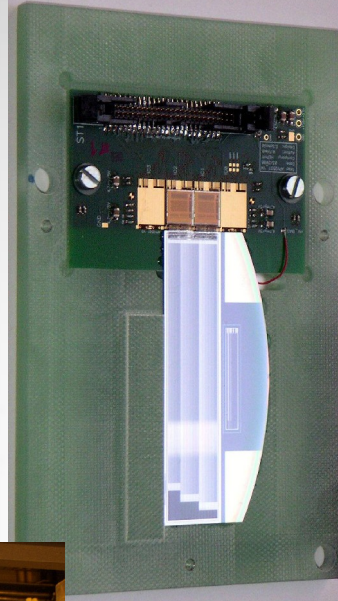
– Al strips & Al backside

(1 wafer)

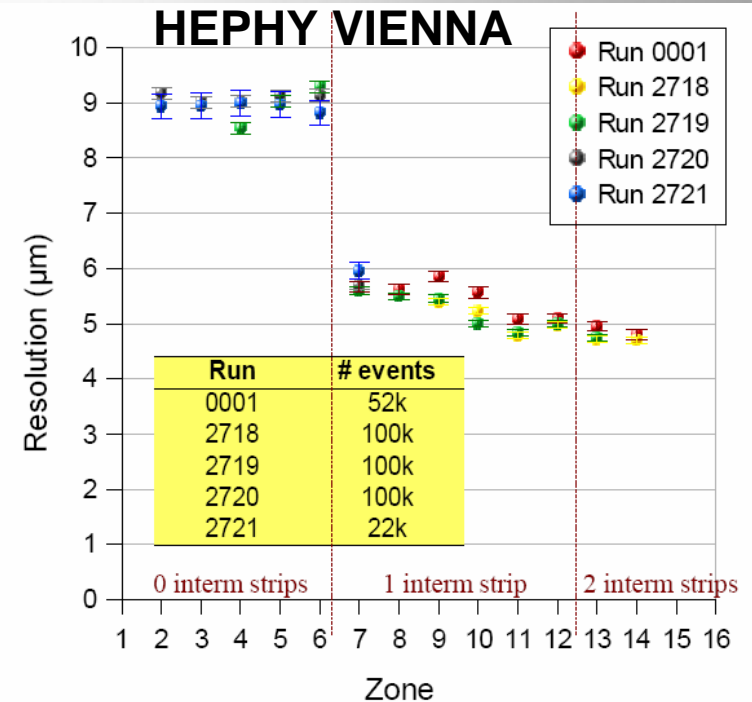
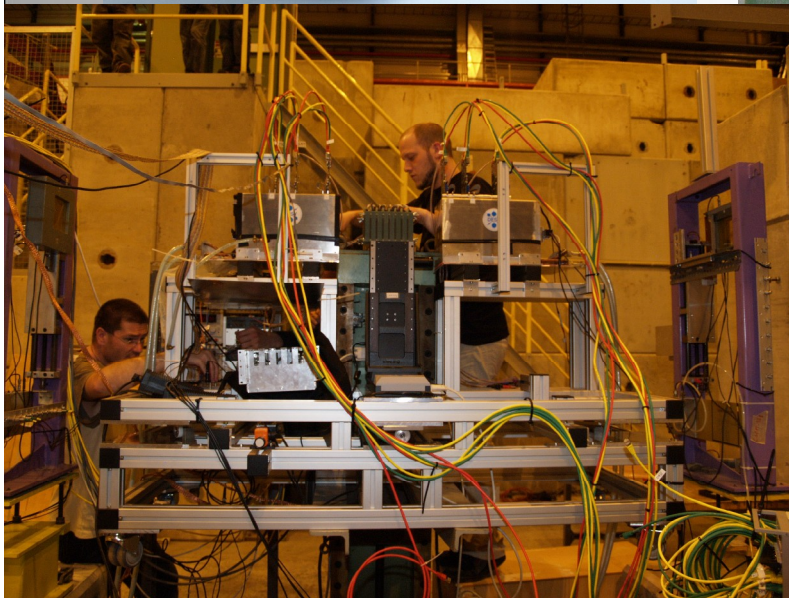
*Slide from Marcos Fernandez Garcia (IFCA)*

# Ongoing R&D activities: example test bench to measure the sensor detailed performances

HEPHY VIENNA



New series of tests this year at CERN with novel sensors from IMB-CNM and from Poland with wire bonded chips. Expertise and well experienced teams = asset



(CU Prague)

Silicon ILD Tracking A. Savoy-Navarro

Th. Bergauer, S. Haensel, M. Krammer et al.(HEPHY)



# Concluding remarks

- Based on the SLC R&D activities and the contribution of a large number of its members, a detailed design of the Silicon tracking system for ILD is achieved.
- The construction and integration issues are addressed in a more and more realistic way (supported by more and more detailed performance simulation studies),
- As well as the needed advanced technology to be pursued for achieving the requested performances.
- It also opened a new phase of larger scale prototypes (realistic) and of even more aggressive R&D challenges especially in sensors, electronics and mechanical issues
- The SLC collaboration is dedicating a large effort to achieve these goals, very demanding in person-power, high expertise and financial support.

With many thanks to all the SLC collaborators



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