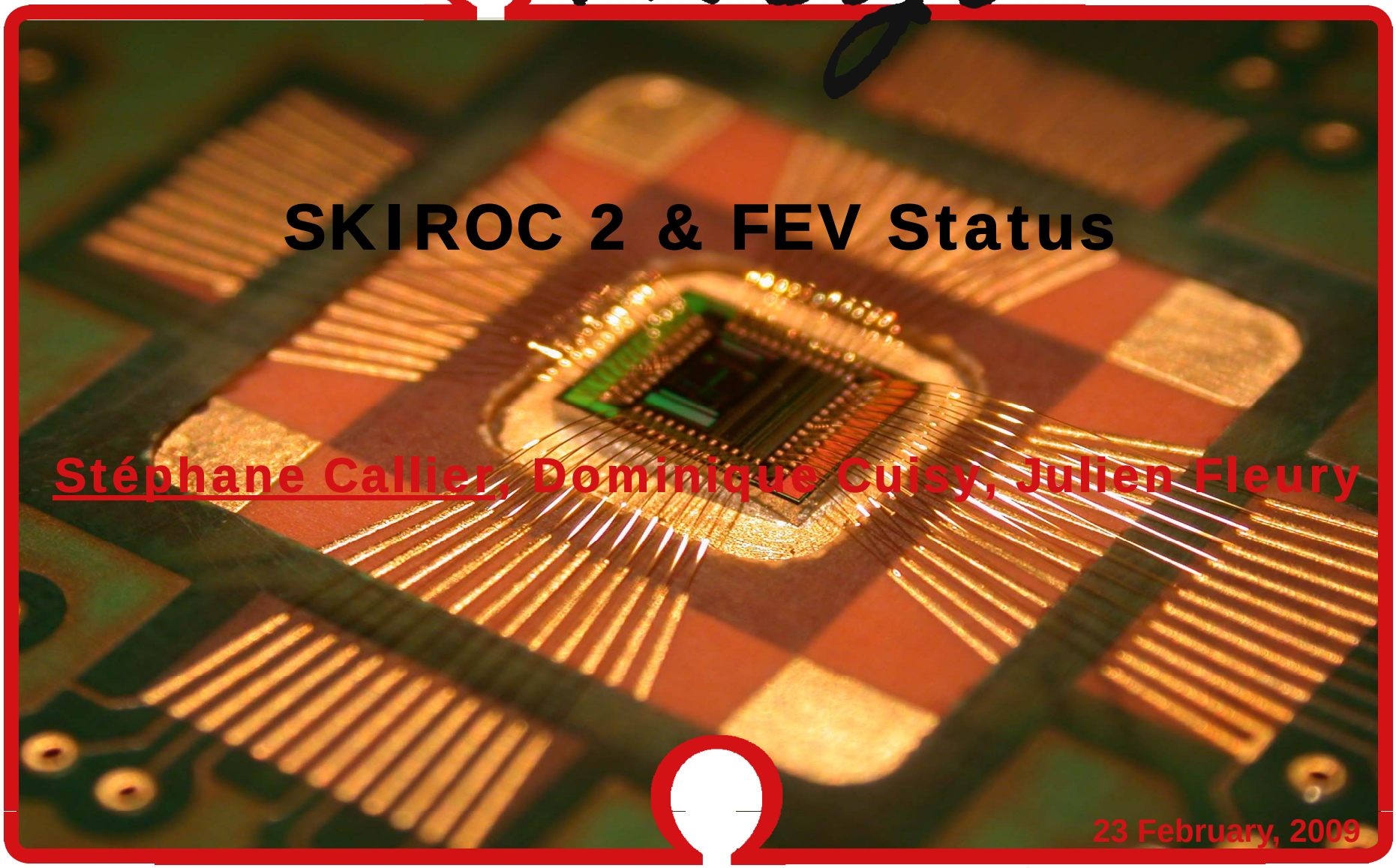
IN2P3 CSNSM LAL LPNHE IPN Orsay

Omega



SKIROC 2 & FEV Status

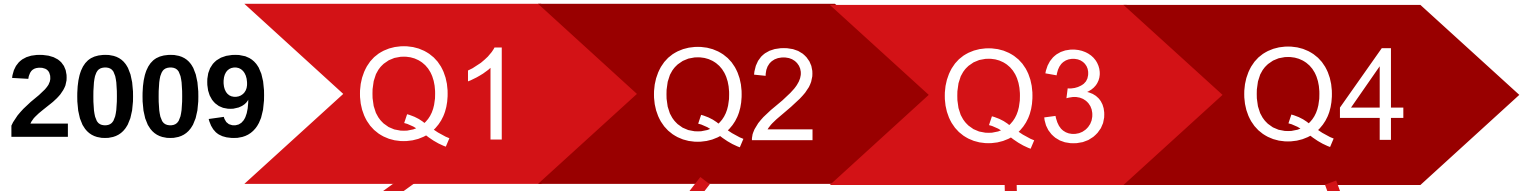
Stéphane Callier, Dominique Cuisy, Julien Fleury

23 February, 2009

Orsay MicroElectronics Group Associated

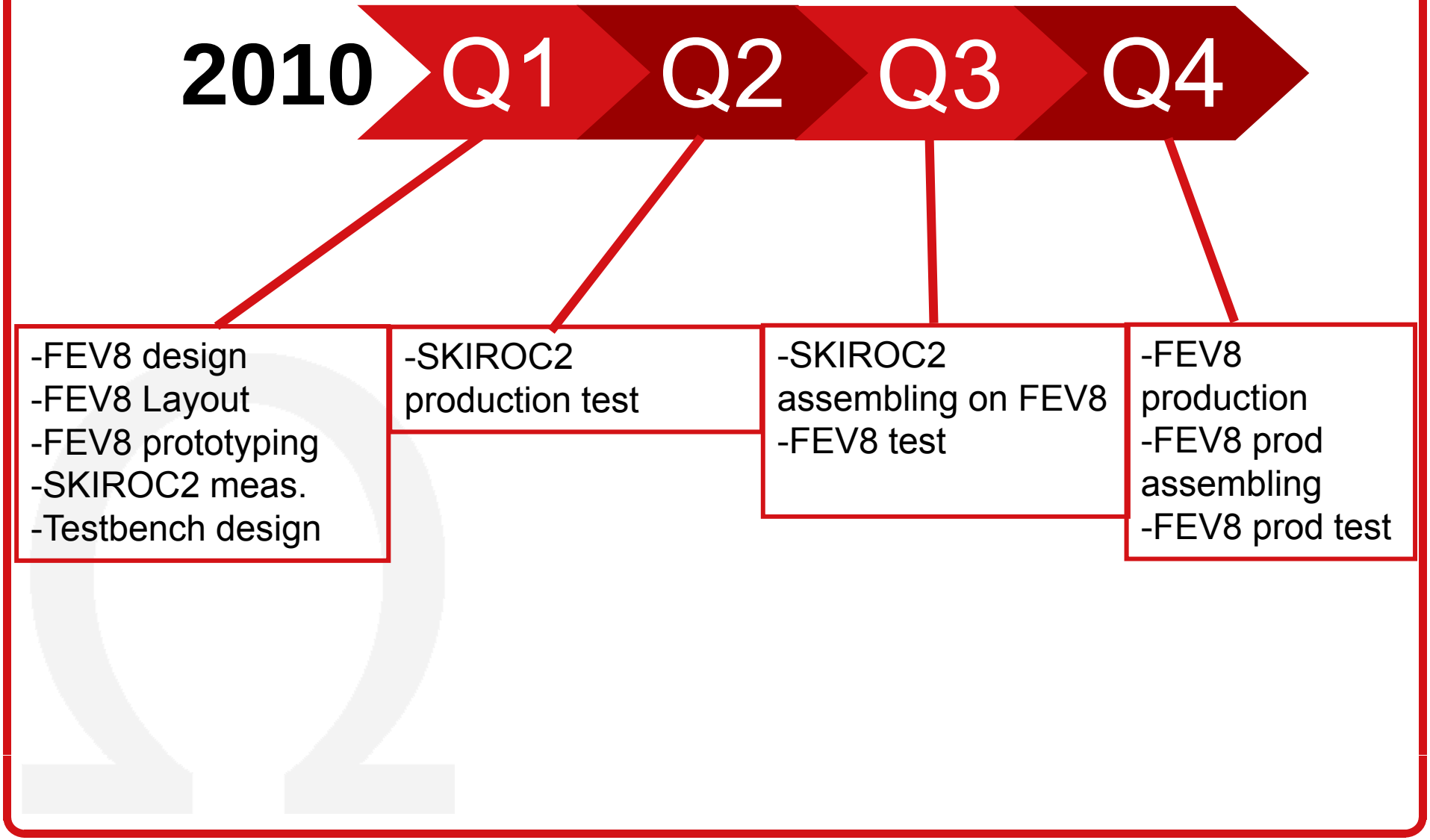
ASIC Schedule
SKIROC 2

Schedule 2009



Q1	Q2	Q3	Q4
-FEV7 design -FEV7 Layout -FEV7 prototyping -SPIROC in SKIROC mode meas. -SKIROC2 design -Schematic -Simulation	-FEV7 bonding -FEV7 debug & first test -SPIROC in SKIROC mode meas. -SKIROC2 design -Layout -Floorplaning	-PRODUCTION ROC Chips -Prototyping test bench design -Production test bench studies & design - FEV7 test	-Prototyping test of SKIROC2 -FEV7 test

Schedule 2010



Funding request

2009 → Prototyping

PCB R&D and fabrication

-Prototyping of FEV7 in 3 different companies to ensure (?) success of fab.

PCB assembly (prototype)

-SKIROC2 characterization test (dicing, packaging, testboard, etc.)

Needed before assembly

-SPIROC assembling on FEV7, process validation, machining

Can be done by CERN to save money, official agreement needed

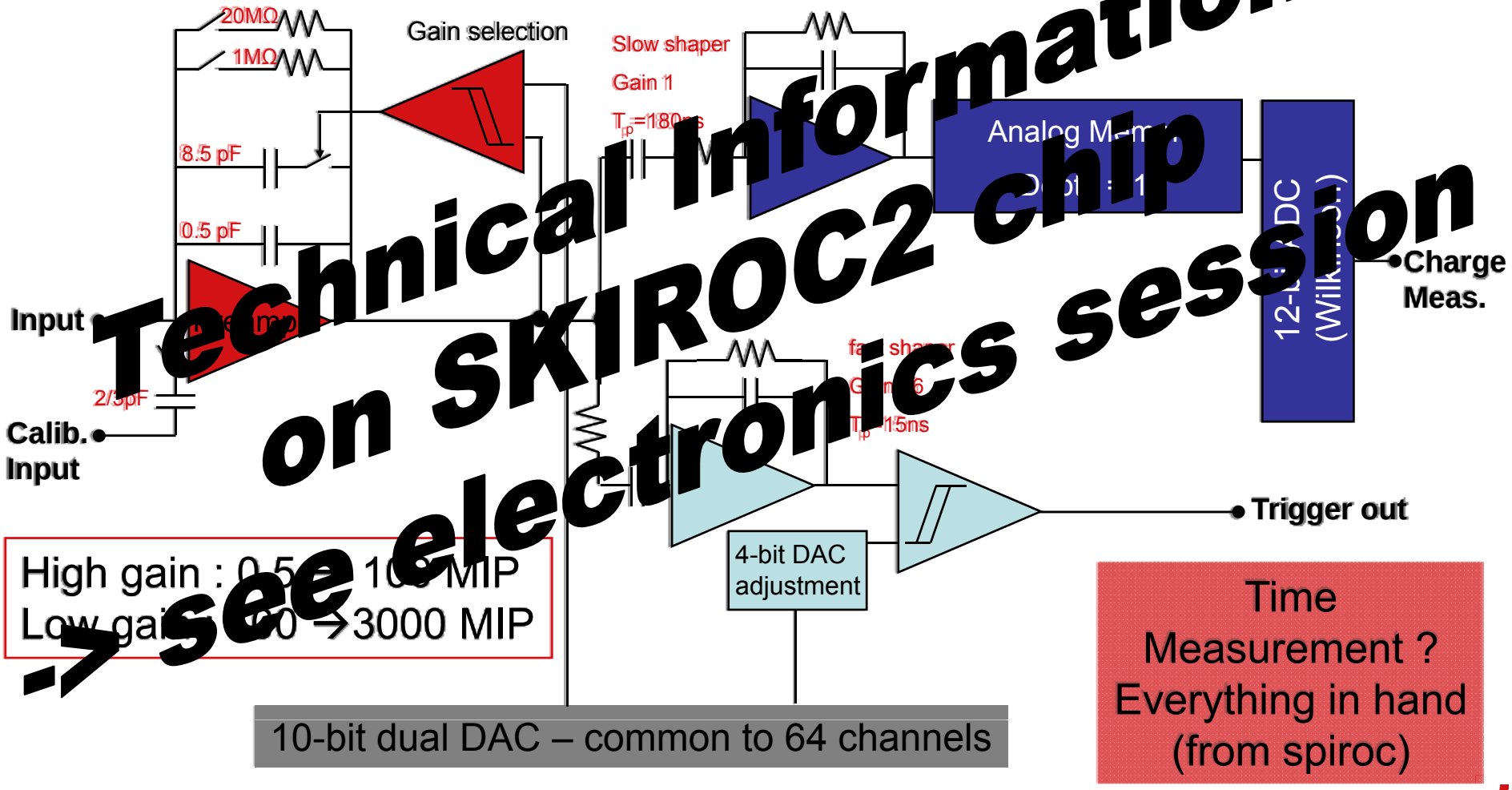
2010 → Production (~10 ASIC wafers)

- Microprobe station for SKIROC2 production test (100k€)
- Bonding of FEV8 production (try to establish collaboration with CERN)
- Selective dicing of wafers after probe testing (SKIROC).

SPIROC and HARDROC go to packaging

- SLAB test setup in LAL to validate assembling

SKIROC 2 block scheme proposal

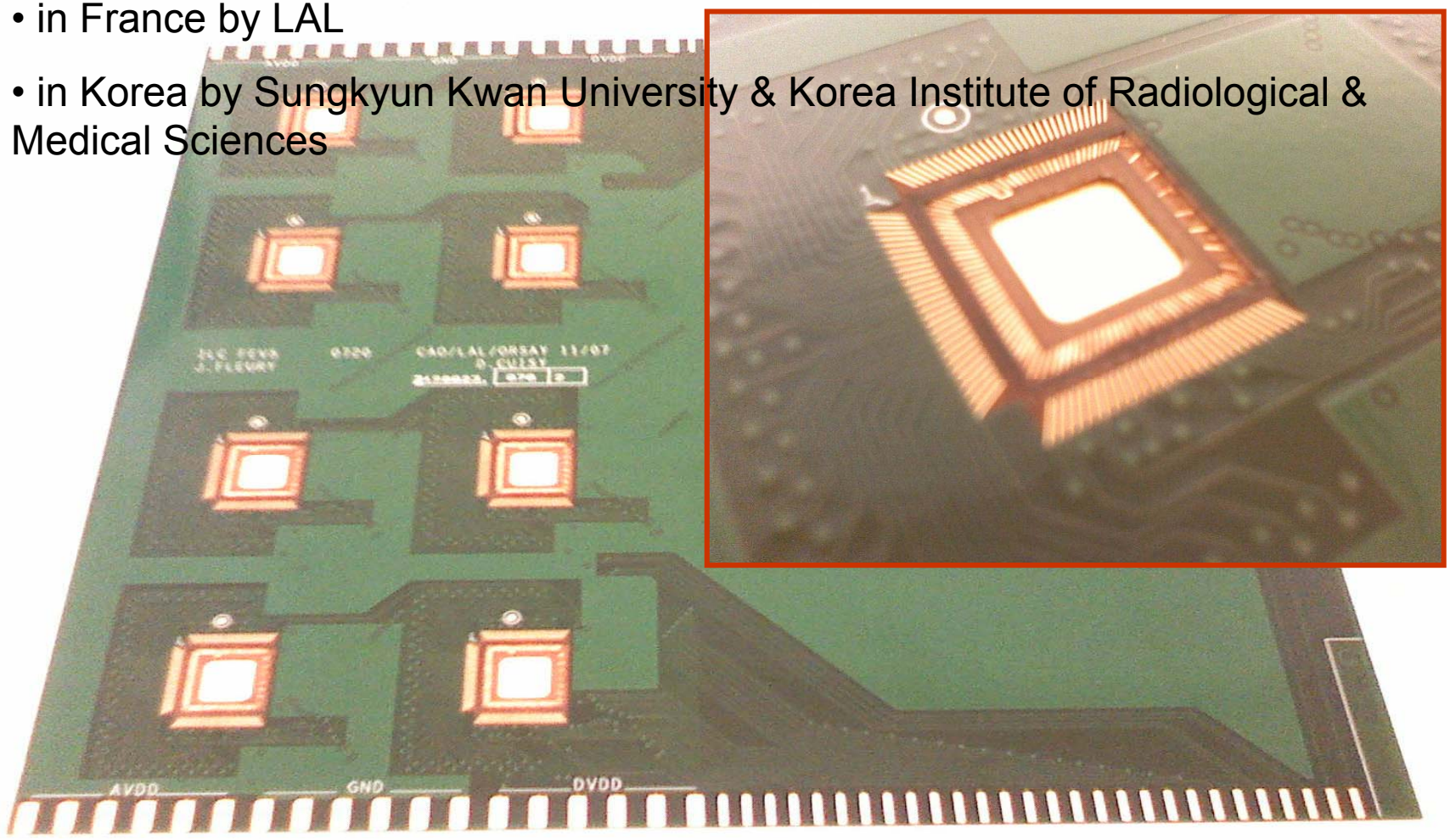


PCB design
FEV status

Reminder : FEV5 design

FEV5 manifacturing order:

- in France by LAL
- in Korea by Sungkyun Kwan University & Korea Institute of Radiological & Medical Sciences



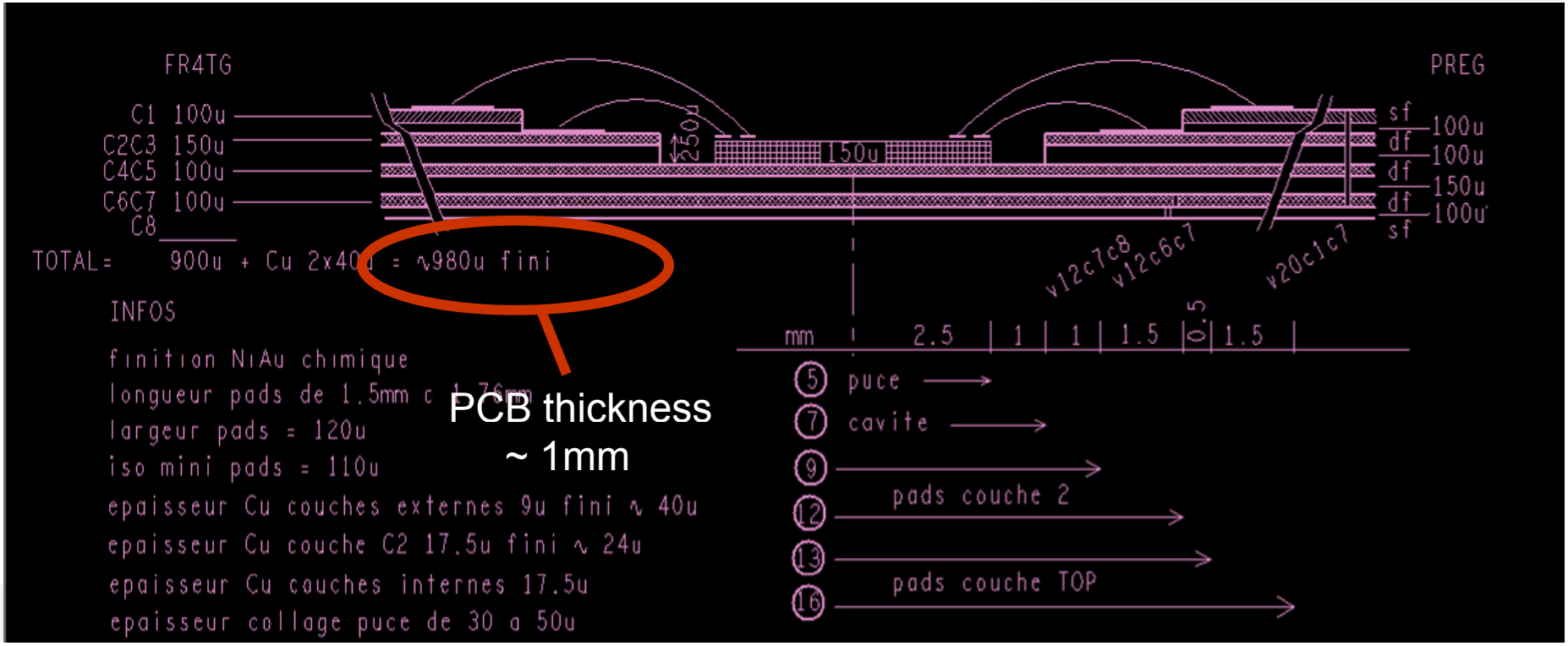
Chip Embedding + PCB Pile-up

Omega

Pile-up	
TOP	GND+routing
C2	AVDD+routing
C3	AVDD+DVDD
C4	GND + horizontal routing
C5	AVDD+ vertical routing
C6	GND+pads routing
C7	GND (pads shielding)
BOT	PADS

FEV 5

3 drilling sequences :
- Laser C7-C8 120µ filled
- Laser C6-C7 120µ
- Mechanical C1-C7

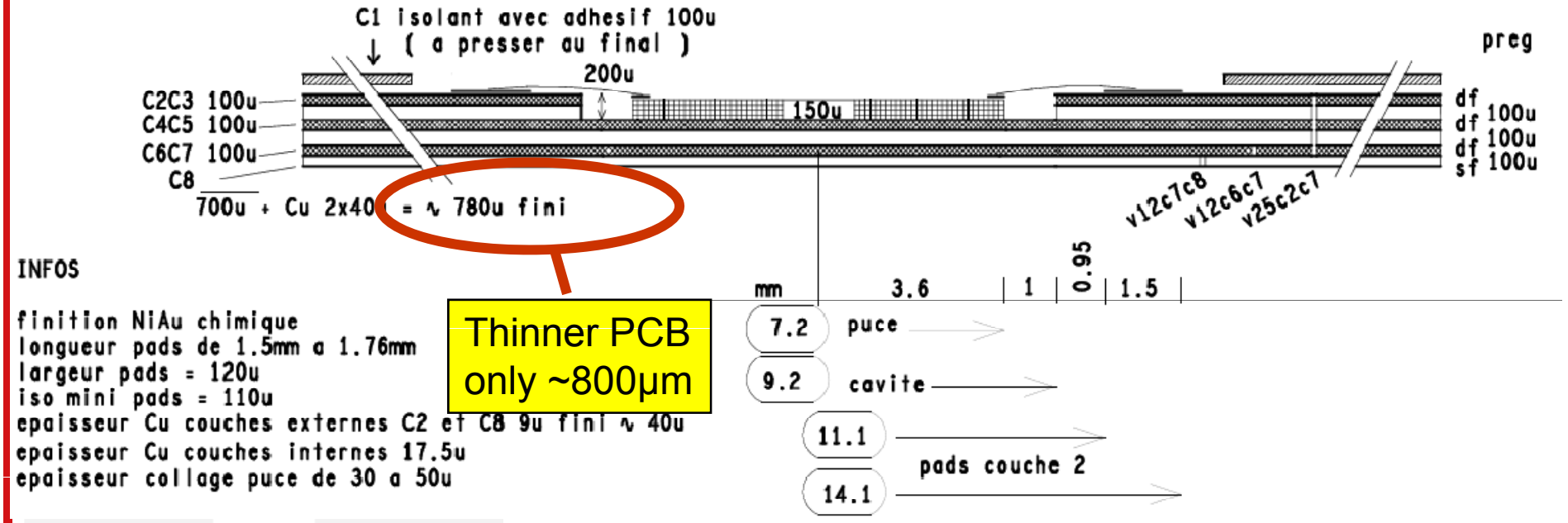


Chip Embedding + PCB Pile-up

Pile-up	
TOP	Mechanical filling layer
C2	AVDD + routing
C3	AVDD + DVDD
C4	GND + horizontal routing
C5	AVDD+ vertical routing
C6	GND + pads routing
C7	GND (pads shielding)
BOT	PADS

FEV 7

3 drilling sequences :
- Laser C7-C8 120µ filled
- Laser C6-C7 120µ
- Mechanical C2-C7



Issues : Layer 2 not bondable

FEV7

- First EUDET full compliant PCB, using SPIROC2 in SKIROC mode.
- several pads merged for each electronics input
- Halfway from expected granularity and physics prototype granularity

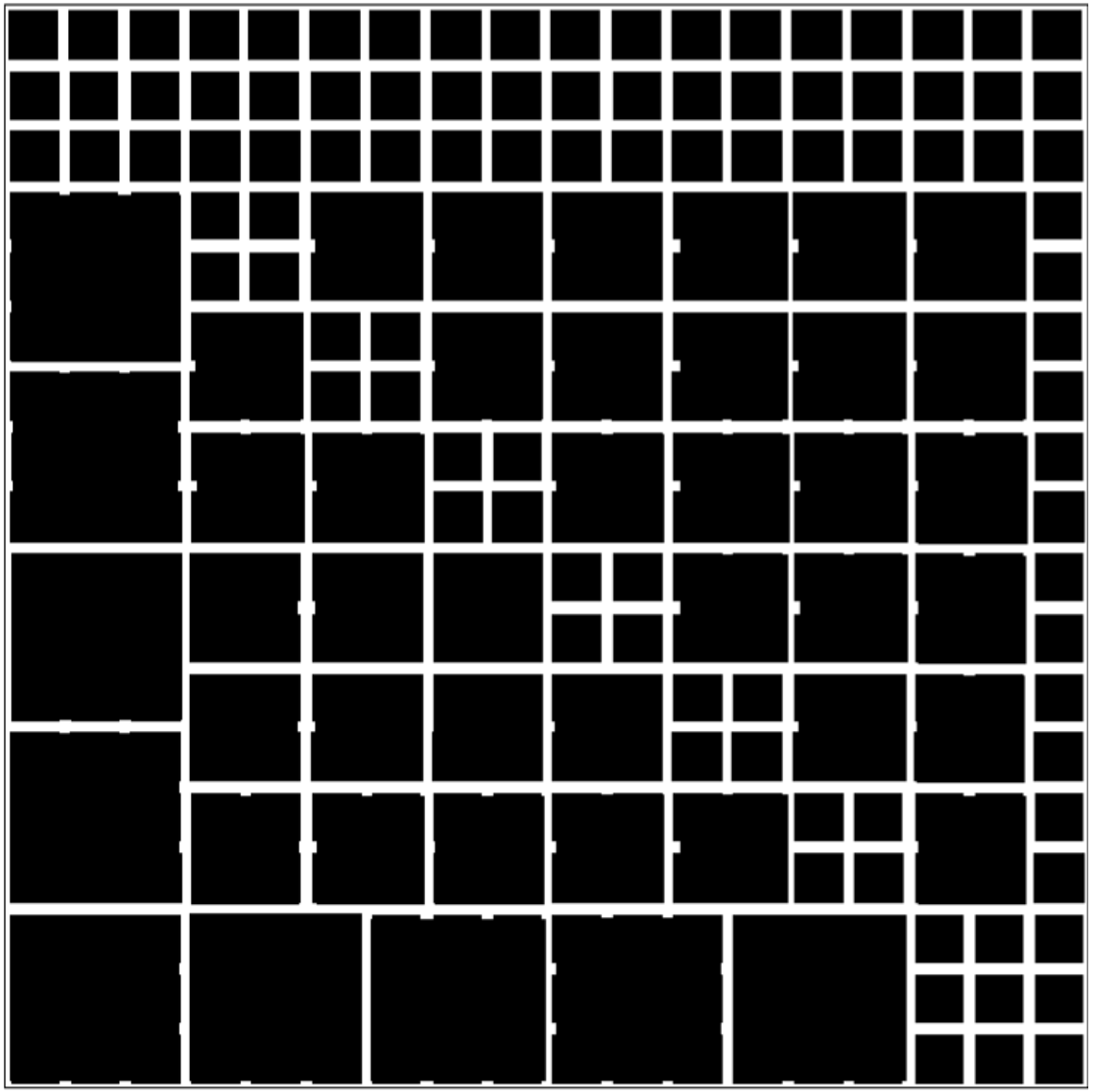
- Schematic finished using 4 SPIROC2 chip
- Layout in progress
- Production plan ? When technical issues solved !
- Eudet deliverable : 30th June 2009

FEV7 wafer footprint

144 Channels
Will be used for Wafer characterization

Need SPIROC2 validation

→ SPIROC2 measurement in progress…
see L. Raux's talk



Conclusion

- PCB design
  - Several FEV5 engineering done, in France and in Korea…
  - NOT SO EASY TO BUILD → still not validated since **November 2007**
  - FEV7 design using Hamamatsu Wafer and Spiroc2
  - FEV8 plan to use skiroc2
    - Opportunity to have 256 ch. Wafers ? (5.5mm pads)
    - Wafer size : 90 x 90 mm → 16 x 16 pixels
- Front-end ASIC design
  - Skiroc2 planned for June 2009
  - Hardroc2, Spiroc2 & Skiroc2 production
  - Very Aggressive schedule
  - Funding needed for production test in 2010 !

Backup slide : Schedule & Info

- Skiroc 2 expected to be sent in fab in June 2009
  - Still in design and simulation phase
  - Sharing of the HARDROC2 and SPIROC2 production
  - If SKIROC 2 is validated → production in hand for EUDET module
  - Cheaper than an engineering run for prototyping due to big silicon area (60mm² ie ~60k€)
- Next PCB prototype will use SPIROC2 with Hamamatsu wafers
  - Validation of all electronics and assembling process
  - missing : dynamic range (500MIP/2500MIP), granularity
  - PCB in hand in April 2009 ?

Backup slide : Expectations for EUDET module

- 64 channels to read out new 256 pads wafers with 4 chips
  - This is a critical PCB requirement
  - This will make SKIROC2 the biggest chip of the ROC family
    - 50-60 mm²
- Capability to operate in ILC mode and in test beam
  - This is a physics requirement to take data with EUDET module
  - Calculation of data rates to be validated
- High dynamic range from 0.1 to 3000 MIP
- (Eventually) time measurement to tag events in test beam (not useful in ILC mode)