# DHCAL Construction Status

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CALICE Meeting, February 19 – 20, 2009
Kyungpook National University, Daegu, Republic of Korea

# 1 m$^3$ – Physics Prototype

## Description

40 layers each ~ 1 x 1 m$^2$
Each layer with 3 RPCs, each 32 x 96 cm$^2$
Readout of 1 x 1 cm$^2$ pads with one threshold (1-bit)
~400,000 readout channels
Layers to be inserted into the existing AHCAL structure

## Purpose

Validate DHCAL concept
Gain experience running large RPC system
Measure hadronic showers in great detail
Validate hadronic shower models

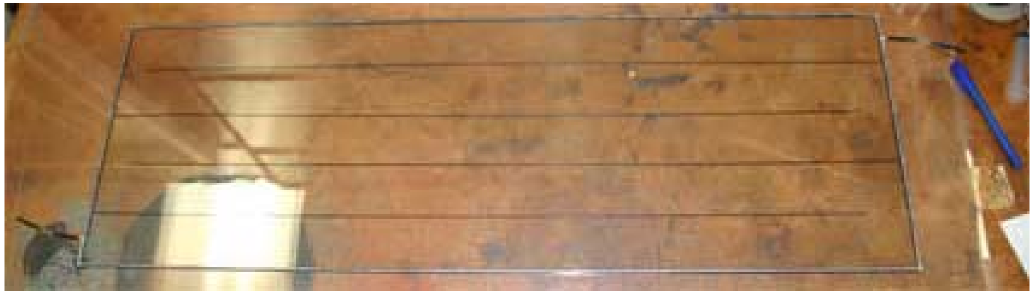
## Status

Started construction in fall 2008

# RPCs and cassettes

Not on critical path

## RPC design



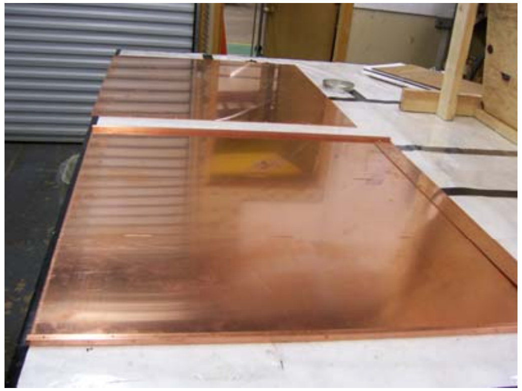
2 – glass RPCs
1 – glass RPCs (developed by Argonne)

## Prototypes

| Number of RPCs | Number of glass plates | Glass thickness [mm] | Size [cm] | Status | Tests | Problems |
|---|---|---|---|---|---|---|
| ~15 | 2 | 1.1 | 20 x 20 | built | 2 years | None |
| 1 | 1 | 1.1 | 20 x 20 | built | 2 years | None |
| 1+3 | 2 | 1.2 | 32 x 96 | built | 1 month | High pad multiplicity |
| 3 | 1 | 1.1 | 20 x 20 | built | 2 months | None |
| 2 | 2 | 0.85/1.2 | 32 x 96 | being built | | |

## Cassettes

Purpose: protect RPCs, cool front-end ASICs, compress RPCs
2 x 2 mm$^2$ copper sheets
First prototype  being tested



## Comment I: Glass thickness

Pad multiplicity of 32 x 96 $cm^2$ too large: due to glass of 1.2 mm (and track extrapolation)
Difficulty to obtain 0.85 mm glass in the U.S.
Vendor from Europe identified, provided 10 samples

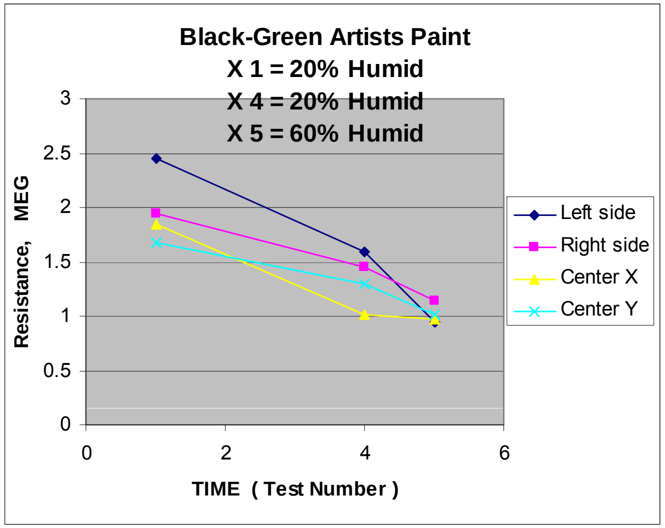
## Comment II: 1 – glass RPCs

Advantages: pad multiplicity ~1, thinner, simpler,
surface resistivity not critical,
better rate capability,
compression with electric field
Disadvantage: can't be assembled without final electronics,
recent design (less tested)
Some layers for the physics prototype will be equipped with 1 – glass RPCs

## Comment III: Resistive paint

LICRON paint (we all used for years) not available anymore
New LICRON product difficult to apply (backup solution)
Explored two alternatives

Artist paint (currently preferred solution)
Floor paint (possible solution)

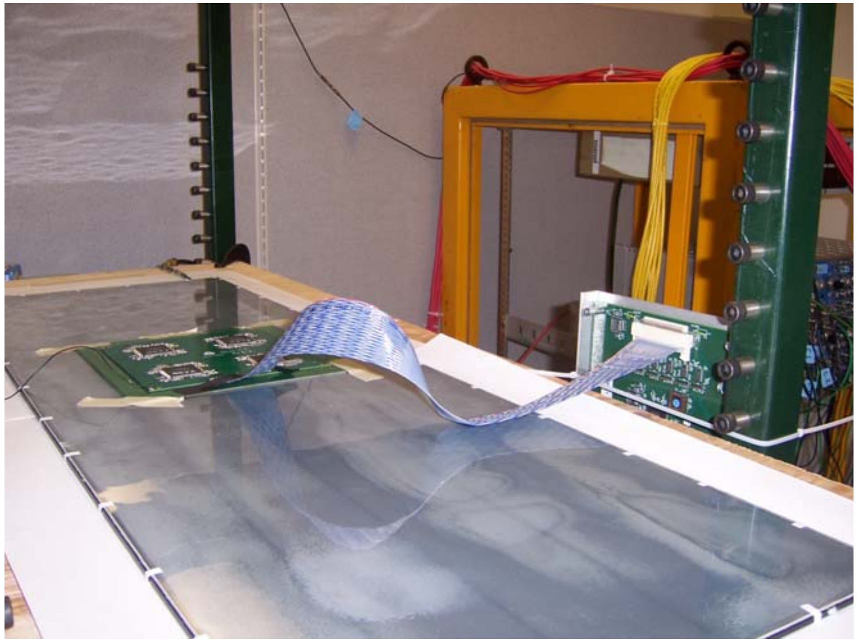


# Production of chambers

Need 120 chambers for physics prototype
Standard assembly procedure not yet developed
Availability of Argonne technicians

→ Expect production rate of 1 – 2 RPCs/day
→ Estimated 3 – 6 months for 120 chambers
(significant faster for 1 – glass chambers)

Cosmic ray test stand exists



# Front-end Electronics

## DCAL III chip

Currently on critical path

Produced in 2008
Received 11 wafers with 966 chips each → 10626 chips
Problems with packaging

Previous packaging obsolete
New package identified, clamshell for testing available
More chips than expected!

→ Packaged chips by early March

Testing to be done

'by hand' at Argonne for first chips (board being fabricated)
by robot at FNAL (being programmed)

## Pad- and Front-end board

Soon on critical path

32 x 48 $cm^2$ → 4 x 6 chips
Being designed (to be prototyped and tested in March)

## Data concentrator

Design and firmware completed
To be implemented onto front-end board

# Gluing fixture

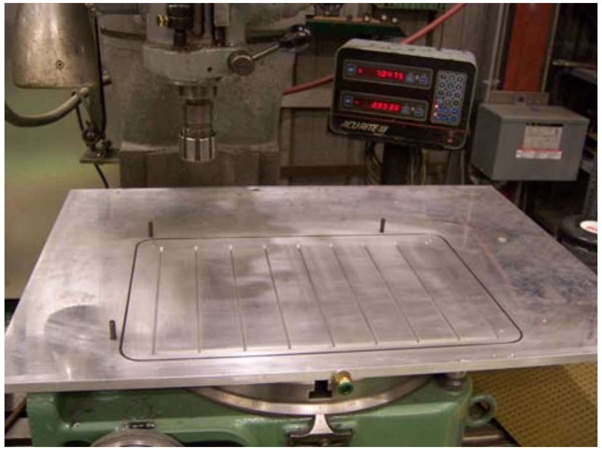
Conductive glue between pad- and front-end boards

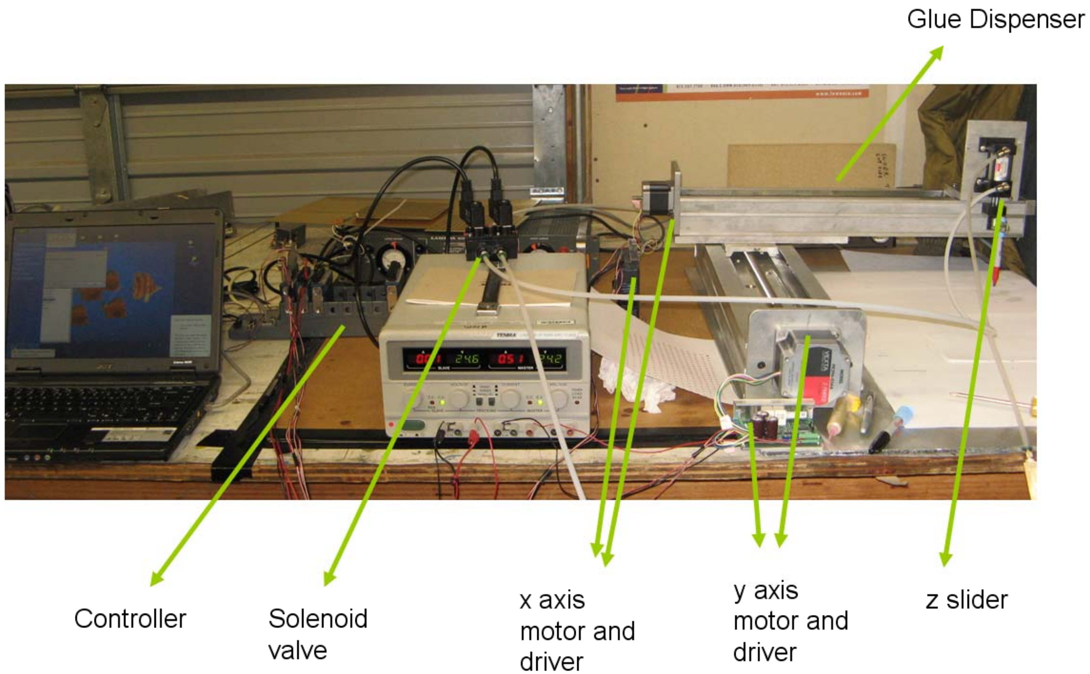
1536 dots in less than 3 hours

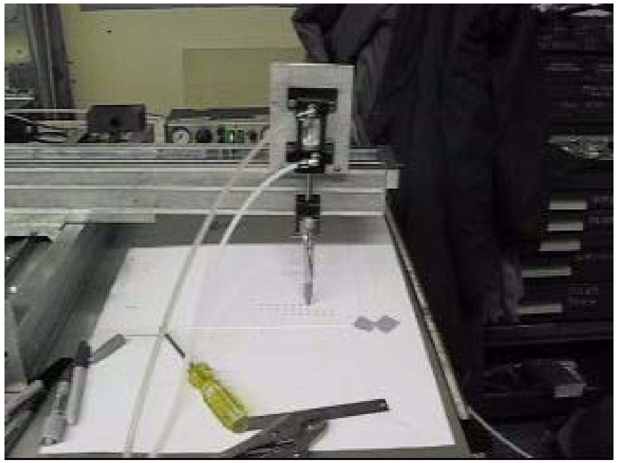
x-y machine designed and partly assembled

Control software written

Tests with glue to start soon





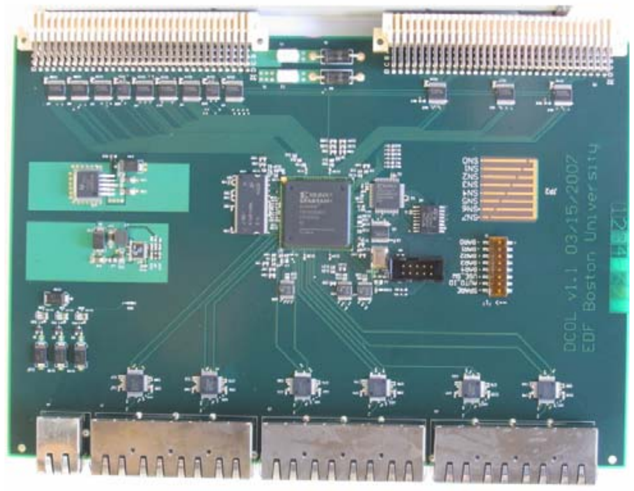



# Back-end Electronics

Not on critical path

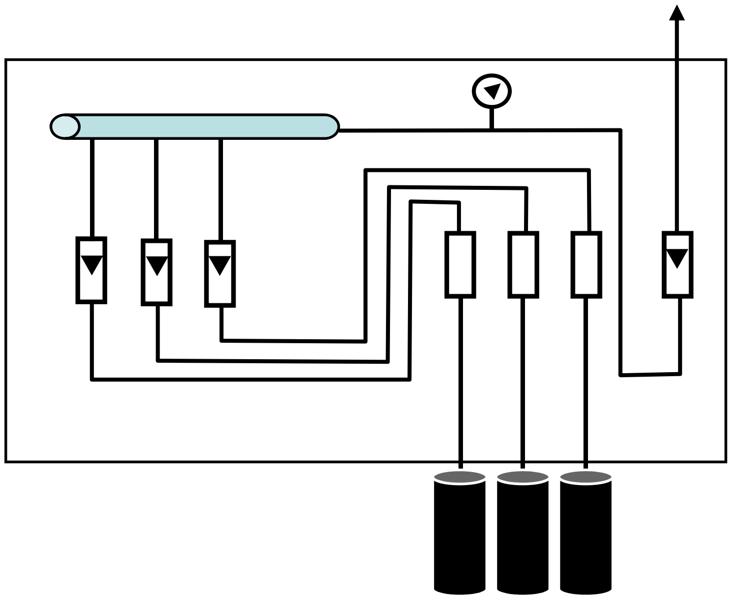
## Data collector (DCOLs)

New system design requires 20
Design finalized (identical to VST)
Production of 35 modules in March
Testing in April



## Timing and trigger modules (TTMs)

New system design requires 2 – 3
Minor design changes to be implemented
Production in March - April



# Gas and HV systems

Not on critical path

## Gas mixing system

Designed and gas flow controllers purchased
Other parts to be ordered this week
Assembly in March

## Gas distribution system

Re-use system from Vertical Slice Test

## HV system

Two full systems available
Control software written

## DAQ software

Not on critical path

Implemented into CALICE DAQ framework
New readout architecture and geometry being implemented

## OFFLINE software

Not on critical path

Conversion of VST data to LCIO done
Will be developed in next few months

Tentative agreement to use standard LCIO – Marlin – LCCD – Mokka chain
Detailed discussions at the next Technical board review at FNAL in May

# Test Beam Plans

Start with standalone DHCAL program (including TCMT!)

- Broadband muons for calibration
- Positrons 1 – 16 GeV
- Pions 1 – 66 GeV
- Protons 120 GeV

Followed by data taking with Silicon-Tungsten in front

Time scale still uncertain

- Possible start in 2009
- Definitely data taking in 2010

# DHCAL Construction Overview

| Item | Status | Outstanding problems/tasks | Critical path |
|---|---|---|---|
| **RPC construction** | Several prototypes exist | Test of thin-glass 2-glass chambers<br>Test of full-scale 1-glass chambers<br>(requires final front-end board)<br>Develop production procedure | (October - ?) |
| **DCAL chips** | Being packaged | Robot testing | Until ~May |
| **Front-end boards** | Being designed | Final design/prototype (requires final ASIC)<br>Testing procedure to be developed | ~May - October |
| **Back-end** | Being produced | Small modifications to the TTM design | No |
| **Gas system** | Being assembled | None | No |
| **HV system** | Completed | None | No |
| **DAQ software** | Being modified | None | No |
| **OFFLINE software** | Being developed | None | No |

# Towards a Technical Prototype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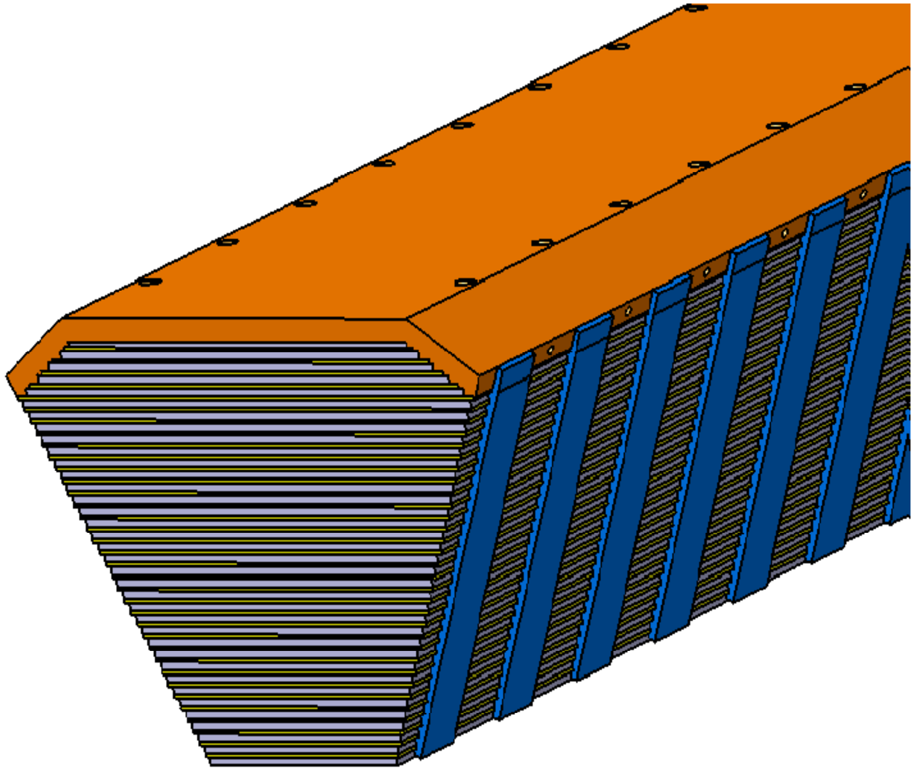
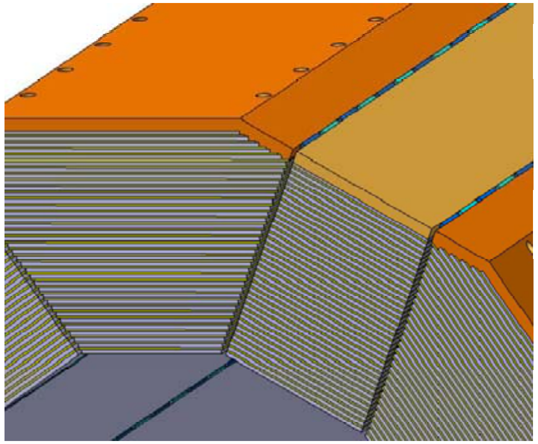
# What is a Technical Prototype

E.g. SiD's latest ideas about the HCAL barrel



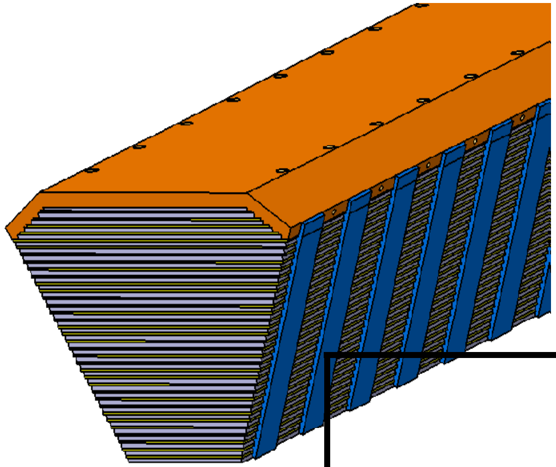
12-sided polygon



Technical prototype module

Wedge-shaped
6 m long
40 active layers
$120\ m^2$ of RPCs

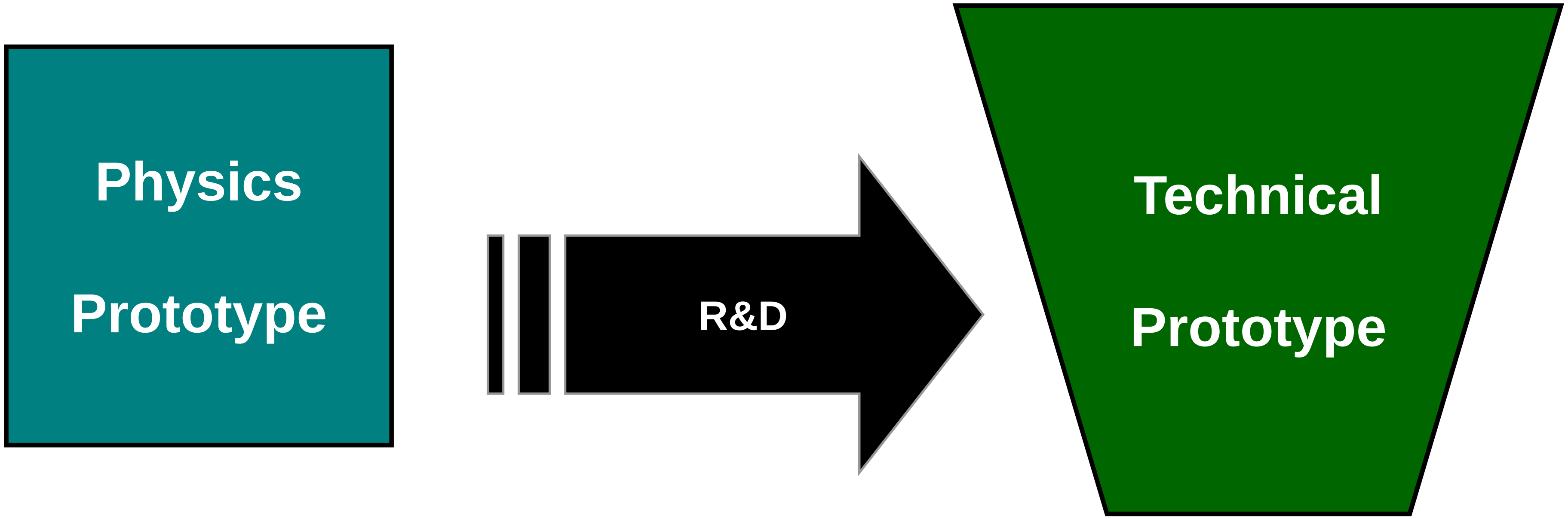
} approximately



# Connections to the outside world

| | Connection | 1 $m^3$ prototype | Technical prototype |
|---|---|---|---|
| **RPC** | Gas inlet | 40 | 1 |
| | Gas outlet | 40 | 1 |
| | High-voltage supply | 40 | 1 |
| | High-voltage computer control | - | 1 |
| **Front-end electronics** | Low-voltage | 120 | 1 |
| | Cooling water inlet | 40 | 1 |
| | Cooling water outlet | 40 | 1 |
| | Data cable | 240 | 1 |

# Topic of this Talk




View from the U.S. DHCAL group…

# A. Large Area RPCs

**Area approximately up to 1 x 6 $m^2$ in one layer**

How to handle 3 - 6 m long glass, is it available?

Typical thickness 0.8 – 1.1 mm

How to distribute high voltage on the surface?

Difference in high voltage leads to different efficiency

How to circulate the gas within a chamber?

Flow needs to be uniform, since gas contamination uniform

How to minimize the dead area?

In 1 $m^3$ prototype about 3.3% (frame) + 1.4% (fishing lines)

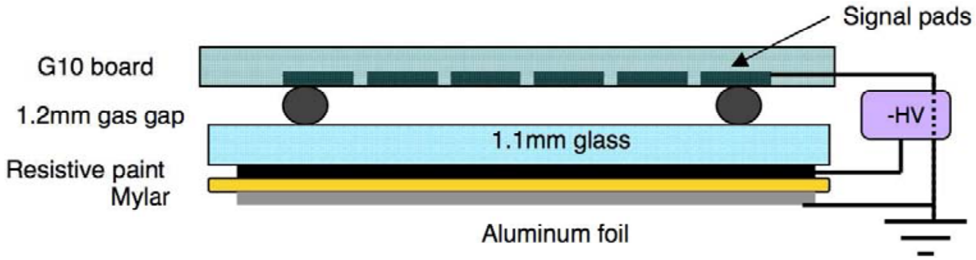
**Currently not being investigated**

# B. Thin RPCs

Marty keeps telling us that every mm costs several M$

## One-glass design developed by Argonne

Saves ~ 1mm/layer
Improves rate capability, pad multiplicity
Surface resistivity not critical
No problem with keeping the front-end board flush with the glass




## Is it reliable?

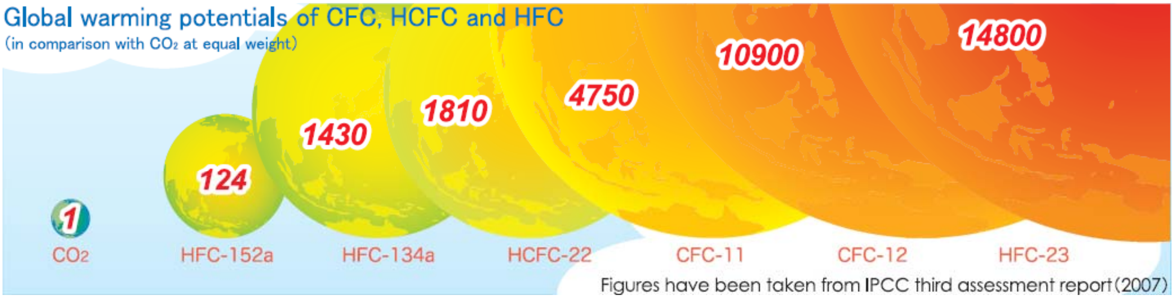
One prototype has been tested for 18 months
No changes in performance seen
Was opened – deposits around fishing line

## Is it practical?

Once glued on, the front-end board can not be exchanged, without destroying the chamber

**Will be further investigated with the 1 $m^3$ prototype calorimeter**

# C. Gas System




Using Freon HFC-134a

- Currently being vented
- Will be prohibited in the near future

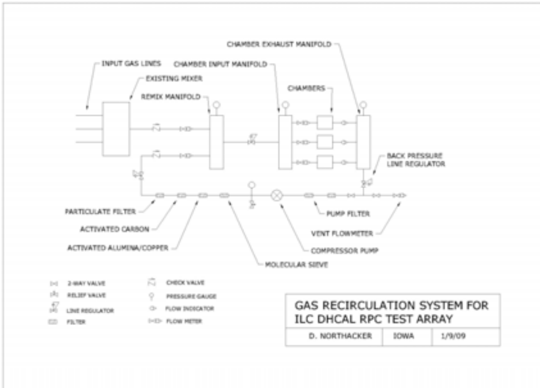
Need to identify an alternative with comparable performance

- So far Ar, $CO_2$ based mixtures do not match HFC-134a
- Perhaps HFC-152a will do (just approved as coolant for car A/C systems)

**Don't know about recent activities**

Need to recirculate the gas

- Difficult issue
- Not entirely successful at the LHC
- We have new ideas…

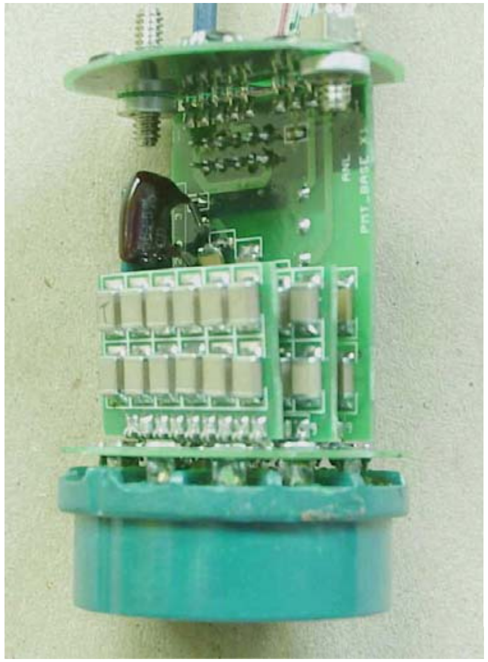



Gas distribution within a module

- Major headache
- Needs manifolds, implemented in wedge structure
- Needs to provide same gas flow to each layer!

**Requested funds for Iowa to develop**

# D. High Voltage Distribution



Currents in RPCs are small (~nA)

Voltages are high (~6.3kV)

Variations between layers due to construction

Need to set HV in each layer individually
Need ability to measure current in each layer
Need ability to switch off sparking layers

Brilliant idea?

Cockcroft-Walton technology?

**Requested funds for Iowa to develop (together with Argonne)**

# E. Cassette structure

Needed to protect RPCs (glass)
Needed to maintain smallest gap between glass and pad-board

→ Only for 2-glass design ←

**Experience with 1 $m^3$ prototype calorimeter will help**

Not needed for cooling of Front-end electronics?

DCAL power consumption ~ 0.2 Watt/chip
Assuming 120 $m^2$ → 1,200,000 channels → 18750 ASICs → 3750 Watt/module
Power pulsing (?) reduces this to 40 Watt/module

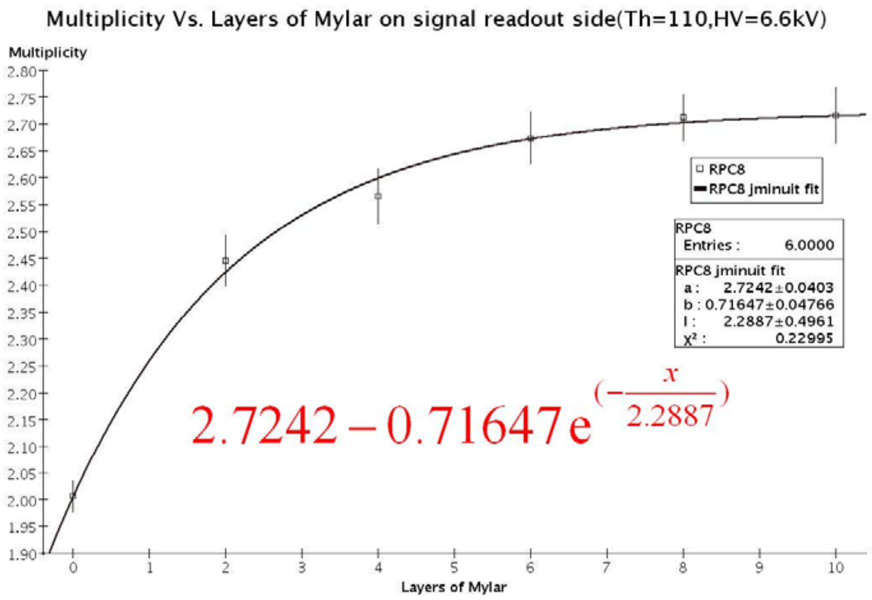
Test beam, Cosmic Rays

Requires triggered readout
Can't apply power pulsing efficientl
Needs cooling…

Additional challenge

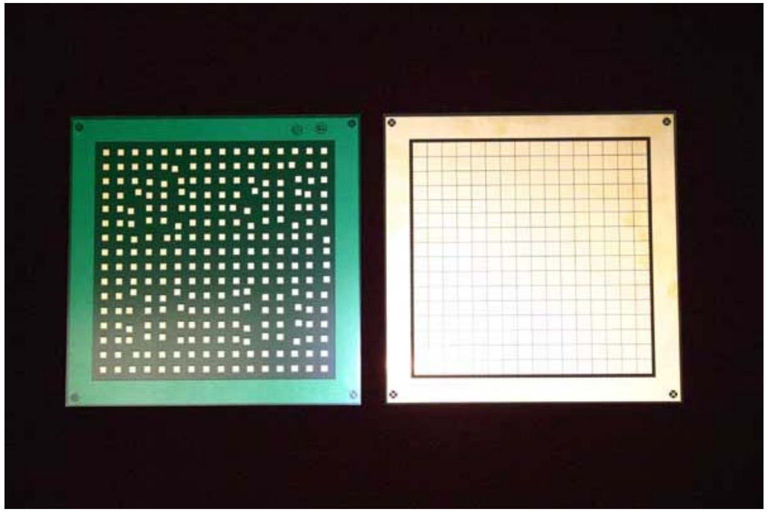
Cassettes needs to be stiff enough not to
crash the glass, electronics

→ in any module orientation ←



# F. Pad-board

Assuming we keep the 1 x 1 $cm^2$ segmentation



## Current design

Pad-board separate from front-end board
Neither has costly blind or buried vias
Connection to front-end board with conductive glue
Total thickness of pad- + front-end boards ~ 3 mm
Fixed width for 1 x 1 $m^2$

## New design needed

Minimize thickness (but reasonably stiff)
Avoid blind or buried vias
Avoid gluing
Accommodate wedge shape

**Currently not yet pursued**

Fixed or variable number of pads?
Fixed or variable width of pads?

# G. Front-end ASIC

**Memorandum of Agreement between ANL and FNAL concerning the design of ASICs**
**Plan is to work on DCAL IV**
**(among other things)**

## Currently (DCAL III chip)

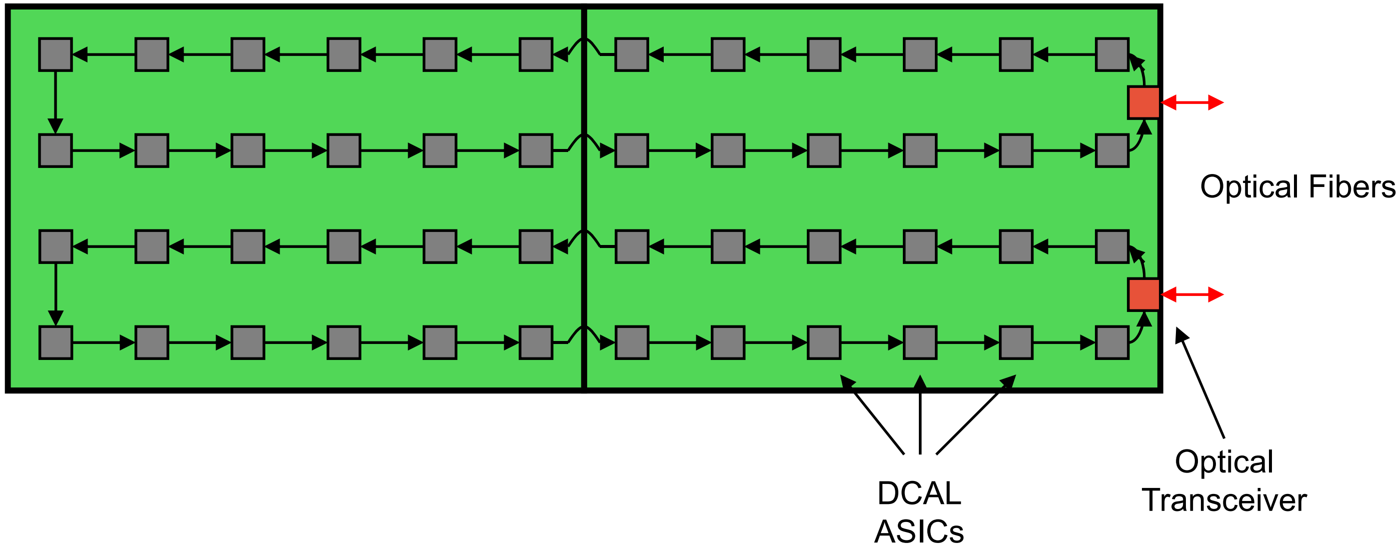
64 channels/ASIC
No power pulsing
Direct communication with data concentrators
Height ~ 1.4 mm

## Needed for the technical prototype

Increased number of channels?
Power pulsing
Token ring passing
Minimal thickness (not packaged?)
Keep triggered readout for test beam, cosmic rays
Further improvements to DCAL III

Trivial implementation into chip
Challenge with large pulsing system

→ power supplies
→ em noise




**Reliability!**

# H. Front-end data concentrator

**Reliability!**

Currently

- 6 x 4 ASICs per board → 1 data concentrator

Exploit more modern technologies

- e.g. Gigabit Transceivers
  - Serving a whole row of ASICs (up to 50)
  - Output 1 single optical fiber to be routed to outer edge of module

**Currently not yet pursued**

# I. Low-voltage distribution

Currently

1 cable per front-end board

Need to develop

Distribution system
Ability to turn on/off each layer individually
Ability to measure currents to each layer individually
Ability to handle power pulsing

**Currently not yet pursued**

# J. Back-end readout system

Currently

VME based system located in rack
LVDS communication with data concentrators

Technical prototype needs

System located in back beam area
Optical fiber link with front-end

**Currently not pursued (by us)**

# K. Mechanical Structure

Currently

Being developed by both ILD and SiD

Details of the design

Depend on the outcome of the above mentioned R&D
Significant effort needed to design a viable structure

} **Not yet urgent**

# Overview of R&D for Technical Prototype

| R&D topic | Being addressed | Planned to be addressed | Plan to be developed |
|---|---|---|---|
| Large area RPCs | | | x |
| Thin RPCs | x | | |
| Gas system, distribution | | x | x |
| High Voltage distribution | | x | |
| Cassette structure | | x | |
| Pad board | | | x |
| Front-end ASIC | | x | |
| Front-end data concentrator | | | x |
| Low Voltage distribution | | | x |
| Back-end readout system | | | x |
| Mechanical structure | x | | |

**Lots of challenges and work…**