Behavioral simulation of the front-end & read-out electronics

ROC & DIF behavioral model

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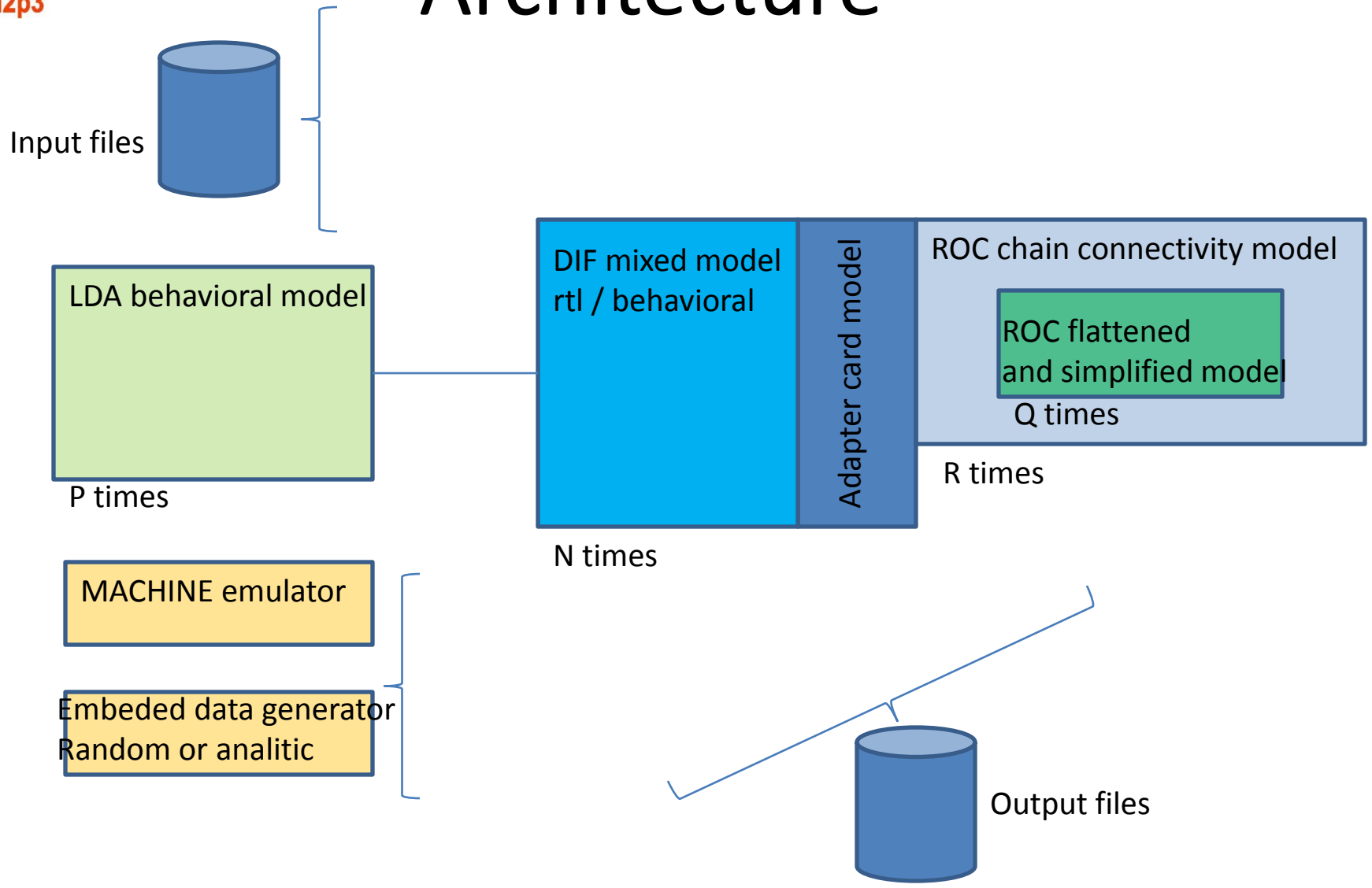
Outline :
Motivations
Simulation bench

Motivations to have a global behavioral simulation

- ROC
  - behavioral model can be seen a data sheet
    - Common material to discuss on
    - Can be use as simulation bench for FW dev.
  - Reference model to be use for development of other parts
    - Allow a lightweight "realistic" simulation
    - Can include simplified analogue blocs
- DIF, DCC, LDA
  - Study various scenarios: buffer depth, number of chip partitions, read-out sequence
  - Provides a test bench that can help to develop code
  - Reference simulation for procedure
    - common tool to agree on a way to do things,
    - better than a long description on paper…)

Architecture

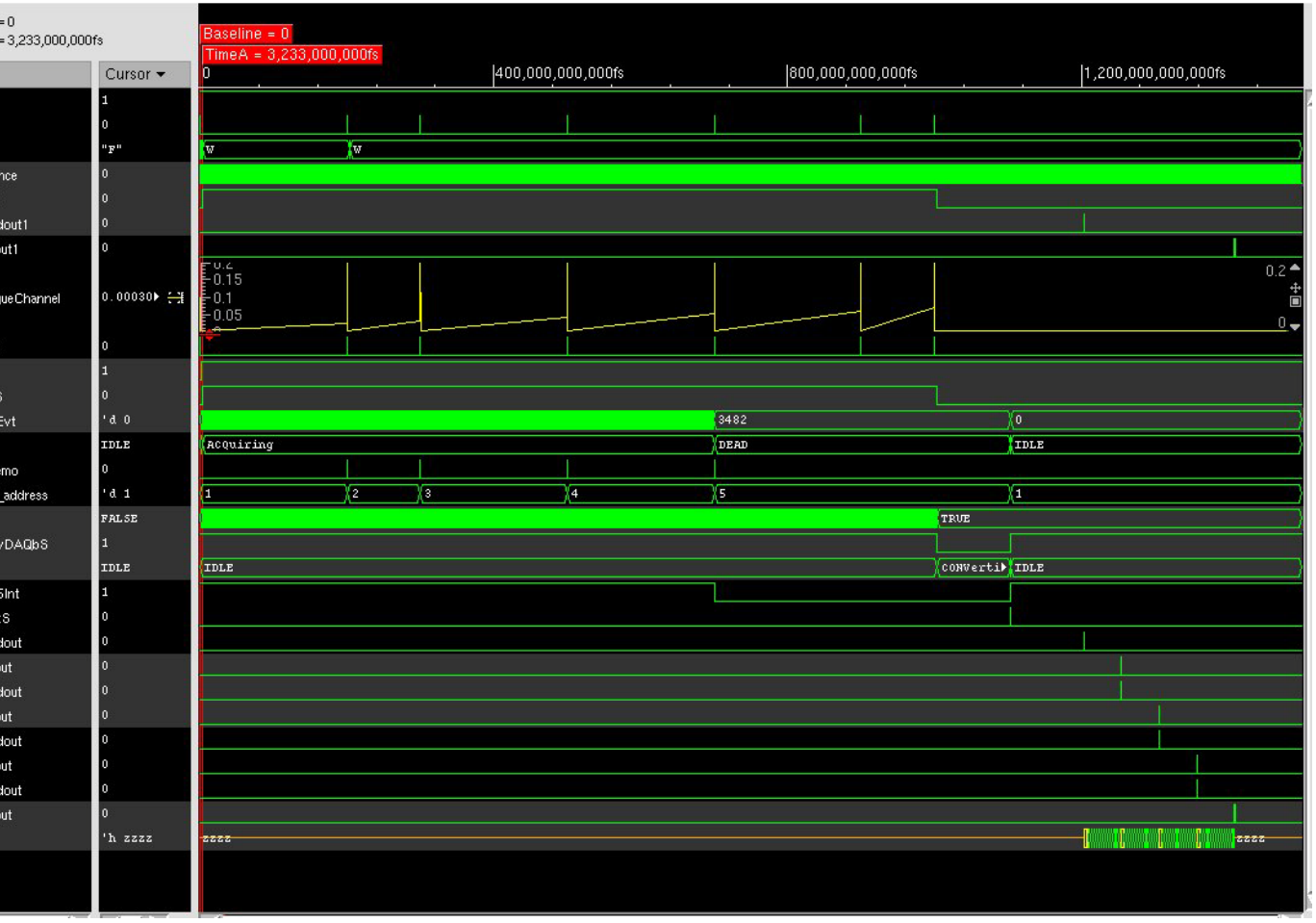


Input files

- Script to sequence operations
  - Send commands
  - R/W SC data
  - R RO data
  - Wait for data aquisition
- Data files
  - Could be physics occupancy maps
  - Fake or taken from real events/simulation
  - Configuration (SC, transmission delays, etc…)
- Configuration could be generated by the real SW

Example of DEMO 0.5 version

COSMIC mode : acquisition, conversion and read-out



Random trigger pulses Machine CLK

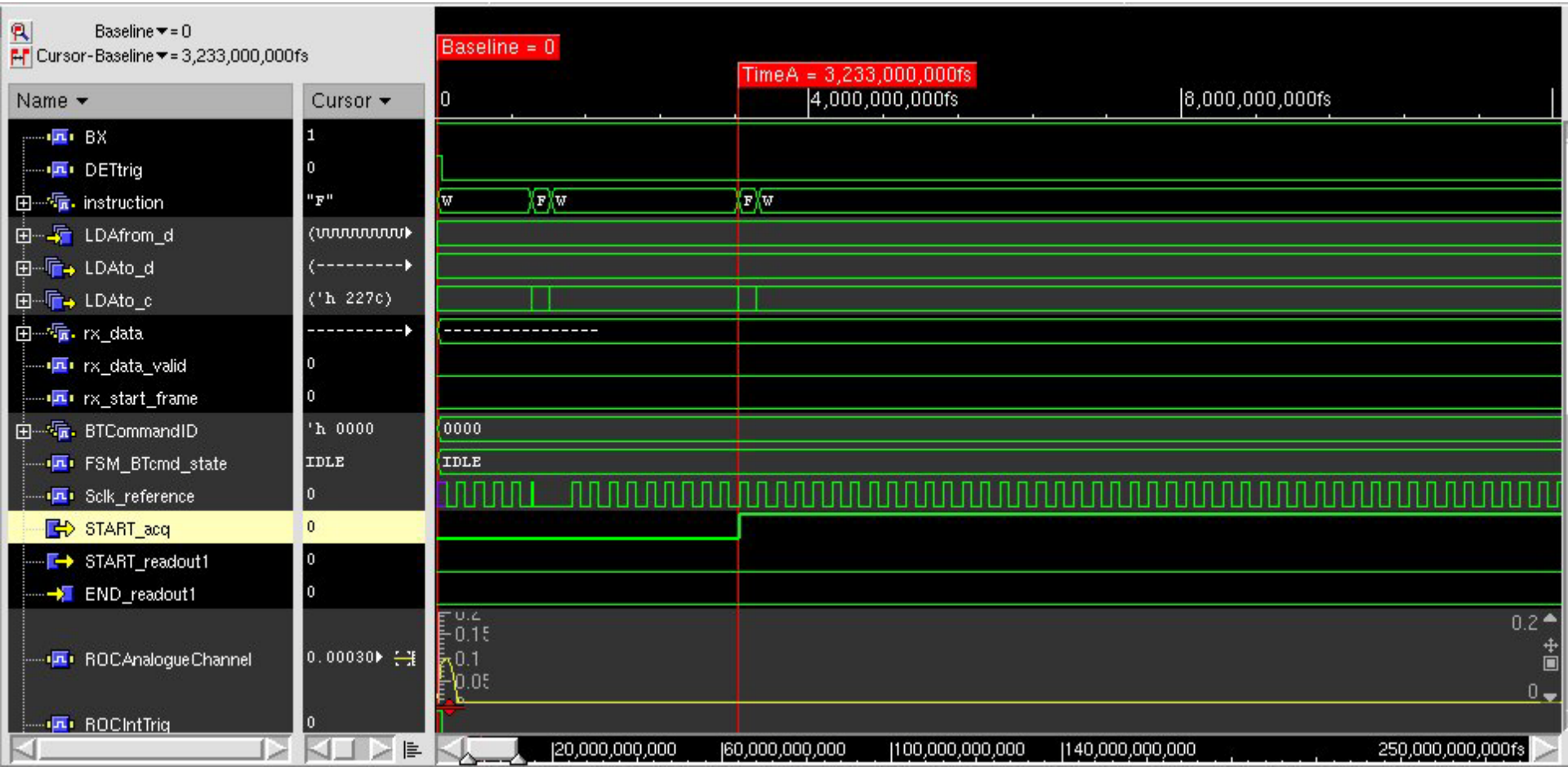
Optional analogue data generator

ROC model : amplifier, gain selection, internal trigger, analogue memory, digital part, etc..

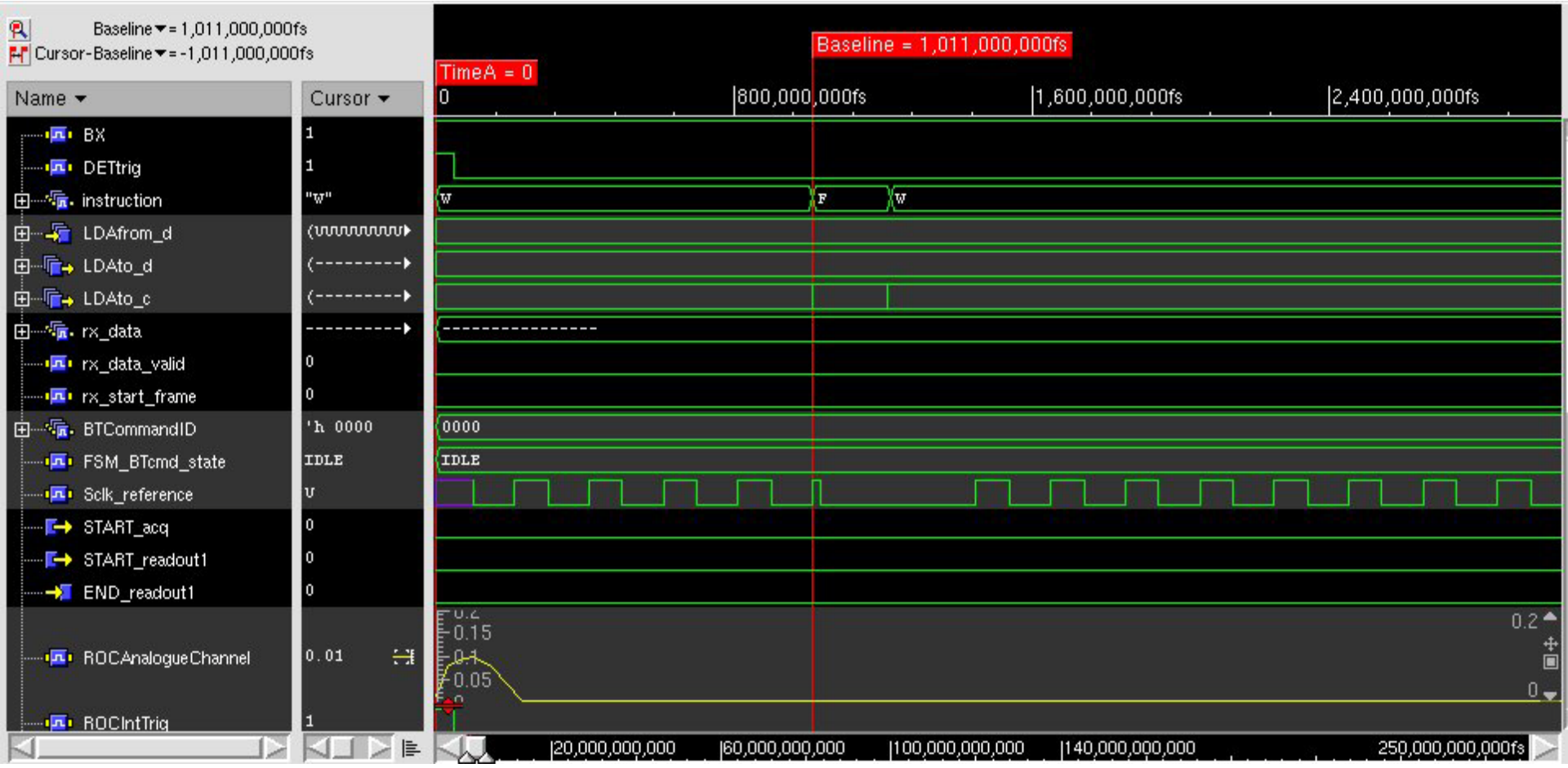
DIF signals (start/stop read-out)

Data flow (simplified interface, allow to check buffer occupancies, etc…

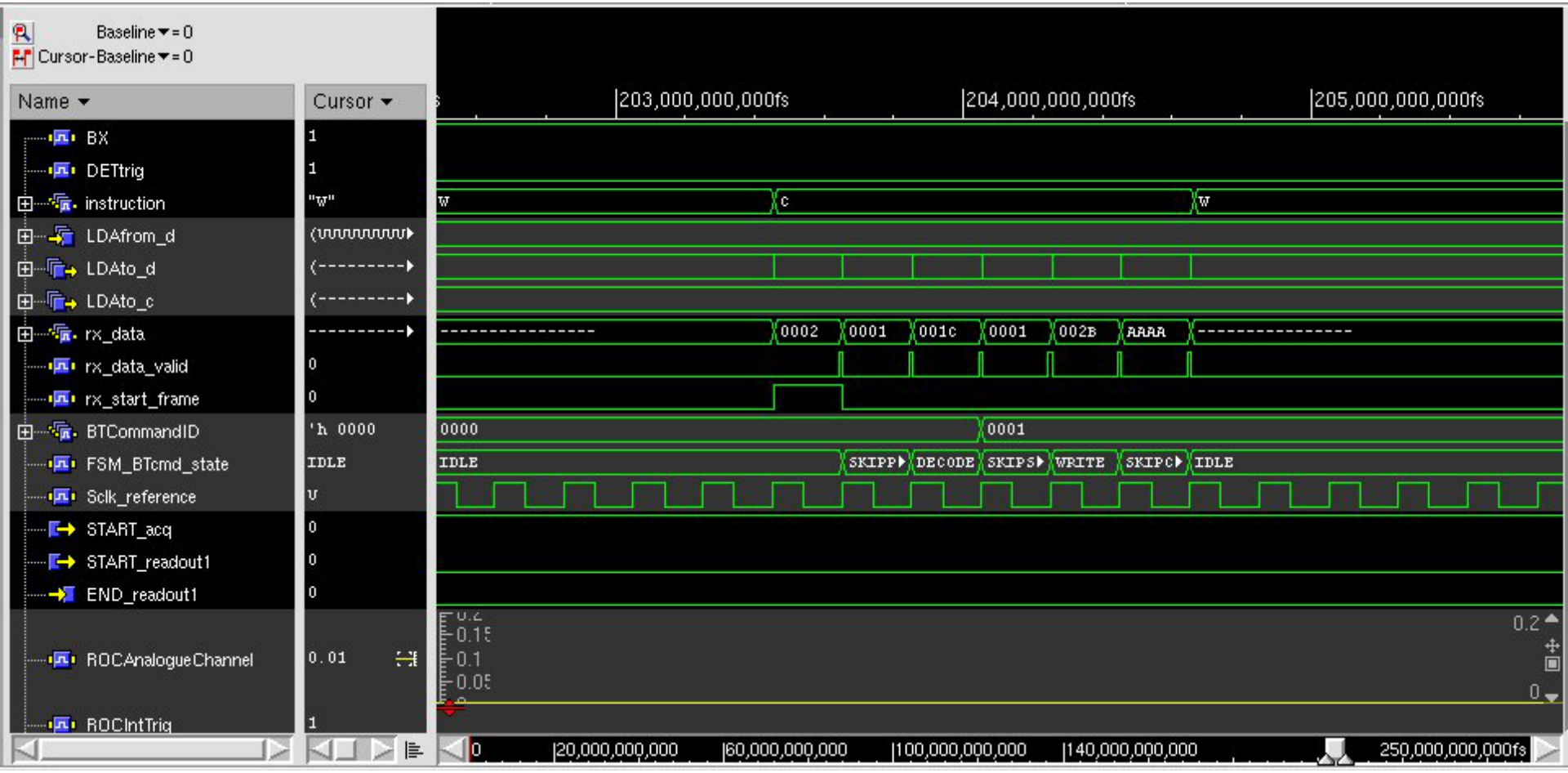
DEMO 0.5 : start aquisition



DEMO 0.5 : Sclk Resync



DEMO 0.5 : command decoding by DIF



Status

- Structure of the simulation bench is done
  - Blocs interfaces allow either studies at functional level or with rtl code (developement)
- Improvements needed to output nice results
  - Buffer occupancy based on detector statistics
  - Interface to SW
  - Interface to physics data
  - A lot of behavioral code is still to be written
    - Not a huge effort as it is behavioral
    - Simple things but very useful to have a comprehensive overview of the front-end/readout electronics

Conclusion

- Attempt to enable a behavioral simulation of the overall electronics, at system level
  - Timing checks, synchronization, data flow
  - Can use physics data
  - Can include power, signal integrity features
- DEMO version on the web (ask me for login/pswd)
  - http://cvs.in2p3.fr/calice
- Reference code to agree on, a way to document the system