

SW for European RPC DHCAL

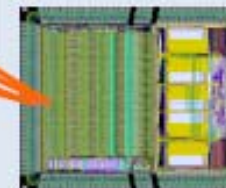
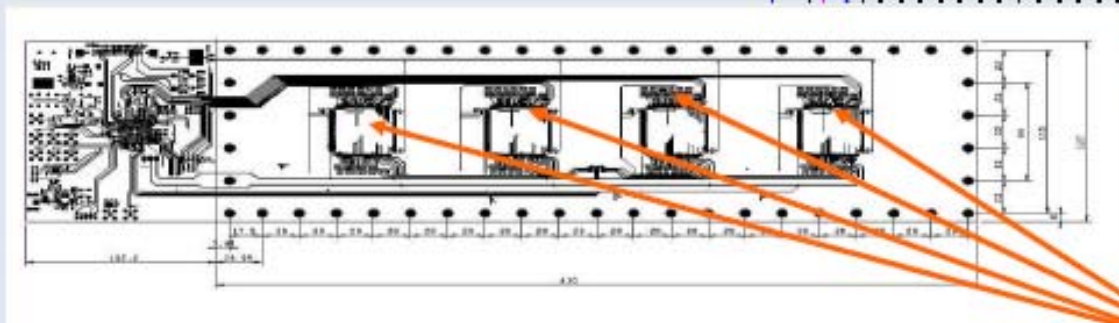
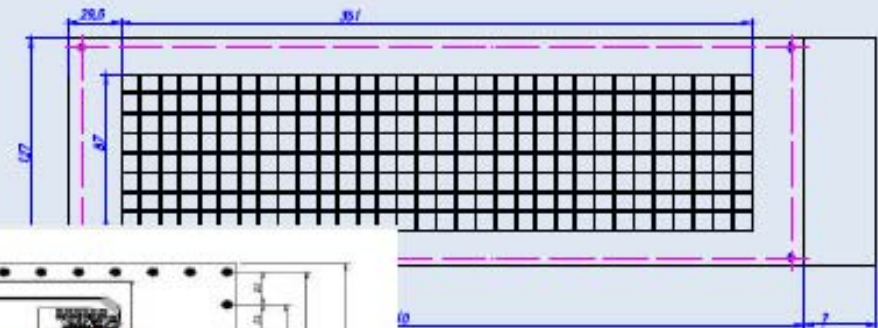


Manqi Ruan

- Test Beam Experiment:
 - Electronics
 - Raw data & Plan for data format transition
- Simulation:
 - ILD SHcal04 with Mokka
 - Plan for Digitization process
- Analysis: PandoraPFA (see Imad's talk)

DHCAL1 board

- 8×32 pads detector (GRPC and μ MEGAS)
 - 8-layer PCB
 - 4 HARDROC's (64 ch each)
- integrated DIF
 - Code being re-used for the DHCAL DIF's
- USB connector
 - libDHCAL developed
→ C driver, LabView interface





Upgrade : long slabs



DIF

Slab 1

PCBs conected
with 0 ohms
resistors

Slab 2

Information stored in raw data

Raw Train:

```
[[header] incl: train number
Trailer data DIF (data
Checking counters/CRC)
time difference between external
Trigger and RPC hit
[DIF
 [ASIC
  [frames: ASIC ID,
BC ID + 64 * 2bits_thr]
 : x n_frames (<128)
 [frame]
 ]
 : x n_ASIC (<256)
 [ASIC]
 ]
 : x n_DIF (limit ?)
 ]
```



DHCAL Event:

[Header:

- Event index in train
- in beam/out of beam (~ noise)
- Complete/Incomplete (All ASIC ready or not)
- mean TimeStamp

]

[List of Hits: All hits with the same TimeStamp

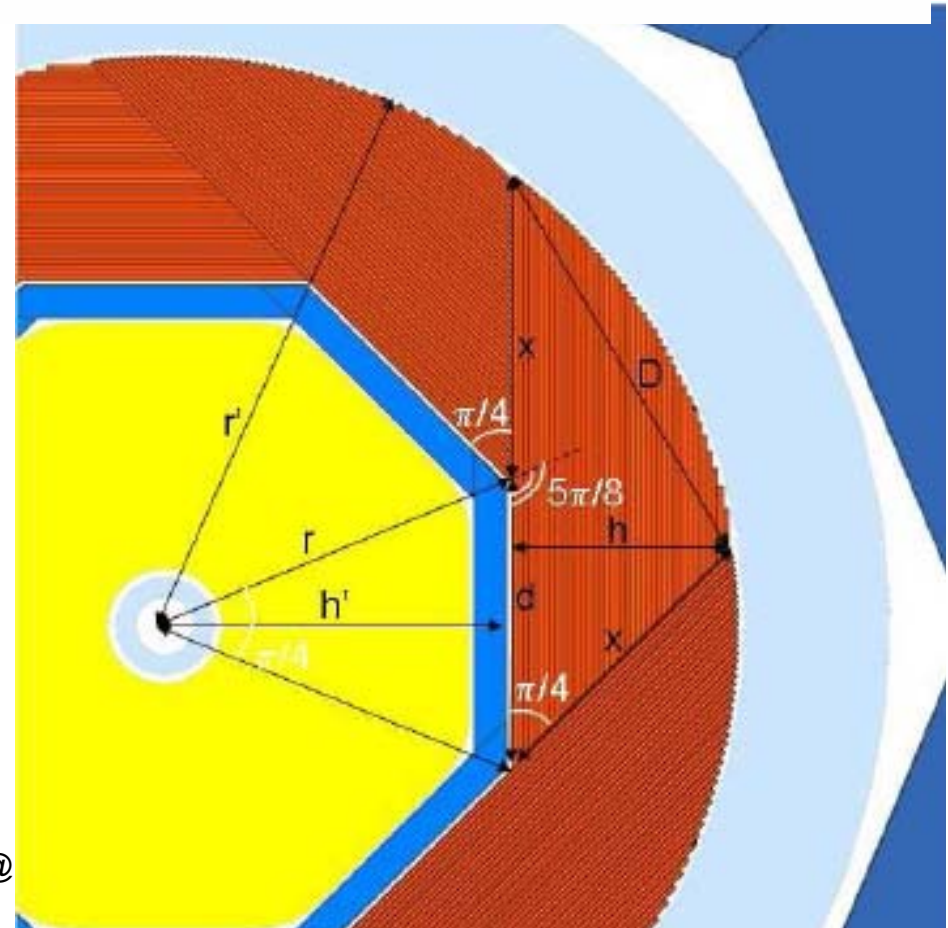
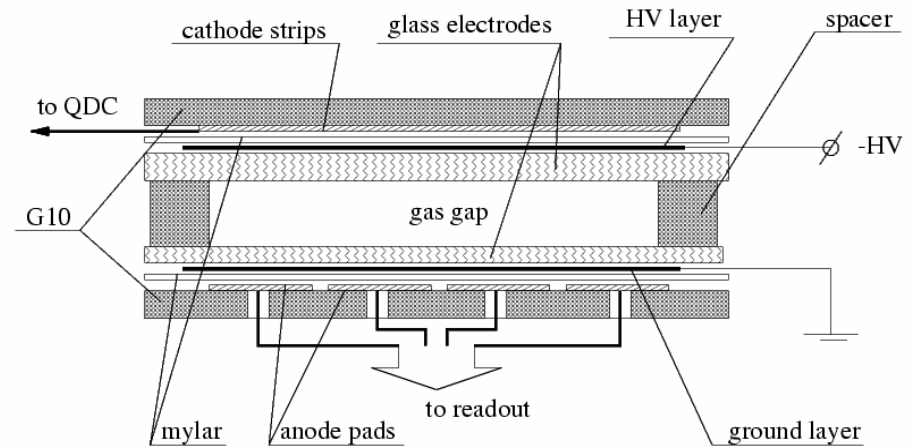
- TimeStamp wrt Spill_start or MeanTimeSTamp
- Threshold (Energy in ECAL & AHCAL)
- IJK
- XYZ
- Time_to_previous_Hit_in_same_cell

]

Plan: rewrite the information into the form similar to Calorimeter Hit

DHCAL Geometry

- Barrel region: 8 staves, 5 modules, 48 layers. 1920 DIFs
 - Ring: 2×4 staves, 6 layers
 - Endcap: 2×4 staves, 48 layers
 - 1cm×1cm cell. Each ASIC is response for 8×8=64 cells.
- ➔ Studies on DHCAL Occupancy & Leakage have been done



SimCalorimeterHit & CalorimeterHit

----- print out of SimCalorimeterHit collection -----

```
...  
[ id ] | cellId0 | cellId1 | energy | position (x,y,z) | nMCParticles  
      -> MC contribution: prim. PDG | energy | time | sec. PDG
```

----- print out of CalorimeterHit collection -----

```
...  
[ id ] | cellId0 | cellId1 | energy | position (x,y,z) |
```

- SimCalorimeterHit → [Digitization Process](#) → CalorimeterHit → Analysis Module (PandoraPFA)
- Current Digitization Process: True energy deposition in RPC Gas layer × Sampling factor → without considering the avalanche effect
- From the Test Beam: efficiency & energy deposition in the Gas by a mip is known → New Digitization Process

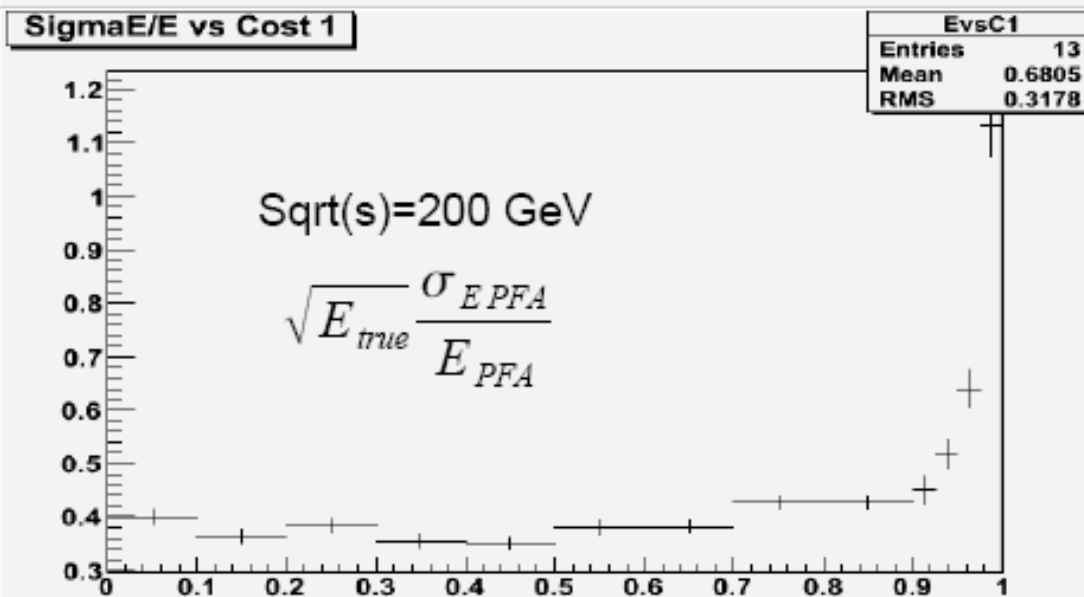
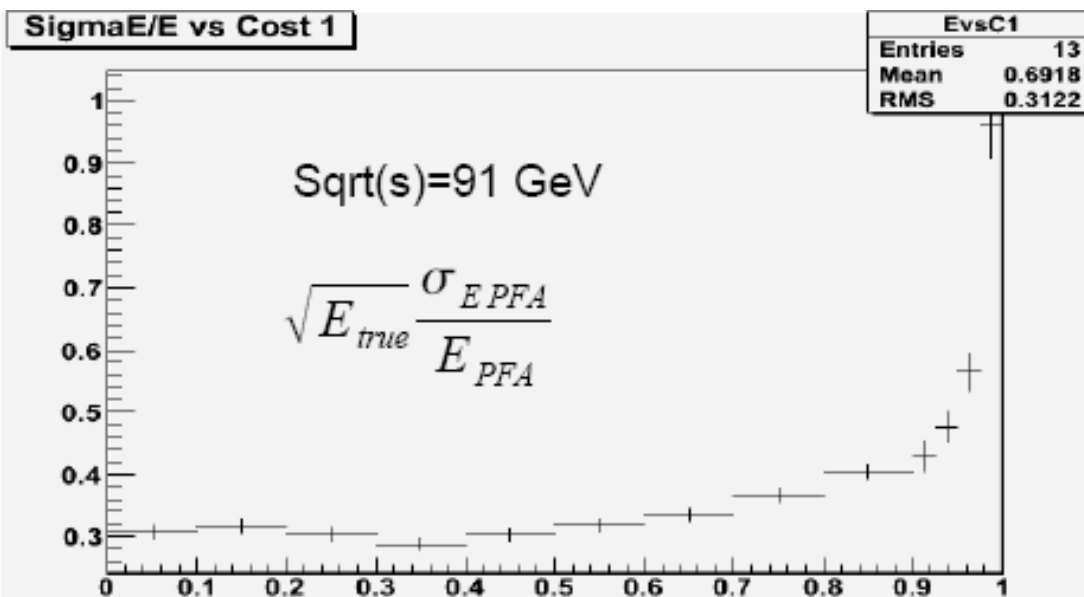
Back Up Slides

Pandora Analysis with SHcal04 Simulation

In barrel :
30.8 % \pm 0.4 % at 91 GeV
Jet resolution = 4.6 %

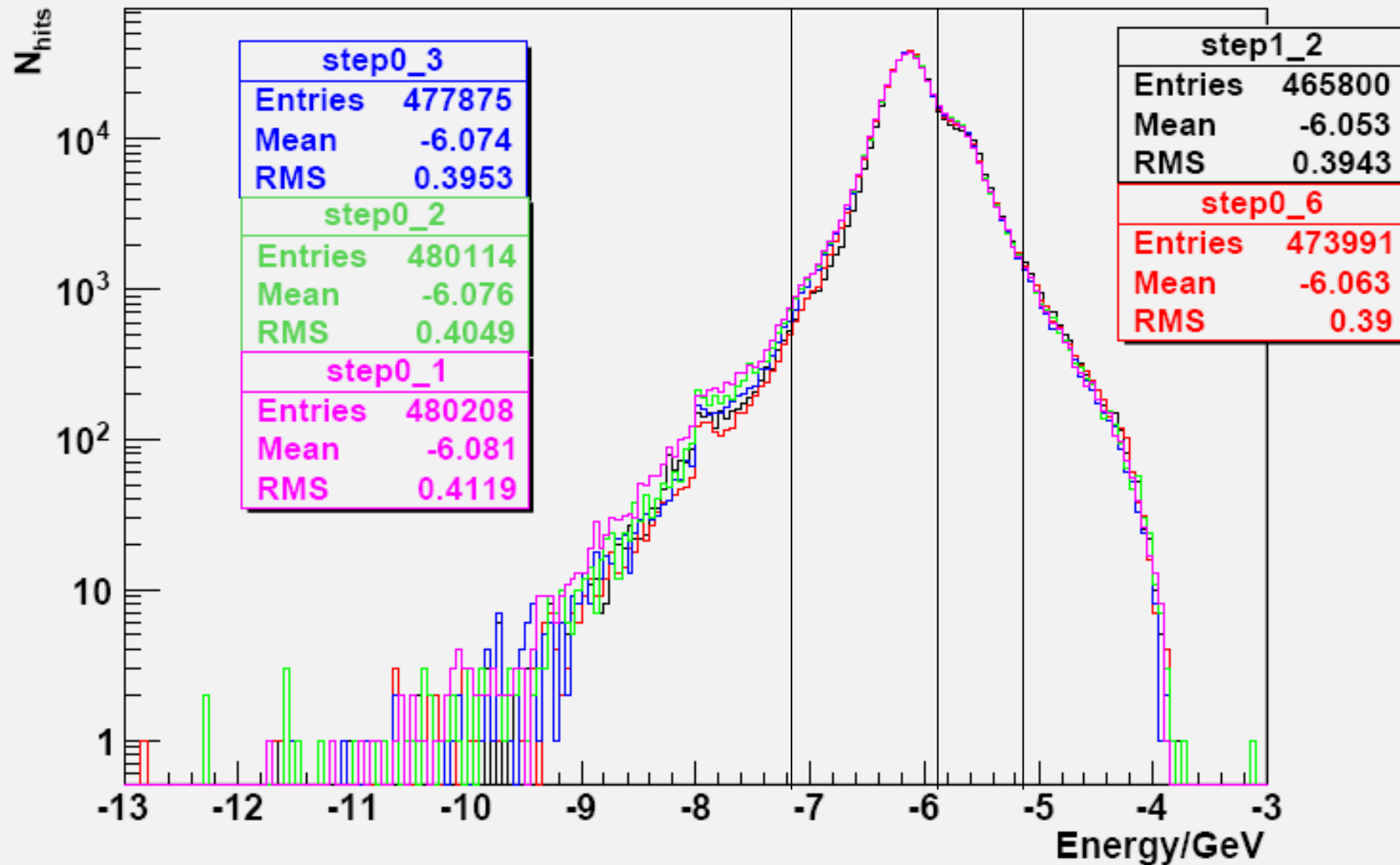
Using tools provided by
Mark Thomson

In barrel :
37.0 % \pm 0.4 % at 200 GeV
Jet resolution = 3.7 %



Semi DHCAL: 3 Threshold at 0.1mip, 2mip & 10mip

Energy Spectrum for Hits in DHCAL Barrel with 10GeV Muon (10k stat each)



Raw Event Data format

```
class RawEvent4Tree {  
public:  
    ulong TrigCount;    // should be the same  
                        // on all boards  
  
    uint fNBoards;      // Number of Boards  
    TClonesArray *fBoards; // Array with all boards  
    uint fNAsics;      // Number of Asics  
    TClonesArray *fAsics; // Array with all Asics  
    uint fNFrames;     // Number of Frames  
    TClonesArray *fFrames; // Array with all frames  
}
```

```
class Board : public TObject {  
    uchar BoardID; // Board ID from the DAQ  
    ulong FpgaID; // Board ID from the FPGA  
    ulong TrigCount; // DIF internal event counter  
    ulong ExtTrigInAcq; // DIF inter counter of  
                        // trigger in Acq mode  
    ulong ExtTrigOutAcq; // DIF inter counter of  
                        // trigger outside Acq mode  
    ushort Flags; // DIF internal flags  
    ulong DiffCount; // 40MHz (25ns) counter between  
                    // last ROC intTrig & ExtTrig  
    ulong LastBC; // BC ID  
  
    int fNAsics_in_Board; // Number of Asics  
    static const unsigned int vers; // version  
}
```

```
class Frame {  
    unsigned char ID; // ASIC ID  
    unsigned long BC; // BC ID  
    double time; // time of frame  
                // in  $\mu$ s wrt trigger (neg)  
    bool t0[NChan]; // Thresholds 0  
    bool t1[NChan]; // Thresholds 1  
}
```

```
class Asic {  
    int ID; // should be the same on all frames  
    unsigned long LastBC; // BC ID  
    unsigned int fNFrames_in_Asic; // Number of  
                                    // Frames  
}
```