

Status & development of the software for CALICE-DAQ





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On behalf of UK Collaboration

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Outline

- Introduction of existing system;
- Development strategies;
- Task lists and its development status;
- Summary & outlook



Software Basis: DOOCS

User Application layer

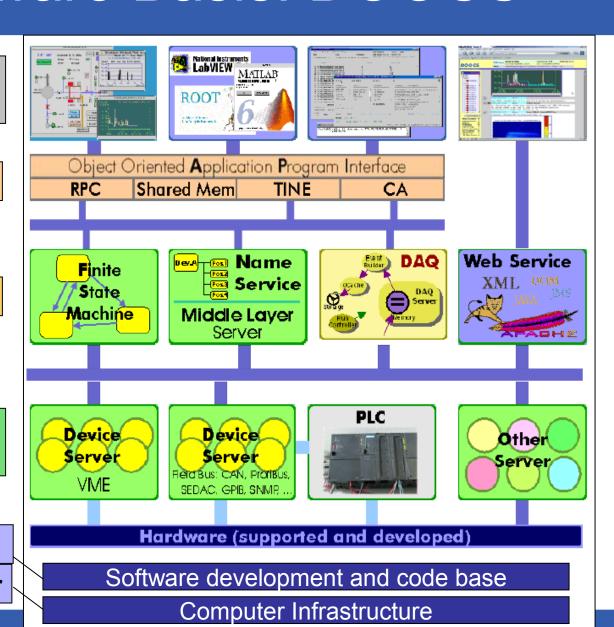
Communication

Middle layer

Hardware Interface Layer

Software Libs

Sun/Linux Cluster



CALICE/EUDET DAQ



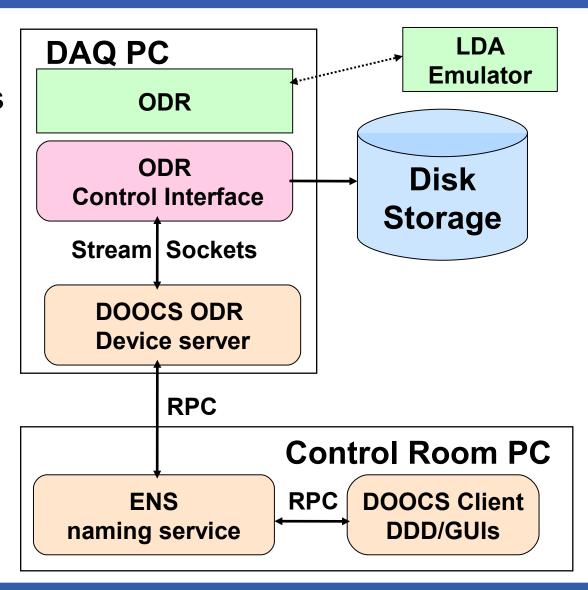
Device server & ENS

- Modeling hardware card via device server in OO
 - Existing: ODR & LDA device servers;
- Equipment Name Server (ENS):
 - Facility(F) / Device(D) / Location(L) / Property (P)
 - Detector type, components, instances & properties;
 - e.g. CALICE.ECAL/ODR/ODR1/Status
 - F: CALICE.ECAL, CALICE.AHCAL, CALICE.DHCAL
 - ► D: ODR, LDA, DIF, ASICs;
 - L: ODR1,ODR2,ODRX; LDA1,LDA2,LDAX; DIF1,DIF2,DIFX;
 - Property: X X X customize.
- To classify all properties and functionalities of each device for our DAQ system is ongoing!
- An interface talking to ODR has been built;



Existing test system

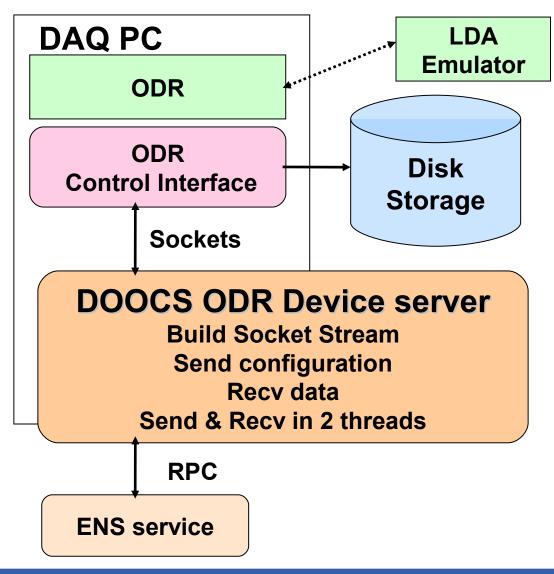
- Communication
 between different parts
 of DOOCS
 Server/Client by
 RPCs
- Configuration data & files are used when the system starts and runs:
 - ODR CTL s/w
 - ODR device server
 - ENS server





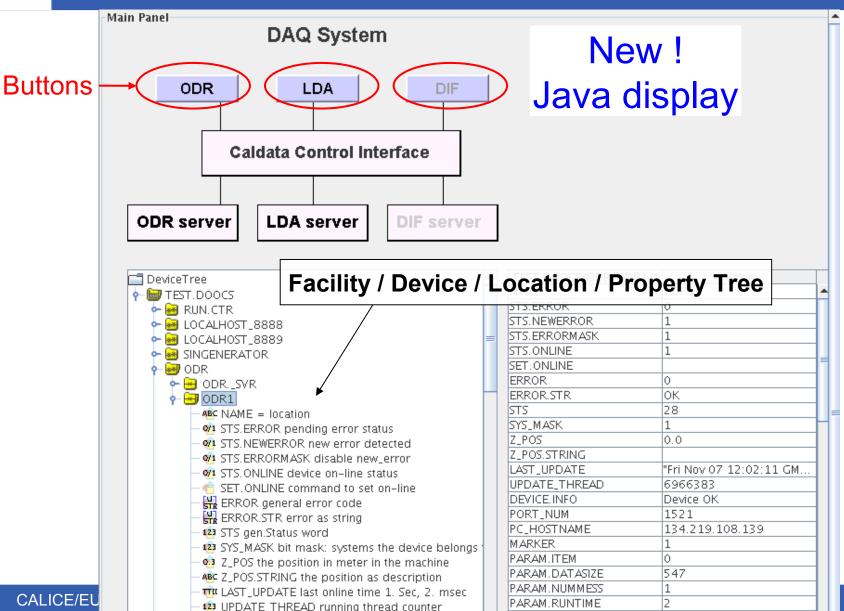
ODR device server

- One device server can serve many instances all connected via different ports and hostnames
- Using 2 threads: one for receiving, one for sending on the socket
- ODR control s/w
 - User-to-HD interface
 - Communication & I/O
- Sockets format is chosen to build an interface to the ODR and the LDA





Client GUI interface





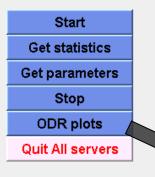
ODR Client interface

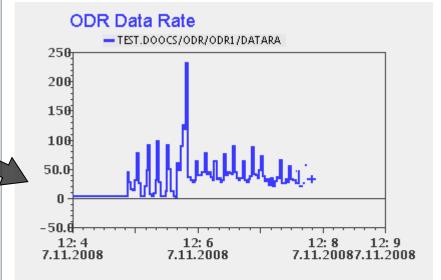
ODR parameters

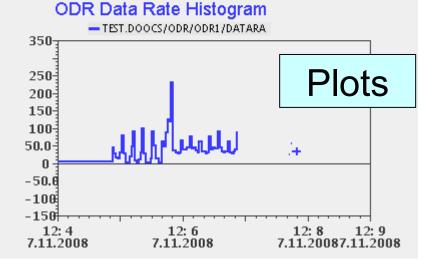
data size no of messages run time (s) dump to screen grouping no of IO Threads dump data to disk 0/1 dump data size word to extract DG:0 Network:1 actibe channels 0/1 No of DMA start data write event grouping DMA debug text next message statistics update freq run quit empty Send 1	•		
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text next message statistics update freq run quit	event grouping	0 ÷	send
statistics update freq run quit 0 - send quit 0 - send	DMA debug	0 ÷	send
run 0 send quit 0 send	text next message	0 -	send
quit 0 send	statistics update freq	0 -	send
quit - ; sem	run	0 ÷	send
empty 1 send	quit	0 -	send
	empty	1 -	send

TEST.DOOCS/ODR/O	Value	
PARAM.ITEM	0	٠
PARAM.DATASIZE	547	П
PARAM.NUMMESS	1	П
PARAM.RUNTIME	2	П
PARAM.DUMPSCR	0	П
PARAM.GROUP	10000	П
PARAM.IOTHREADS	1	П
PARAM.DUMPTOHD	1	=
PARAM.DUMPSIZE	10000000	П
PARAM. WORDEXTRACT	6	П
PARAM.DGNET	0	
PARAM ACTCHAN	0	

ODR Commands

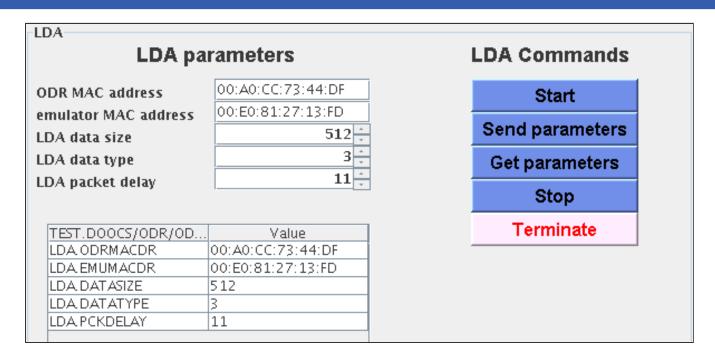








LDA Client interface



Commands are testing with new LDA emulator:

LDASTART
LDAConfig
LDASendConfig
LDASTOP
LDATERMINATE





Development strategies

- Strategies before full chain available:
 - use an LDA emulator instead;
 - Continue to develop the rest parts of software for DAQ system in parallel;
 - Get each part ready as far as we can;
 - Detect new & fix pending problems and investigate better designs meantime.

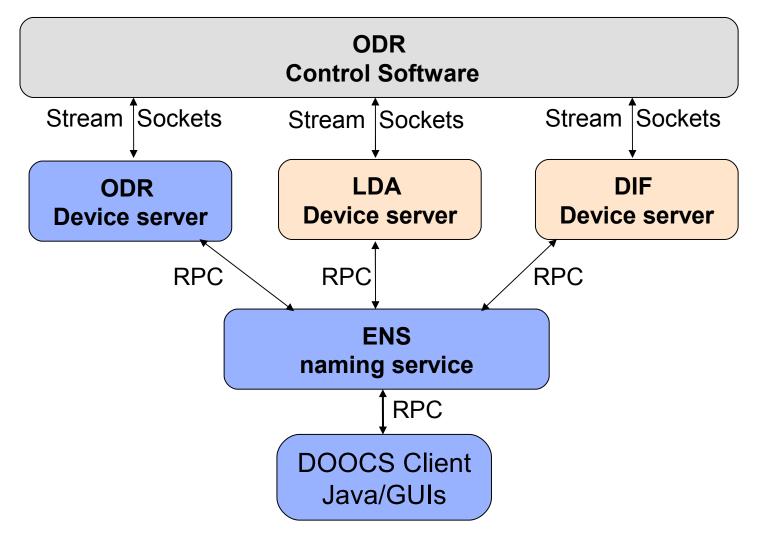


Task lists

Task	Status
ODR-LDA device server	Done
DIF, ASIC device server	Not yet
State Machine	Not yet
Data handling	Started
Error/Alarming handling	Started
Clock device server	investigating



Extendibility & integration of test system





Aim of the database

- Device database:
 - Connections between devices (ODR-LDA, LDA-DIF, DIF-DIF)
 - Starting parameters (e.g. port number, hostname)
- File database:
 - Host and path of file storage
 - Information about stored files
- Configuration database:
 - Static and volatile properties of all devices to be loaded
- All information related to make a RUN



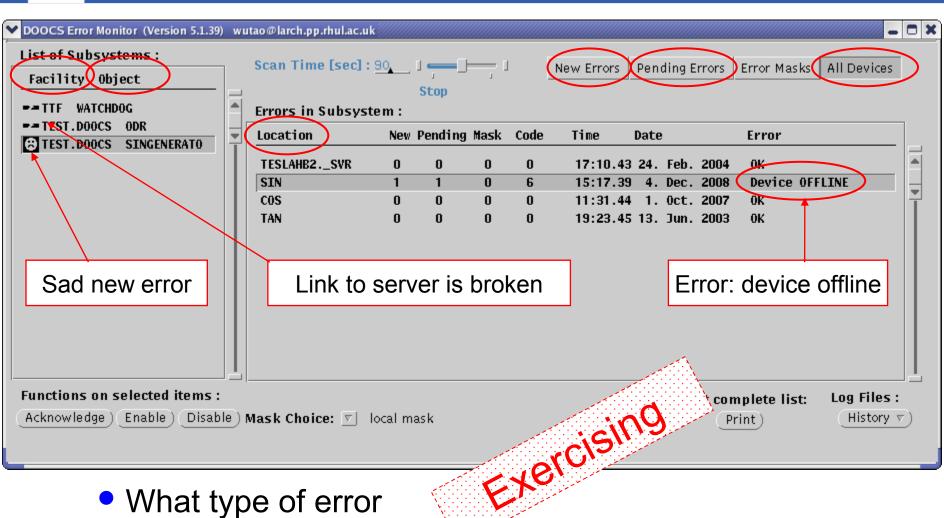
Current status of database

- Choice of database: MySQL;
- Entity diagrams has been made;
- Use cases has been made and evaluated;
- database is populated with mockup data;
- C++ connector wrapped by MySQL++ to be built in DOOCS framework. Optional solution!

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Error handling

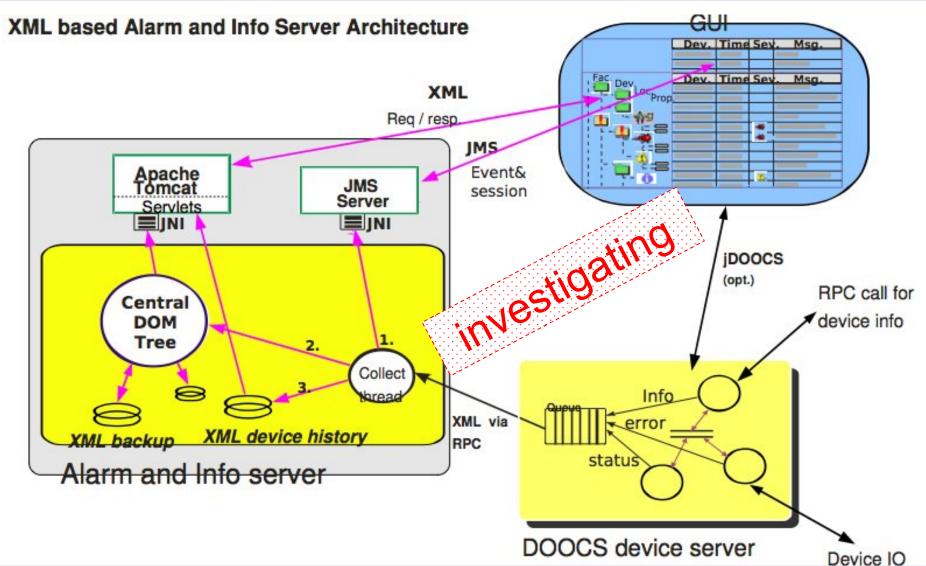


Its severity level

Some error types are defined.

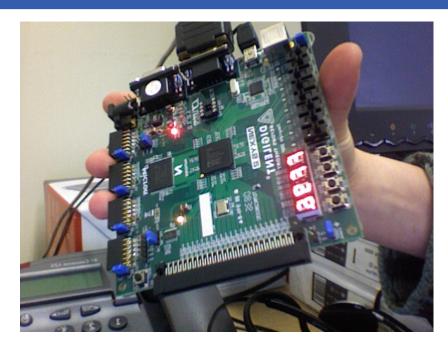


Alarming handling





Clock device server



- Simple hardware system to test with;
- No clock firmware to speak to yet, but
- Software sets registers
- Software handles device like a file
- Not yet integrate in a DOOCS device server

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Exercisin⁹

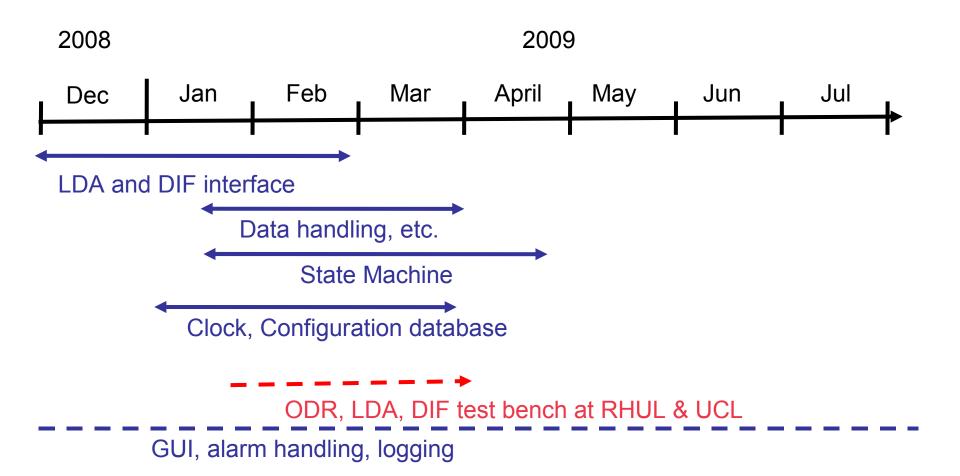


Some essentials

- The components are not integrated in software,
 - LDA / DIF / ASICs
 - Full chain will be available ~Jan/2009.
- No event building & LCIO converting
 - Data are saved to local disk in raw format;
 - Just provide interfaces in the framework;
 - More flexible way to leave them free for subdetector groups to develop.



Timeline estimation





Summary & Outlook

- Software has integrated ODR into DAQ system;
- Software has successfully managed communications and control tests;
- Some further progress ongoing:
 - Device server for other DAQ components;
 - Data handling
 - Error/Alarm handling
 - Clock device server
 - Full chain of DAQ components will be available Jan/2009.



Backup



ODR update

- Tests are ongoing trying to emulate bunch-train data which is saved in single file to disk.
- A list of alarms is being defined:
- 1) ODR not reachable.
- 2) Internal ODR-receiver alarms:
 - 2a) ODR card not detected.
 - 2b) Cannot initialise ODR card.
 - 2c) Cannot initialise ODR network interface.
 - 2d) Cannot allocate memory.
 - 2e) Cannot start "receive" thread.
 - 2f) Cannot start IO thread.
 - 2g) Cannot save received data/error saving data. 4c) LDA response corrupted.
 - 2h) Wrong virtual address of the data buffer.
 - 2i) Data error detected/DMA data corrupted.
 - 2j) Wrong data channel ID.
 - 2k) Unknown data page number FIFO data corrupted.
 - 2I) Error stopping "receive" thread.
 - 2m) Error stopping IO thread.

3) DOOCS own, ODR related alarms:

3a) No response from ODR.

3b) Unknown response from ODR.

3c) ODR response corrupted.

4) LDA related alarms:

4a) No response from LDA.

4b) Unknown response from LDA.

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