

Overview of DAQ status, C&C and ODR

Royal Holloway University of London

MANCHESTER

1824

Matthew Wing (UCL/DESY/UHH) for DAQ groups: Cambridge, Manchester, RHUL and UCL Slides from B. Green and M. Postranecky

Electronics/DAQ meeting, DESY, 12 December 2008



Outline

- Overview of DAQ system
- Overall status
- Immediate plans
- Clock and control card
- Off-detector receiver
- Summary
- (Bart will cover the DIF and LDA)
- (Tao will cover the software)



Overview of DAQ system

Detector Unit: ASICs

DIF: Detector InterFace connects generic DAQ and services

LDA: Link/Data Aggregator fansout/in DIFs and drives links to ODR

ODR: Off-Detector Receiver is PC

interface

CCC: Clock and Control Card fans out

to ODRs (or LDAs)

Control PC: Using DOOCS





Overall DAQ system status

- Prototype ODRs have been around for a while
- LDA had problems which are now fixed
- CCC tested and working
- Prototype ECAL DIFs have been around for a while
- Progress on use of DOOCS
- Work on links ongoing

All hardware ingredients exist and tested - now working on joining up and towards a full system test.



Immediate plans

- Testing links, writing firmware for full system test (next month)
- Then all components in one lab to get full system working
- Procurement of more components
- When is it useful for detector groups to have some parts or a full system?

UCL

Clock and control card - schematic AUTO / X-TAL SW-0 A) <u>CLOCK</u> LVDS on SMA EXT. **CLKI** OR LVTTL on Lemo Ν NIM on Lemo **MPX** +PLL ~ 50 MHz X-TAL B) FAST TRIG **SW-1** LVDS on SMA 2->1 C) <u>CONTROLS</u> . . . CPLD 4x LVDS on SMA 4x NIM on Lemo SW-2 :4x 5->1 LVDS on SMA SW-3 OR NIM on Lemo 2->1 4 o/c TTL on Lemo 8 6 PCB-1 HEADER / CONNECTOR MP + MW, UCL, 29-10-2007



Clock and control card

- Two prototypes tested and fully functional
- Firmware for tests written and more being developed
- A further eight boards are being ordered
- An operating manual is being written
- Interface to DOOCS being done







Off-detector receiver - DAQ PC





Off-detector receiver - DAQ PC status

• Firmware

o Stable, only control message extraction change pending o Available on CVS

- Software
 - o Stable, only control message extraction change pending
 - o Available on CVS
- Documentation
 - o Variable levels of completion
 - o Available on Twiki

UCL

Off-detector receiver - DAQ PC resources

- ODR programming manual
 - <u>https://www.pp.rhul.ac.uk/twiki/bin/view/CALICE/OffDetectorReceiver4Guide</u>
- ODR firmware description
 - <u>https://www.pp.rhul.ac.uk/twiki/bin/view/CALICE/OffDetectorReceiverFPGAFirmware</u>
- Caldata user guide
 - <u>https://www.pp.rhul.ac.uk/twiki/bin/view/CALICE/CaldataUserGuide</u>
- DAQ PC experts
 - <u>b.green@rhul.ac.uk</u>
 - <u>warren@hep.ucl.ac.uk</u>
 - <u>misiejuk@pp.rhul.ac.uk</u>
- Software & Firmware CVS
 - <u>http://isscvs.cern.ch/cgi-bin/cvsweb.cgi/Stage1/?cvsroot=caldaqwp2.5</u>
 - <u>http://isscvs.cern.ch/cgi-bin/cvsweb.cgi/ODR/software/?cvsroot=caldaqwp2.5</u>
 - CVS web access is only available to web browsers running within CERN subnet.



Summary

- All individual components now exist and work
- We must get all links working and plan to put the system together in January
- What would be useful for detector groups and when? Parts of or all system?
- It would be good to have a list and so we can plan and purchase



Extra details

C&C: Top of the PCB silk :

http://www.hep.ucl.ac.uk/~mp/CALICE_C-C/CALICE_C-C_pc3405m1-J_Top-Silk_28-08-2008.pdf

C&C: Top of the PCB assembly schematic :

http://www.hep.ucl.ac.uk/~mp/CALICE_C-C/CALICE_C-C_pc3405m1-K_Top-Assembly_29-08-2008.pdf

C&C: Complete Circuit Schematics :

http://www.hep.ucl.ac.uk/~mp/CALICE_C-C/CALICE_C-C_pc3405m-1aa-K_Schematics_29-08-2008.pdf