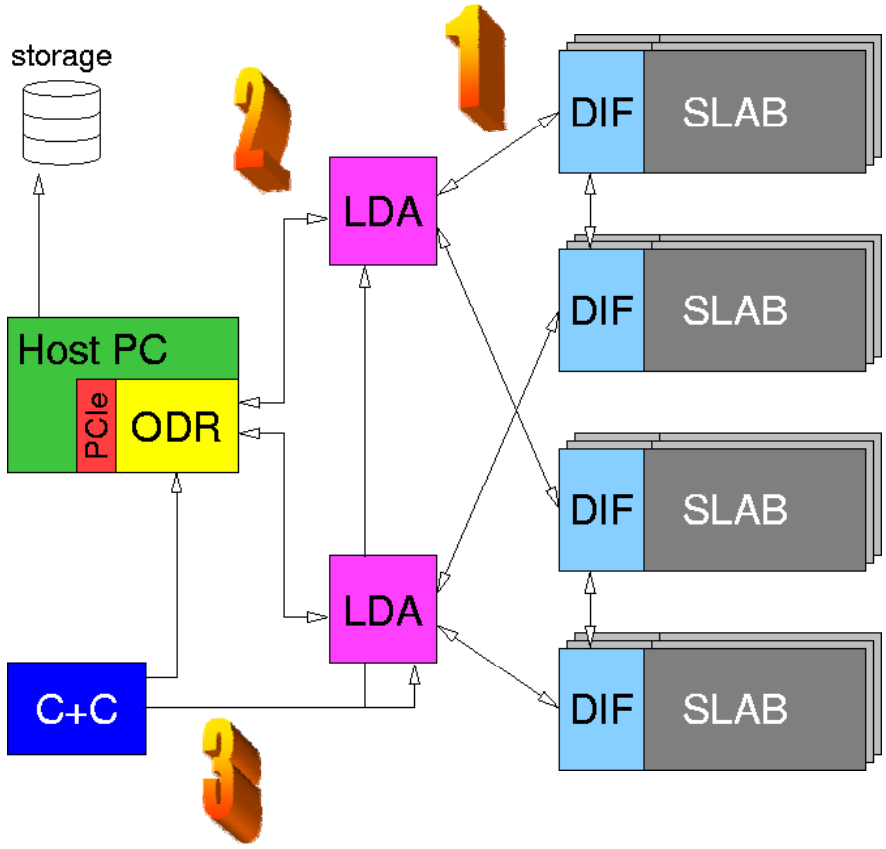
CALICE (ECAL) / EUDET DAQ: DIF and LDA Status

Marc Kelly, Maurice Goodrick, Bart Hommels

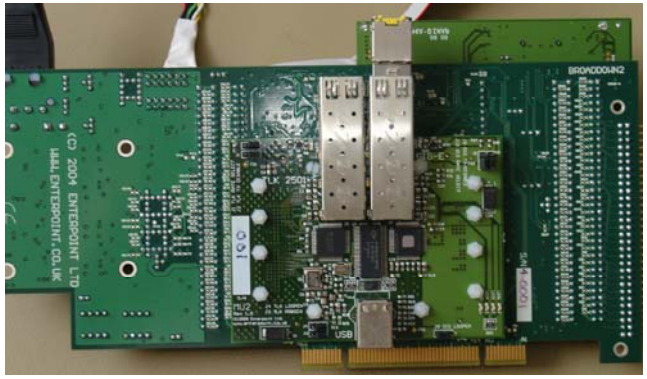
Reminder: links in the DAQ System

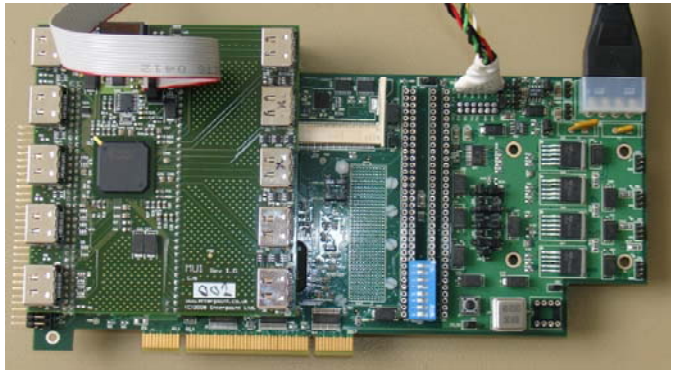
1. DIF ⇔ LDA
   - synchronous, serial link with additional asynchronous pairs. 8B/10B encoded data
   - runs at N*machine clk: frequency 5..150MHz (assume 100MHz)
   - HDMI cabling and connectors
2. LDA ⇔ ODR
   - Gigabit Ethernet (and TLK2501) serial protocol
   - SFP cage connector supports optical fibre
3. C+C ⇔ LDA
   - Compatible with LDA⇔DIF interface
   - C+C & DIF capable of stand-alone operation



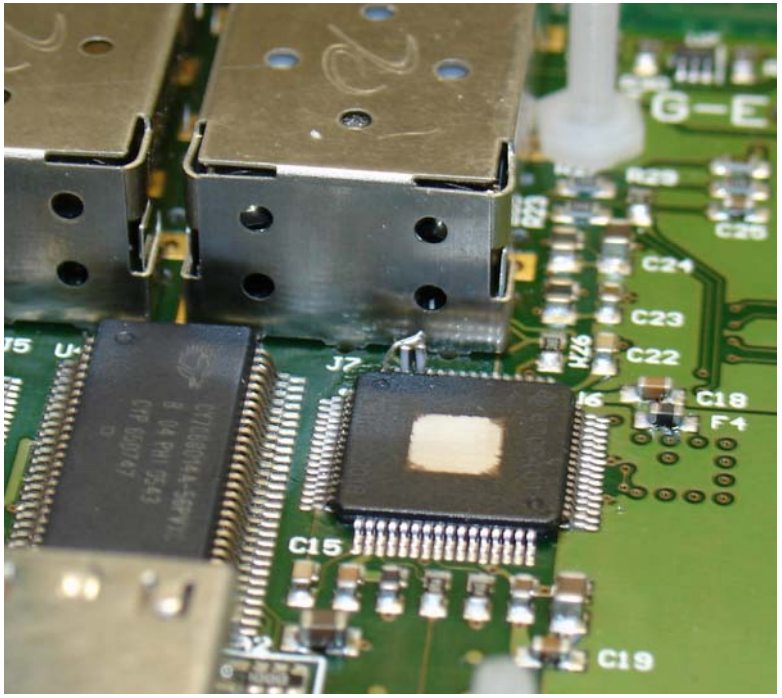
LDA Hardware

M. Kelly
(Manchester)

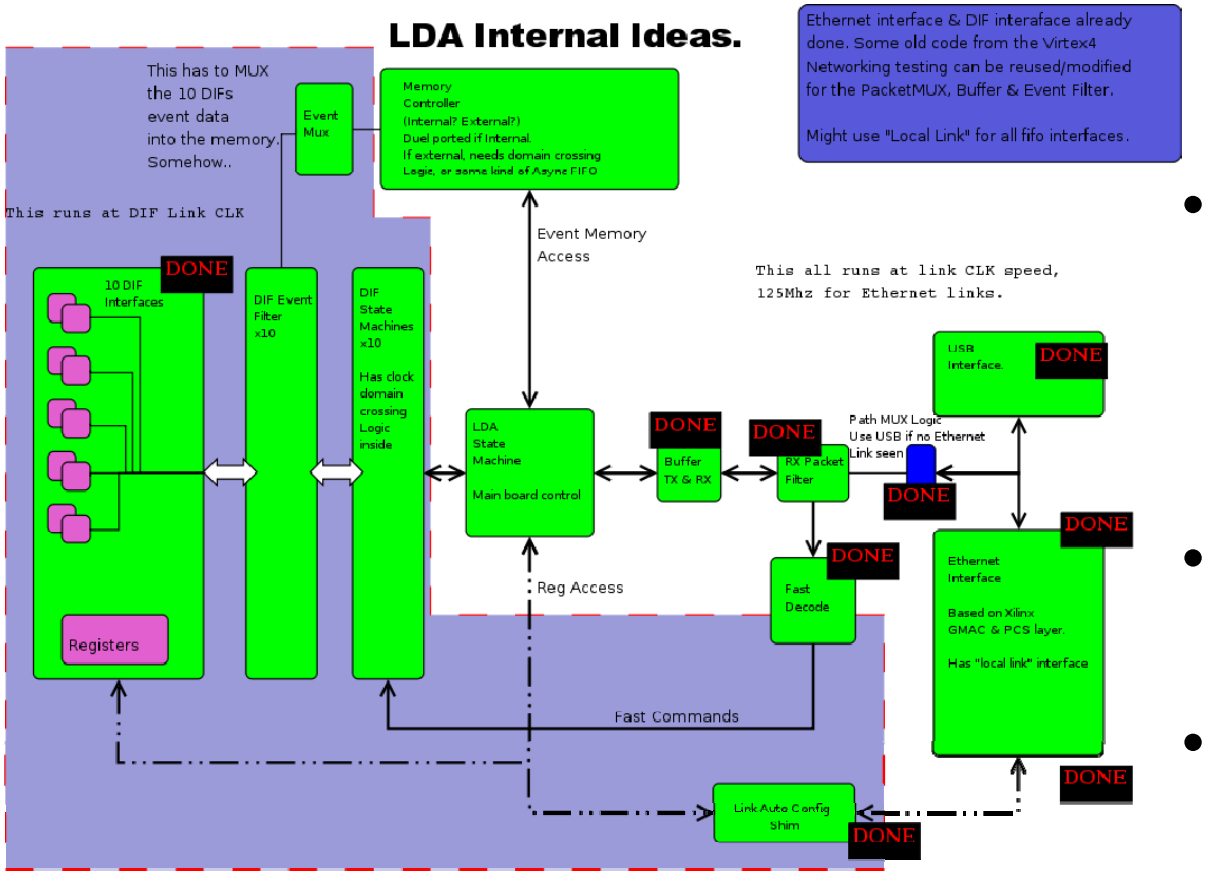




- LDA hardware: Broaddown2 baseboard with Gbit-Eth add-on and DIF links add-on
- Resolved many hardware issues
- Latest fix: terminator resistors on Gbit Eth board
- Hardware works now (!)



LDA Firmware



- While struggling with hardware: good firmware progress
- Gbit Eth now up&running: auto-negotiates link and subsequently sends packets through Ethernet switch
- LDA-DIF interface ready, debugging (partly?) done
- DIF-side of link firmware ready as well

Documentation available on web: http://www.hep.manchester.ac.uk/u/mpkelly/calice/lda/Calice_LDA_Overview.html

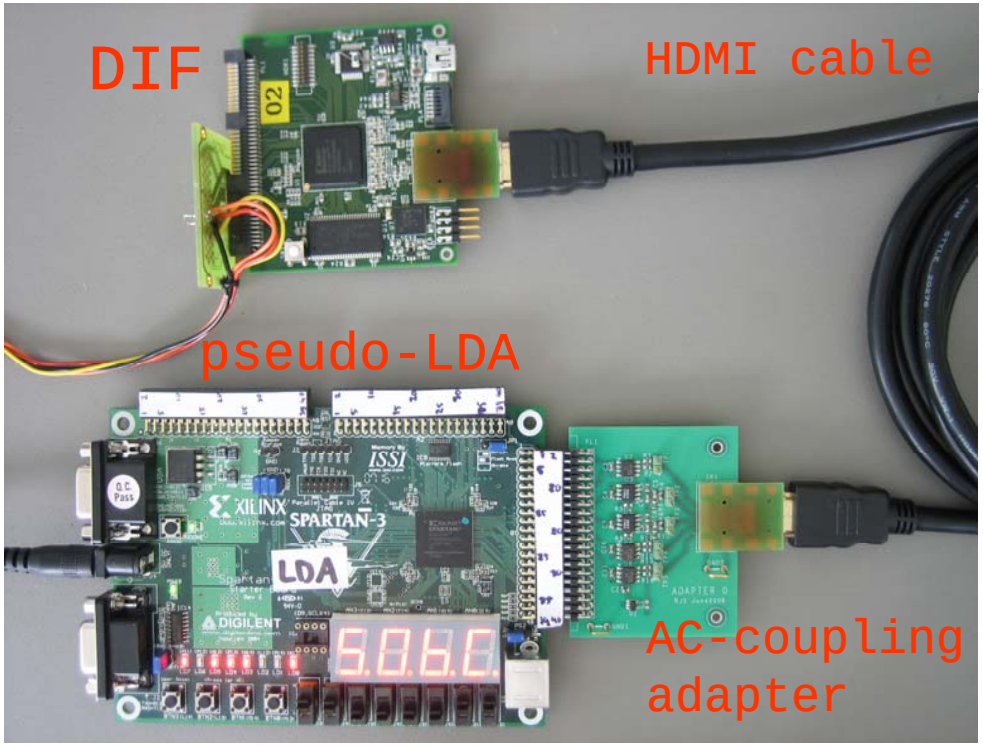
DIF, and DIF-LDA link status

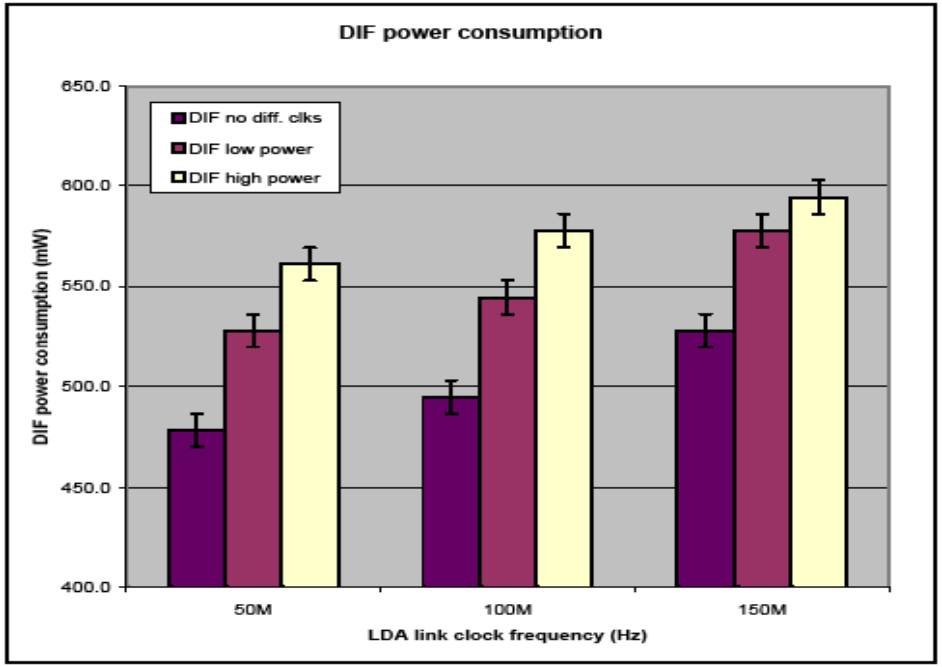
M. Goodrick, B. Hommels (Cambridge)

- 5 DIFs produced, parts available for 5 more.
- DIF hardware is (at least partly) functional

LVDS over HDMI link test:

pseudo-LDA sends CLK & 8B/10B data @ 100MHz over AC-coupled LVDS lines

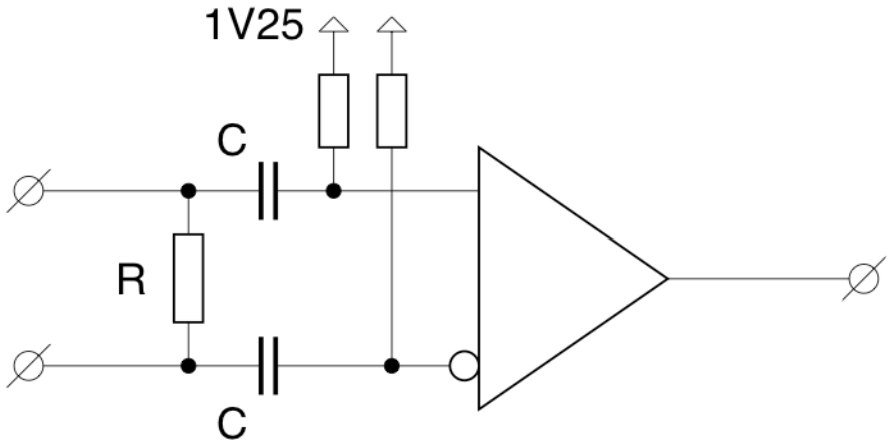


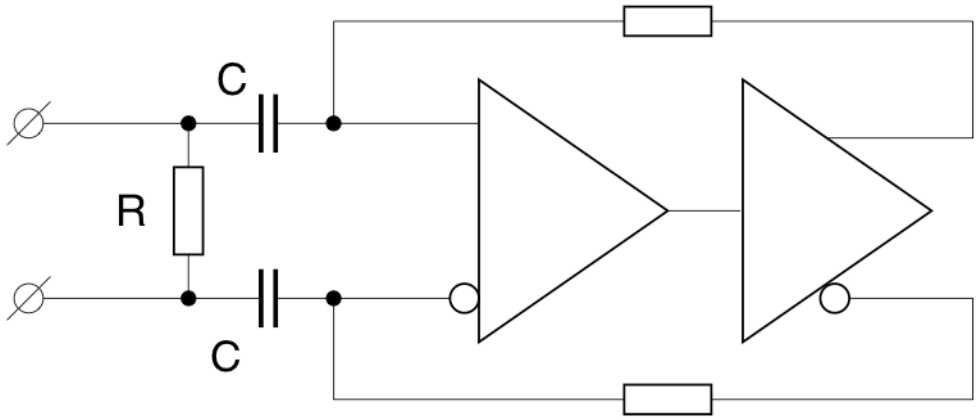


Power consumption vs. link frequency: relatively small power penalty from 50MHz=>150MHz

DIF-LDA link: AC-coupling

- ‘Traditional’ AC coupling is OK for clocks, but not for data.
- Long absence of transitions leads to link being ‘blind’ to first few bits arriving
- Solution is to use a feedback system: edge-detector or bus keeper
- Works well, but needs tuning of RC time constant w.r.t transmission frequency
- Continuous sending of idle characters might circumvent the issue altogether

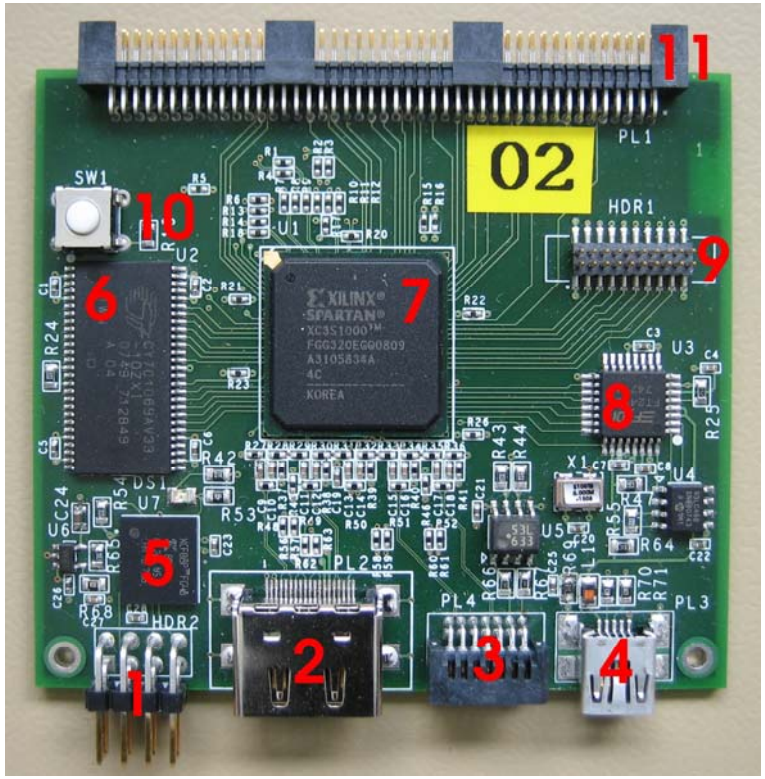




DIF hardware: plans

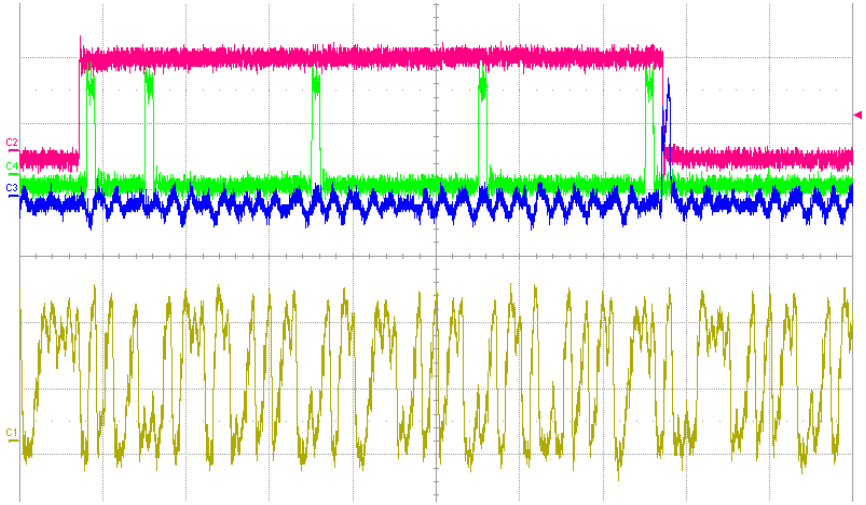
DIF re-spin for EUDET readout, should have smaller form factor.

- No external SRAM (6)
- No user connector (9)
- No reset button (10)
- No USB? (4, 8)
- SPI-flash PROM (5)
- Flash RAM for VFE config
- Include advanced AC-coupling option (2)
- Probably smaller FPGA (7)

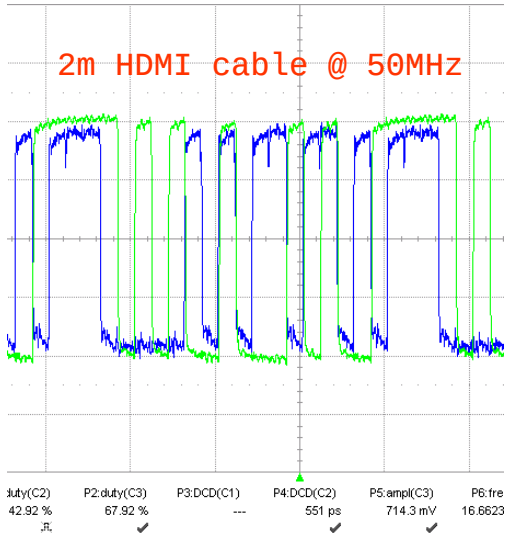


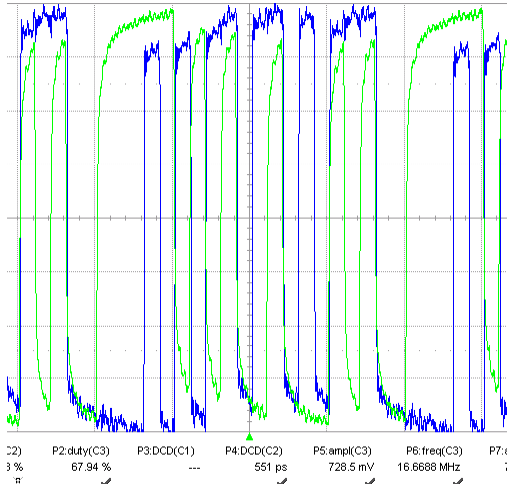
DIF firmware status

- DIF firmware test bench: Pseudo-LDA with clock generation, full-duplex 8b/10b data transmission machinery
- DIF running link firmware as development platform for DIF firmware.
- Initial task: send pseudo-data packets for DAQ system test



First
–and very primitive-
data transmission from
dev. DIF to LDA





DIF ⇔LDA link protocol

DIF ⇔ LDA protocol layer:

Mathias took initiative to start ‘user guide’ writeup ☺

Lively exchange of emails within DIF WG resulted in draft.v7. For further details: see Mathias’ talk

DIF next steps:

- Implement minimal set of DIF commands in firmware for DAQ test
- Extend firmware towards full DIF command functionality