News from the 1m^2 GRPC SDHCAL

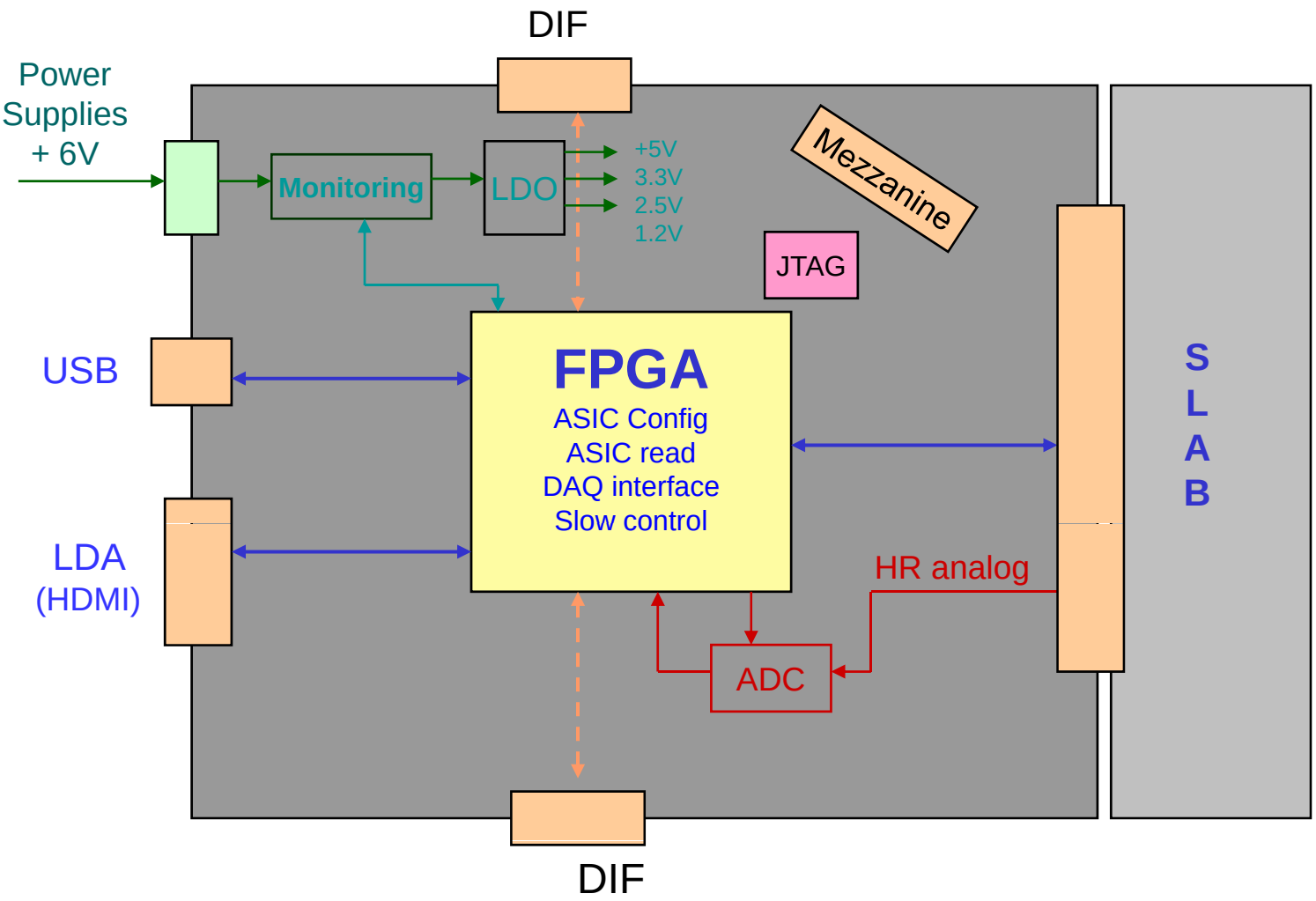
collection of slides from :

Ch.Combaret, I.L, H.Mathez, J.Prast, N.Seguin, W.Tromeur, G.Vouters
and many others

The DHCAL DIF Board

- Based on a Cyclone 3 Altera FPGA (EP3C6F484).
- Separated from the slab for more flexibility.
  - Can handle slab what ever the nb of HardRoc on it.
  - DIF task force interface compliant.
  - MicroMegas and RPC detector compatible.
  - HardRoc, Lyon's asics and also Spiroc and Skyroc compatible.
- On the DAQ side, interface with :
  - The LDA (final DAQ).
  - PC through USB for standalone tests and debugs.
  - DIF neighbors.
  - Interface with the analog DAQ removed.

Architecture of the DIF Board

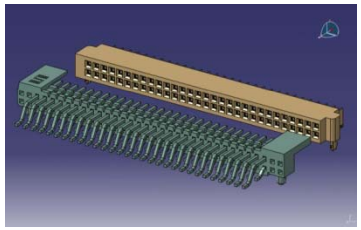


GND	1		2	GND
MUX3_CSn	3		4	Analog_0
MUX2_CSn	5		6	GND
MUX1_CSn	7		8	Analog_1
spare1	9		10	GND
MUX_ENN	11		12	C_test
MUX_WRN	13		14	GND
spare2	15		16	MUX_A4
en_otaq	17		18	MUX_A3
GND	19		20	MUX_A2
SR_reset	21		22	MUX_A1
hold	23		24	MUX_A0
spare3	25		26	Ramfullext
SR_IN	27		28	Reset_BCID
spare4	29		30	GND
SR_OUT	31		32	Resetn
spare5	33		34	Start_Conv_daqb
SR_clk	35		36	End_Readout
GND	37		38	Start_acq
TransmitOn_3	39		40	RamFull
Pwr_analog	41		42	Dout_3
TransmitOn_2	43		44	GND
Pwr_dac	45		46	Dout_2
Pwr_ss/Pwr_sca	47		48	Start_Readout
GND	49		50	Trig_ext
TransmitOn_1	51		52	Start_Readout_Bypass
Pwr_digital	53		54	Dout_1
TransmitOn_0	55		56	GND
Pwr_adc	57		58	Dout_0
SC_SROUT	59		60	SC_SRIN_BYPASS
SC_SROUT_BYPASS	61		62	SC_SRIN
SC_select	63		64	SC_reset
SC_clk	65		66	SC_load
User_LVDS_P	67		68	User_LVDS_N
Trig_Ext_P	69		70	Trig_Ext_N
DVDD	71		72	AVDD
Clk_5MHz_0_P	73		74	Clk_5MHz_0_N
Clk_5MHz_1_P	75		76	Clk_5MHz_1_N
GND	77		78	GND
Clk_40MHz_0_P	79		80	Clk_40MHz_0_N
Clk_40MHz_1_P	81		82	Clk_40MHz_1_N
DVDD	83		84	AVDD
Raz_Chn_P	85		86	Raz_Chn_N
Val_Evt_P	87		88	Val_Evt_N
AVDD	89		90	AVDD

SLAB Interface

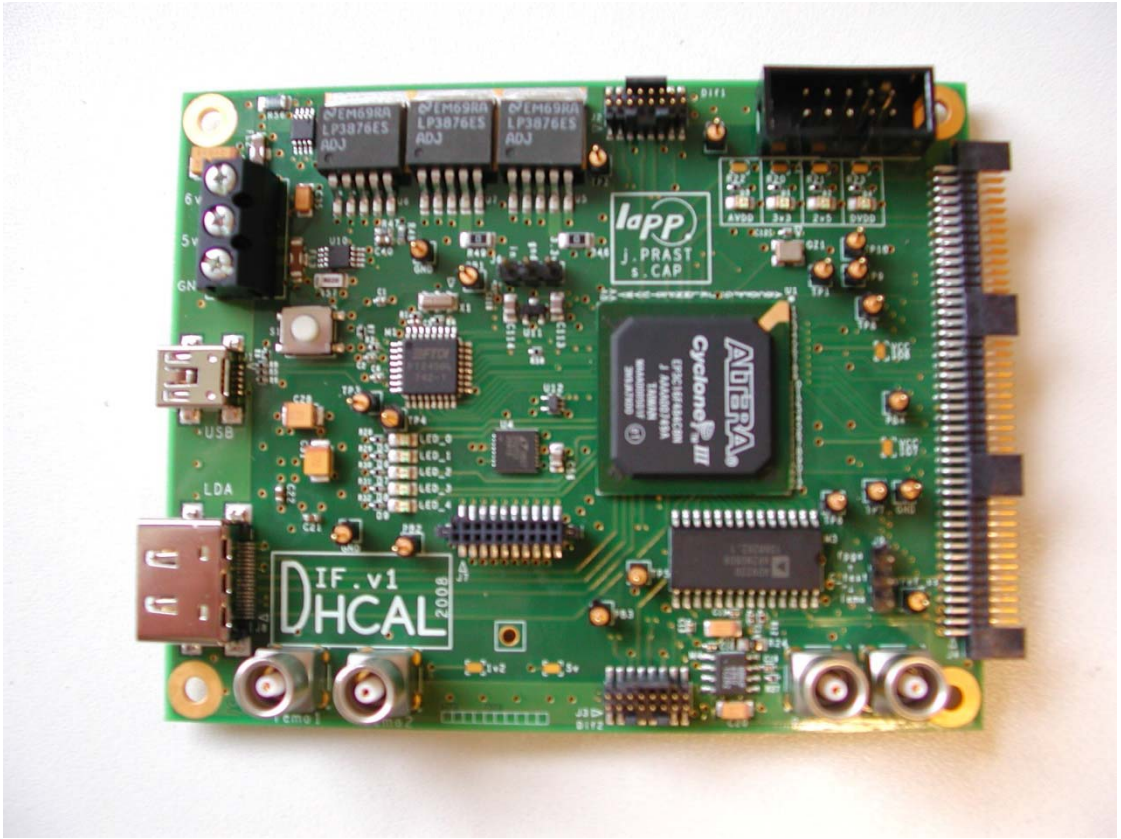
The connector has been designed for DHCAL but also ECAL or AHCAL

So the DHCAL DIF can also be used for ECAL or AHCAL !



Samtec FSH/ SFMH 90 pin connector

The DIF Board



1 m^2 PCB MAIN SPECIFICATIONS

ASU PCB Design

- 24 x 64 1 sq cm pads
- 24 Hardrocs Asics chained

1 m2 PCB board :

- 6 ASUs
- 144 Hardroc Asics

DIF boards :

- 1 DIF for 1 ASU : 6 DIFs
- 1 DIF for 2 ASU : 3 DIFs

<u>Buffered Signals</u>

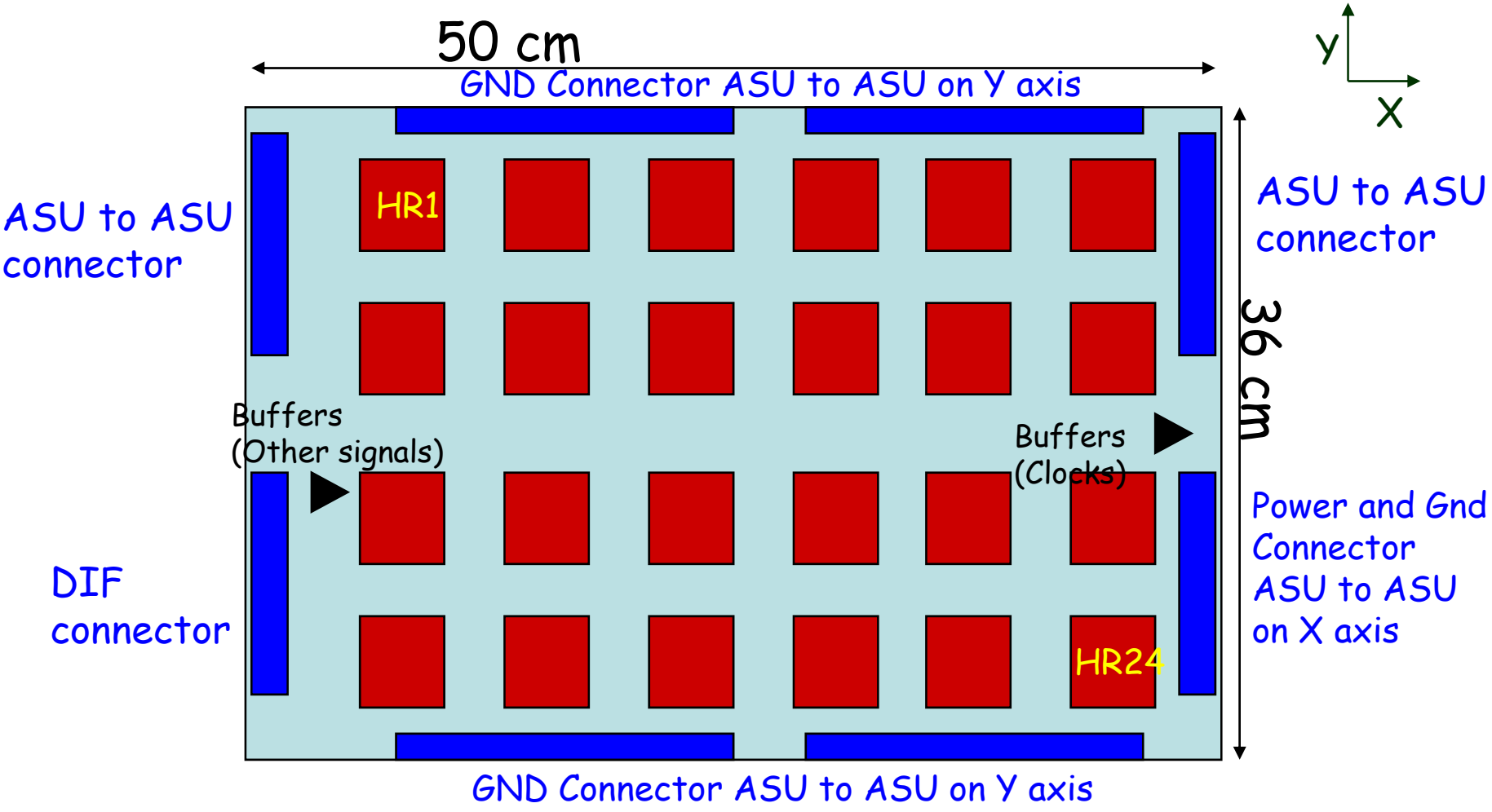
(Long Lines 1 m for Clock on 1 ASU):

- Slow Control
- Power_on
- Control for Analog Readout
- Digital Readout

<u>Analog Readout :</u>

- All OUT_Q are connected together
- EN_OTAQ switch on or off using DIF board and decoder

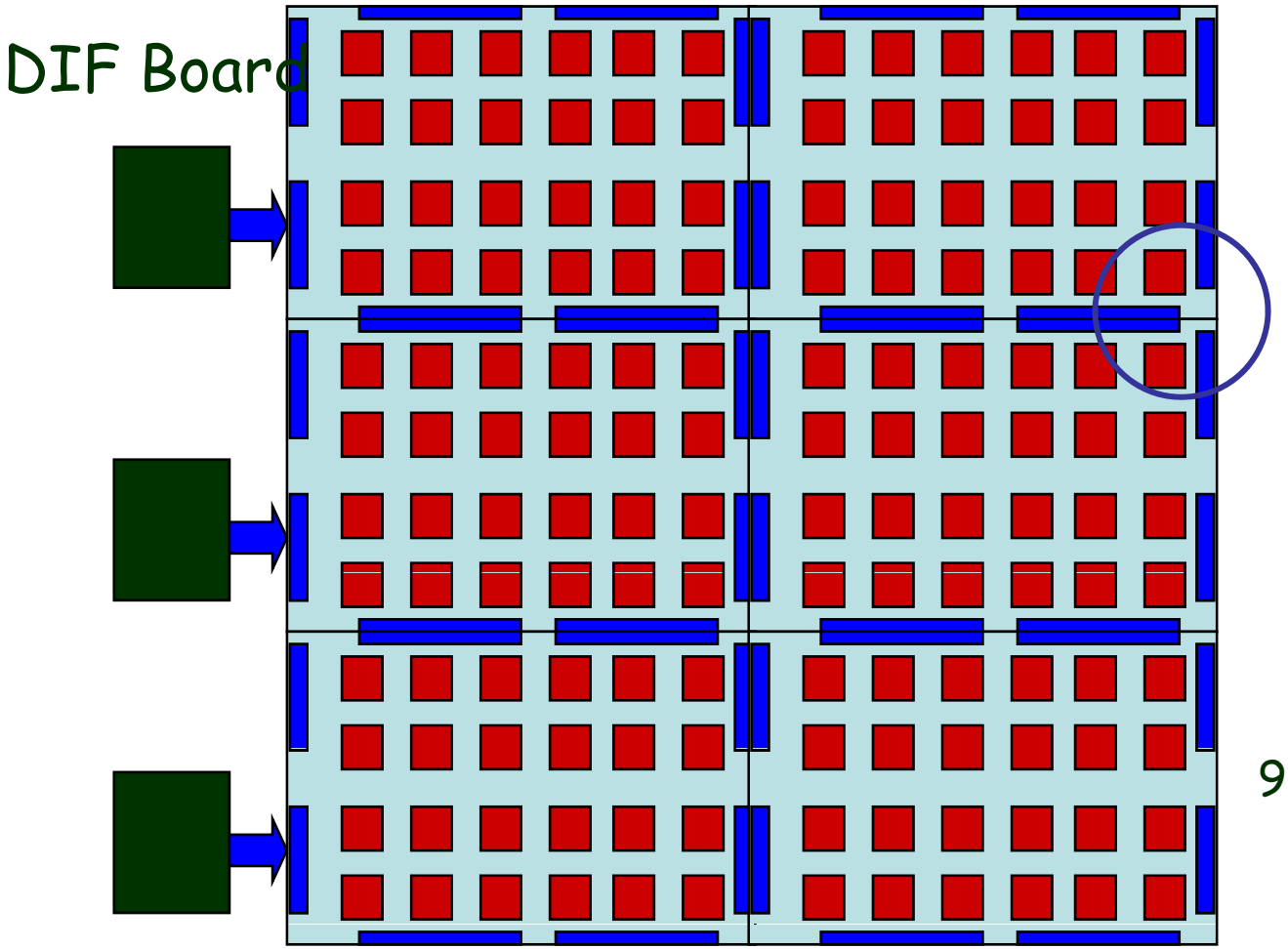
ASU PCB DESIGN



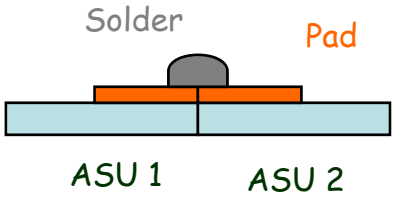
Buried and Blind Vias (Same as the last PCB with 4 HR)

1 m^2 PCB DESIGN

1 DIF for 2 ASUs



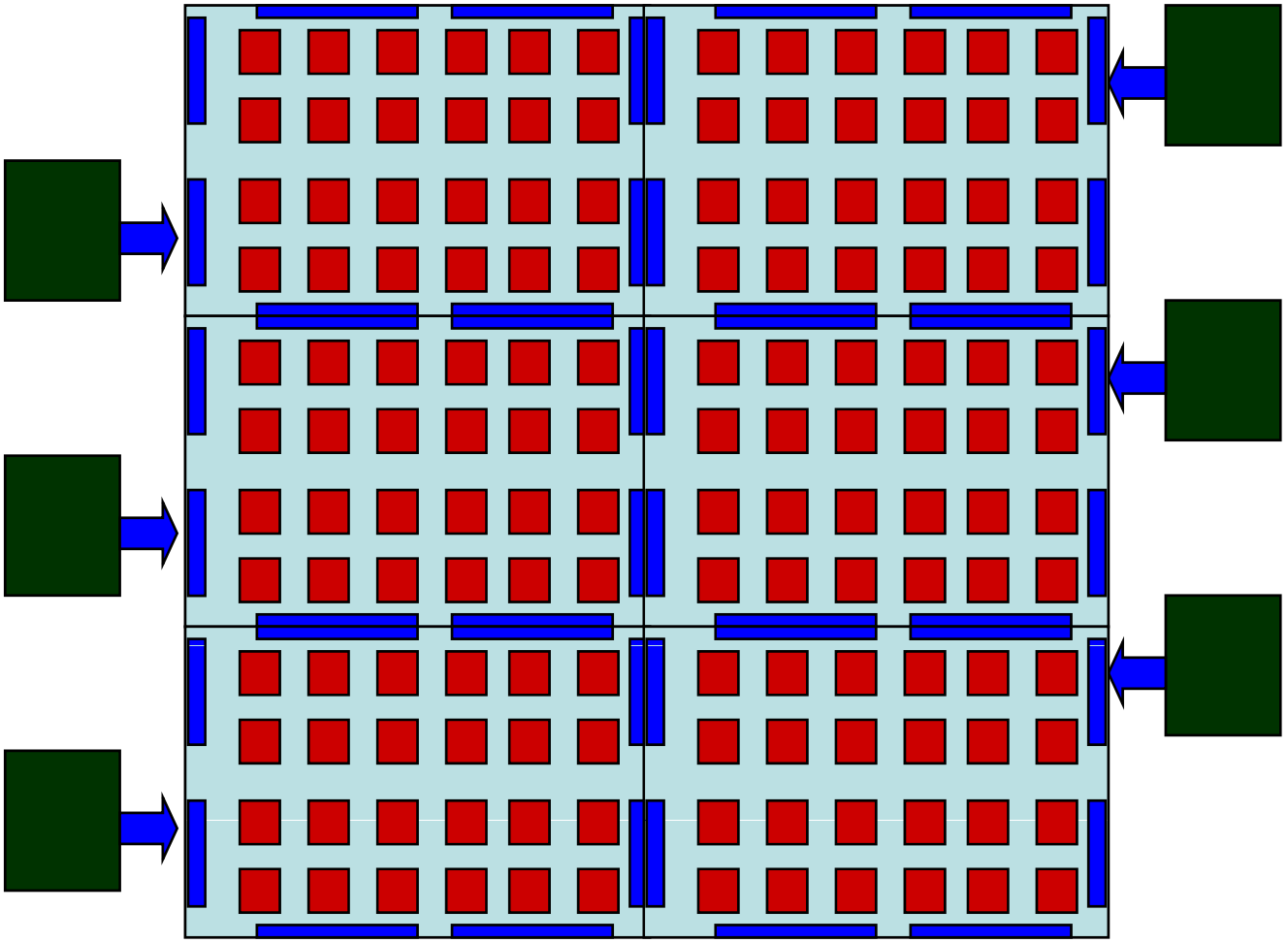
ASU to ASU Connection



9216 pads on Bottom Layer

1 m² PCB DESIGN

1 DIF for 1 ASUs

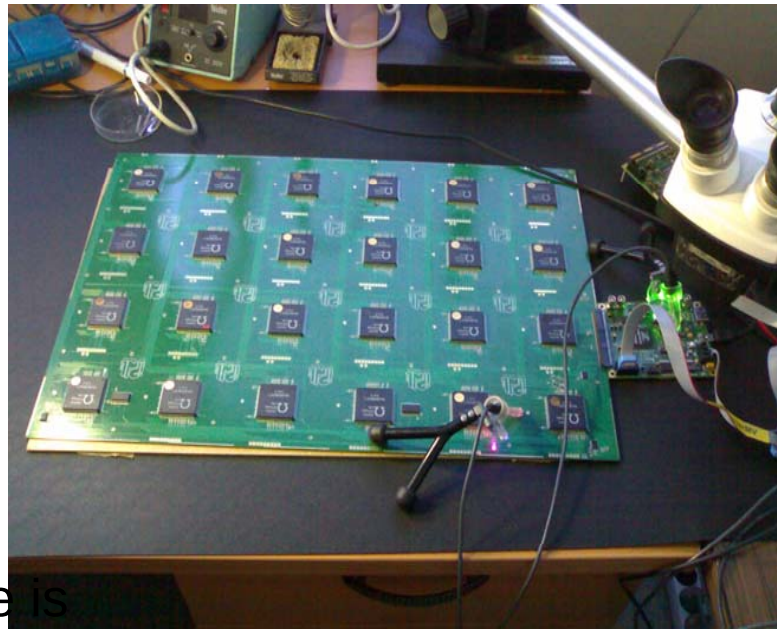


1 m^2 PCB DESIGN (Layers)

- Layer 1 (TOP) : interconnect
- Layer 2 : interconnect
- Layer 3 : 3.3V Digital
- Layer 4 : GND
- Layer 5 : 3.5V Analog
- Layer 6 : PADs to Hardroc
- Layer 7 : GND
- Layer 8 (BOTTOM) : PADs

Pads to Hardroc interconnects are the same for the entire PCB (hierarchical design)

Present Status

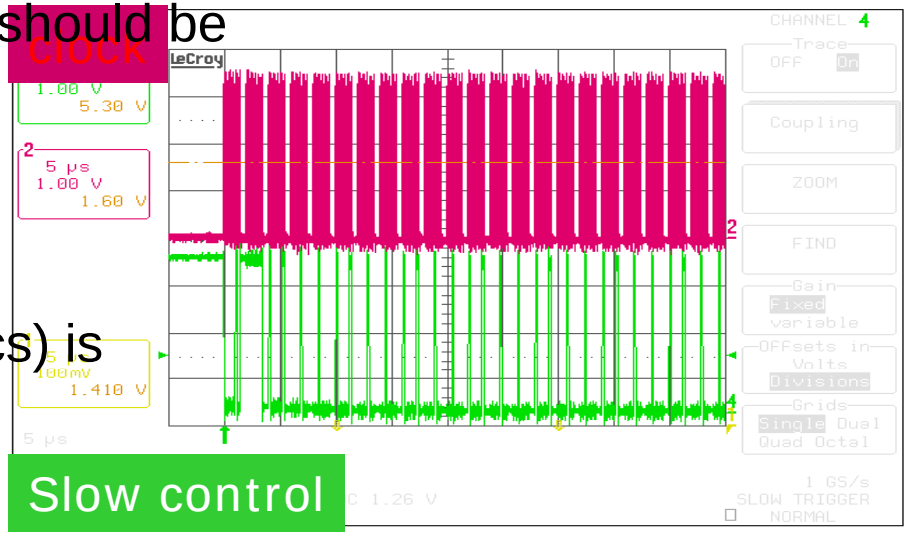


- DIF command and register access use XDAQ software
- DIF is fully functionnal

- The tested slab is fully functionnal with following modifications :
  1. Use of buffers on the SLC clock line is mandatory (max nb of hardrocs chained without buffer could not exceed 12)
  2. Use of buffers on the Open drains readout lines

  (transmit_on, dout and ramfull) should be forseen for next slabs

- Slow control (tested in all hardrocs) is stable and reliable
- Data readout is



Present Status

What was tested :

- Numerical readout has been tested in the following modes :

1. Manual Start Acquisition/Manual Start Readout (Manual Trigger
2. Manual Start Acquisition/ Automatic Start Readout (Internal Trigger)
3. Automatic startAcquisition/ Automatic Start Readout (« Beam test mode

-Both DIF firmware and XDAQ software stable and reliable

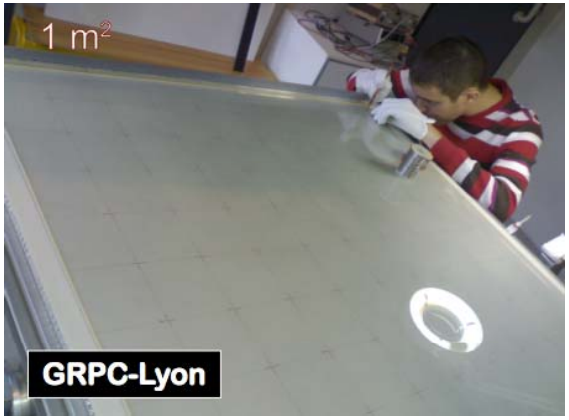
-Both DIF Firmware and XDAQ software have been tested with trigger rate >1kHz and 128 events per trigger

(DAQ levels < noise level)

-DIF temperature and current consumption monitoring on all DIFs

Present Status

We have started tests with cosmics using one slab and step by step we will equip the 1M^2 GRP with the 6 slabs (all now equipped with tested HR1)



We hope the fully equipped 1M^2 GRPC will be running very soon