Status of SPIROC 2

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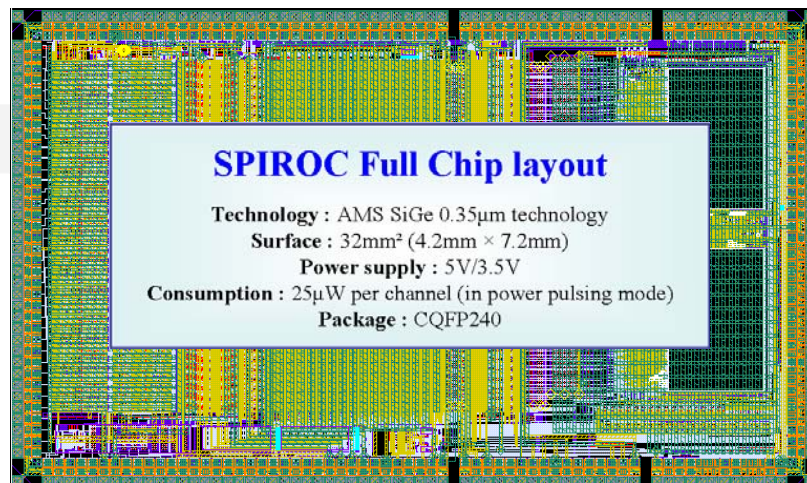Orsay MicroElectronic Group Associated

SPIROC 2 : Reminder

- Status of SPIROC1
    - 2 major bugs which need to be corrected : probe register and ADC
    - Analog part OK, can be used to replace FLC_SiPM
    - Autotrigger at ~50-100 fC
    - Could be tested with existing detector and DAQ
    - Can be used to emulate SKIROC

    A second iteration was necessary : SPIROC 2

- SPIROC2 prototyped in june 2008

SPIROC Full Chip layout

Technology : AMS SiGe 0.35µm technology
Surface : 32mm² (4.2mm × 7.2mm)
Power supply : 5V/3.5V
Consumption : 25µW per channel (in power pulsing mode)
Package : CQFP240

- Correction of the first version bugs (ADC discri, probe and slow control register)
- Add some light improvements (in digital part)

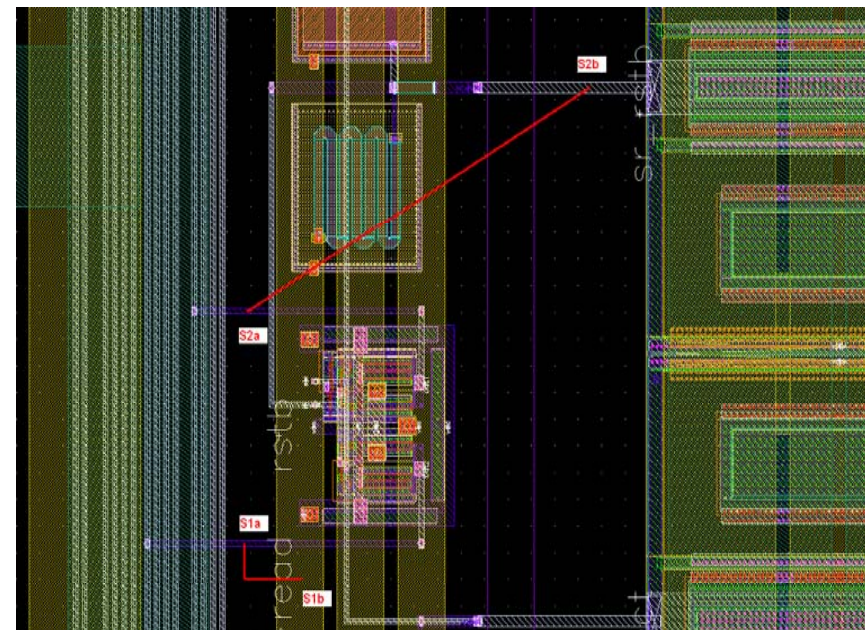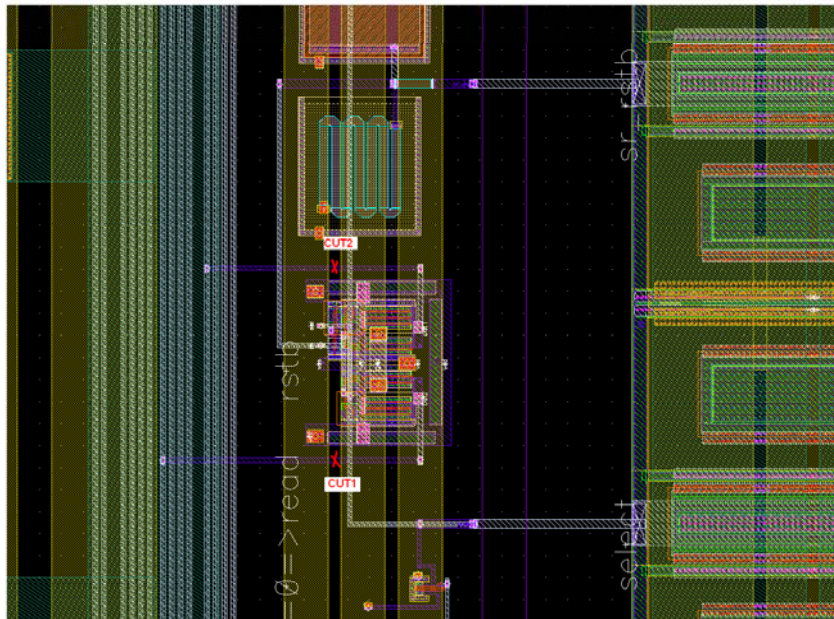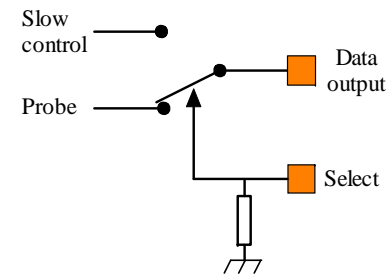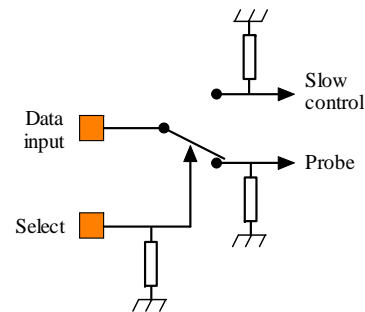Submitted on 9th june 2008

Delivery in October 2008

- **Bug on the reset signal of the new multiplexed probe and slow control register**
  - **Active low reset forced to 0 when not selected**
  - **Intempestive reset when register is unselected**
  - **Same problem on Hardroc 2**

- **Correction by SERMA Compagny : FIB (Focused Ion Beam)**

Spiroc 2 slow control and probe register

- Problem of synchronisation between DATA and Clock during the propagation in the register

- This problem seen on SPIROC 1 probe register was supposed to be resolved in this second prototype with a new clock distribution in the ASIC layout

- Possibly due to parasitic resistance and capacitance on the clock

- Problem resolved with an ad hoc fix for the slow control but not yet for the probe register by decreasing power supply to 1,5V during the loading phase

- Further investigations necessary to understand clearly

Preliminary measurements

- As expected, similar analog performance as the first prototype
  - Gain
  - noise
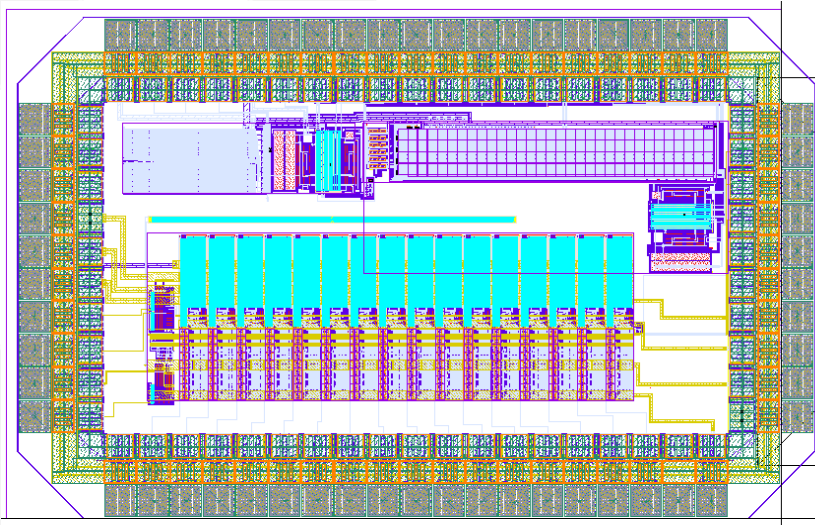 - Ultra-low power input 8-bit DAC
  - Threshold 10-bit DAC
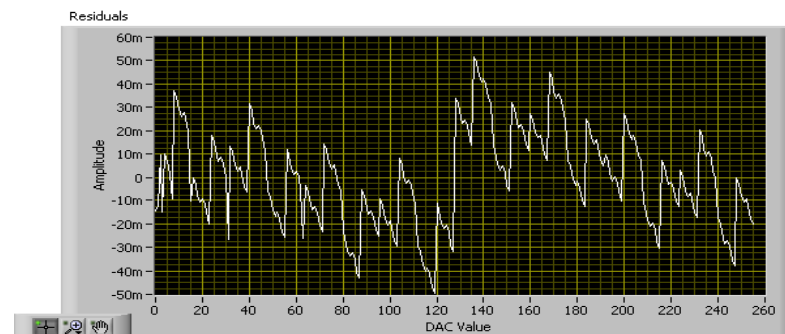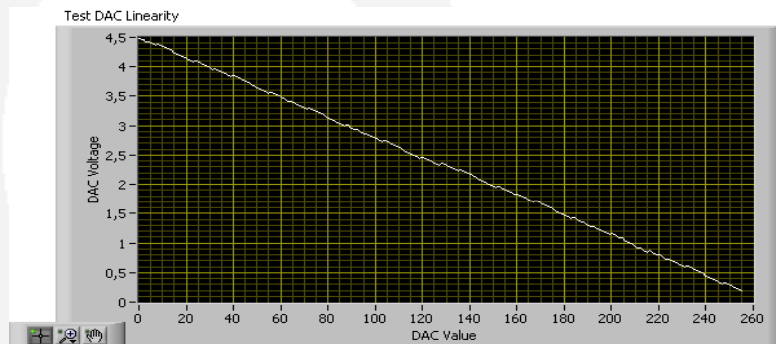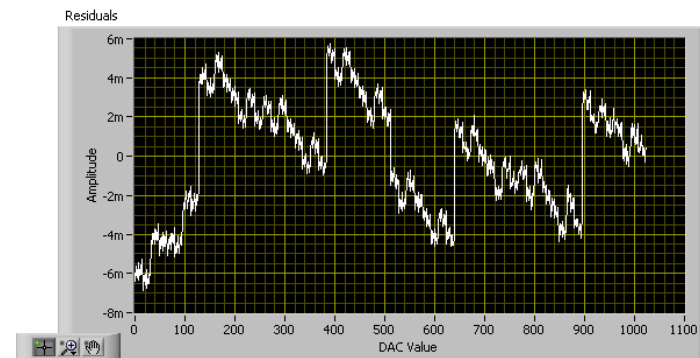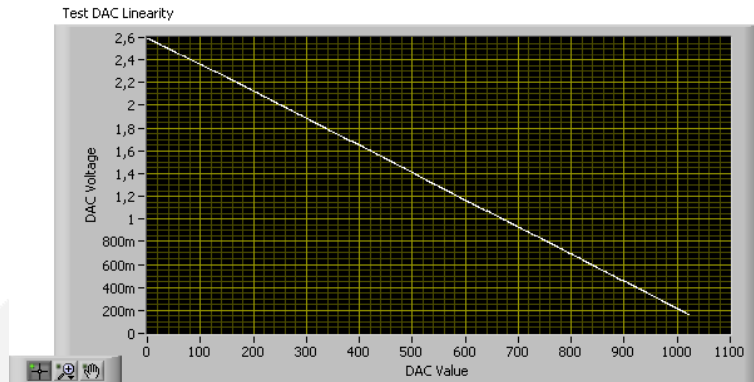
Extended measurements to be performed to validate features like ADC, autotrigger, TDC, power pulsing, etc.

Future improvement

- « Building block » funded by IN2P3 submitted last month
  - Improved 12-bit DAC for the threshold trigger
  - 16 8-bit low power input DAC

- Improved performance (linearity, uniformity channel by channel) expected with a new layout rearrangment for a better matching

- Will be implemented in the next chip if OK
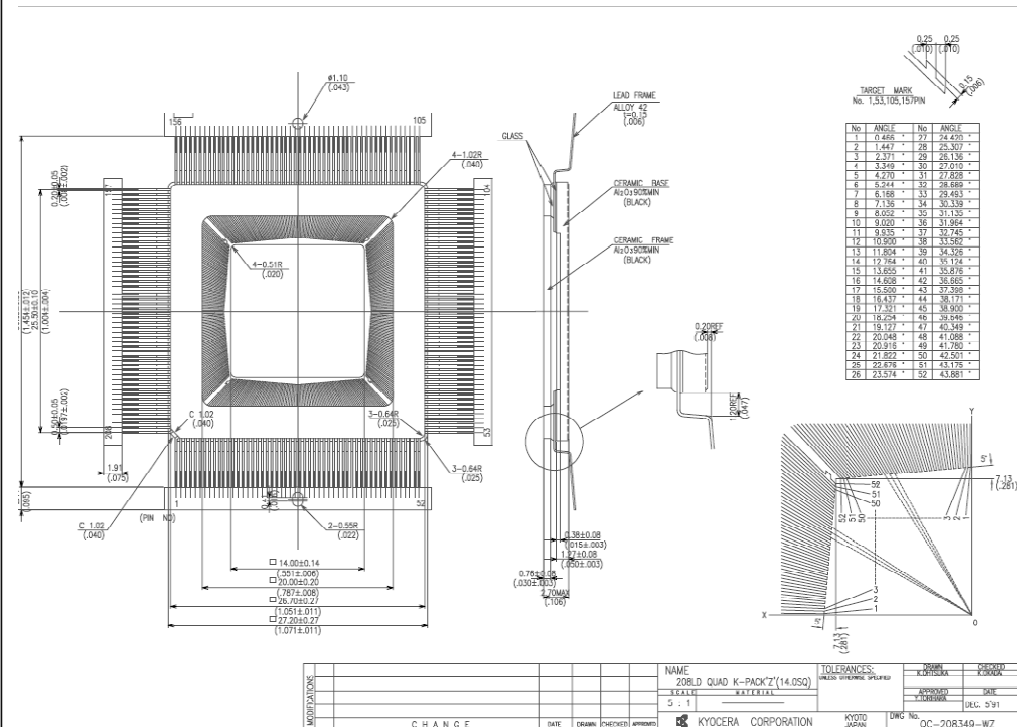
Submitted in November 2008

Delivery in January-February 2009

206 pads to connect

Packaging:

US compagny : I2A

Cost : 3k euros

Best candidate for the production : TCQFP208 (plastic packaging)

Dimensions: 27x27x1.4 mm

Conclusion

- SPIROC 2 chip
  - Very conservative prototype with normally correction of the first version bugs (ADC discri, probe and slow control register) and adding some light improvements (in digital part)

  - New bugs on the slow control and probe register can be circumvented to operate the chip

  - The very first measurement result gives similar results as the first prototype, but it is now essential to perform extended measuremts to see if the chip can be used for the EUDET prototype (ADC performance, auto-trigger, power pulsing)

  - Chip in final package: TQFP 208

  - Next chip will go with the hardroc engineering run (Summer 2009?)