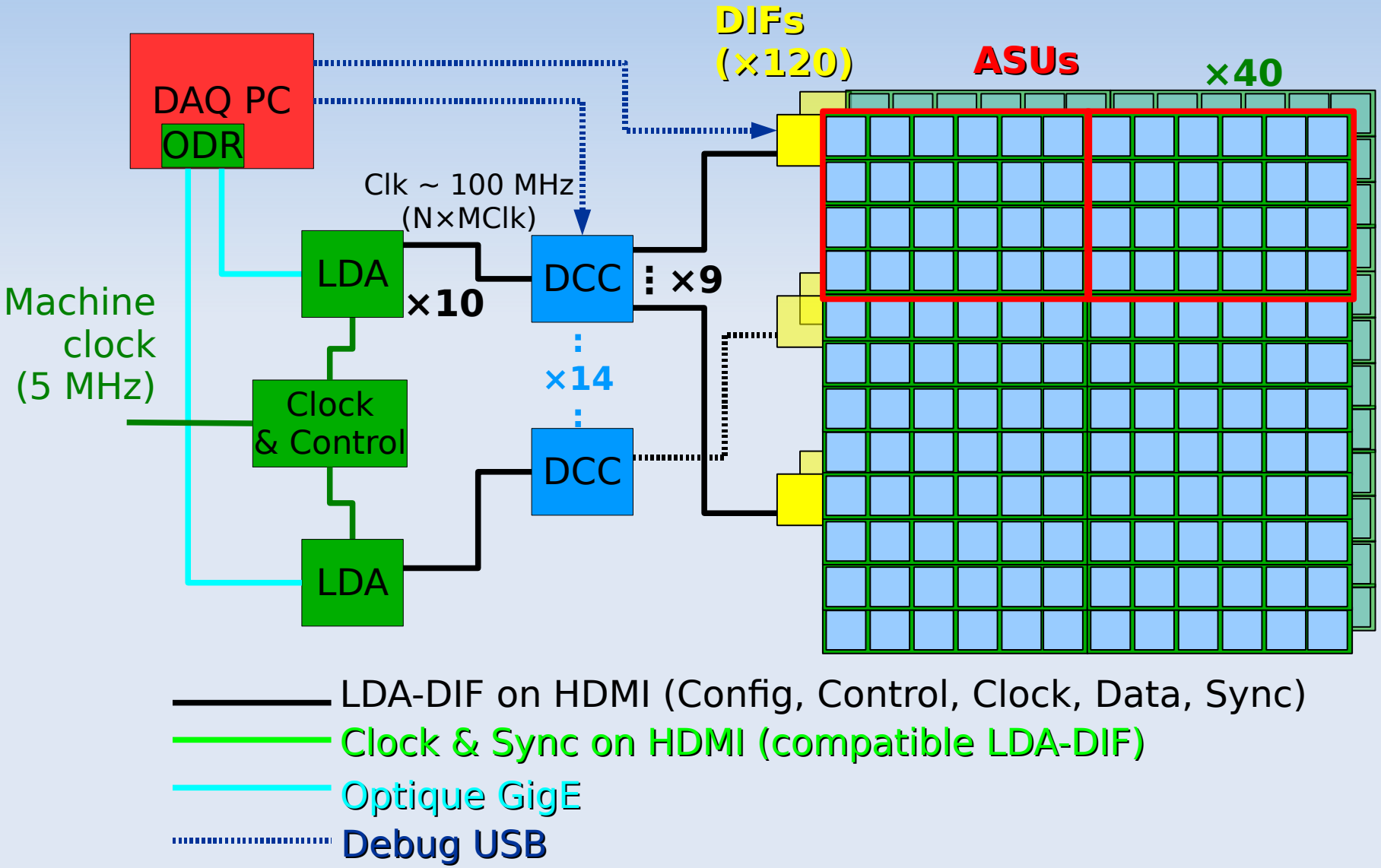
Status of the Data Concentrator Card and the rest of the DAQ

Vincent Boudry
Franck Gastaldi
Antoine Matthieu
David Decotigny

DHCAL meeting

20 jan. 2009
LLR

EUDET DAQ2 for the DHCAL

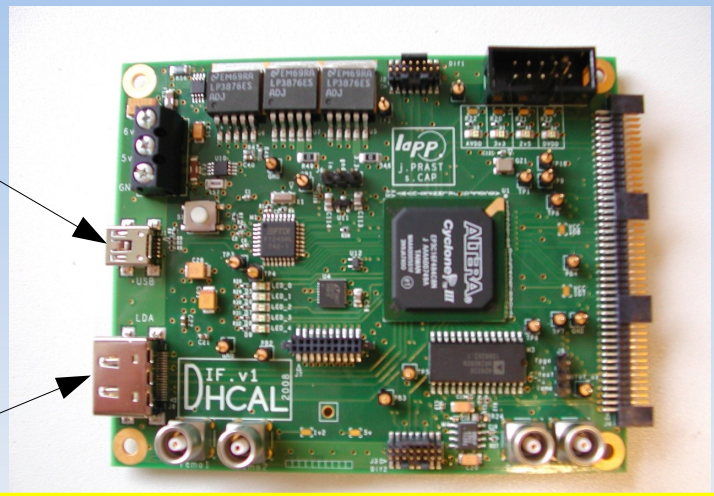


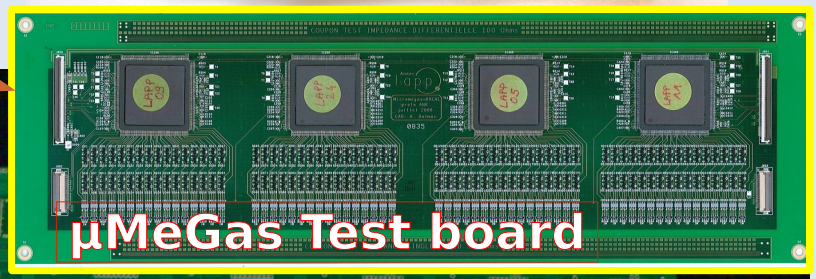
The 1 m² electronics (quick status)

Julie Prast & Guillaume Vouters

DIF

- 10-layer board (6 for signals) designed and prototype produced
- FirmWare & SoftWare operationnal and **tested in beam** (with 4 HR µMegas card)



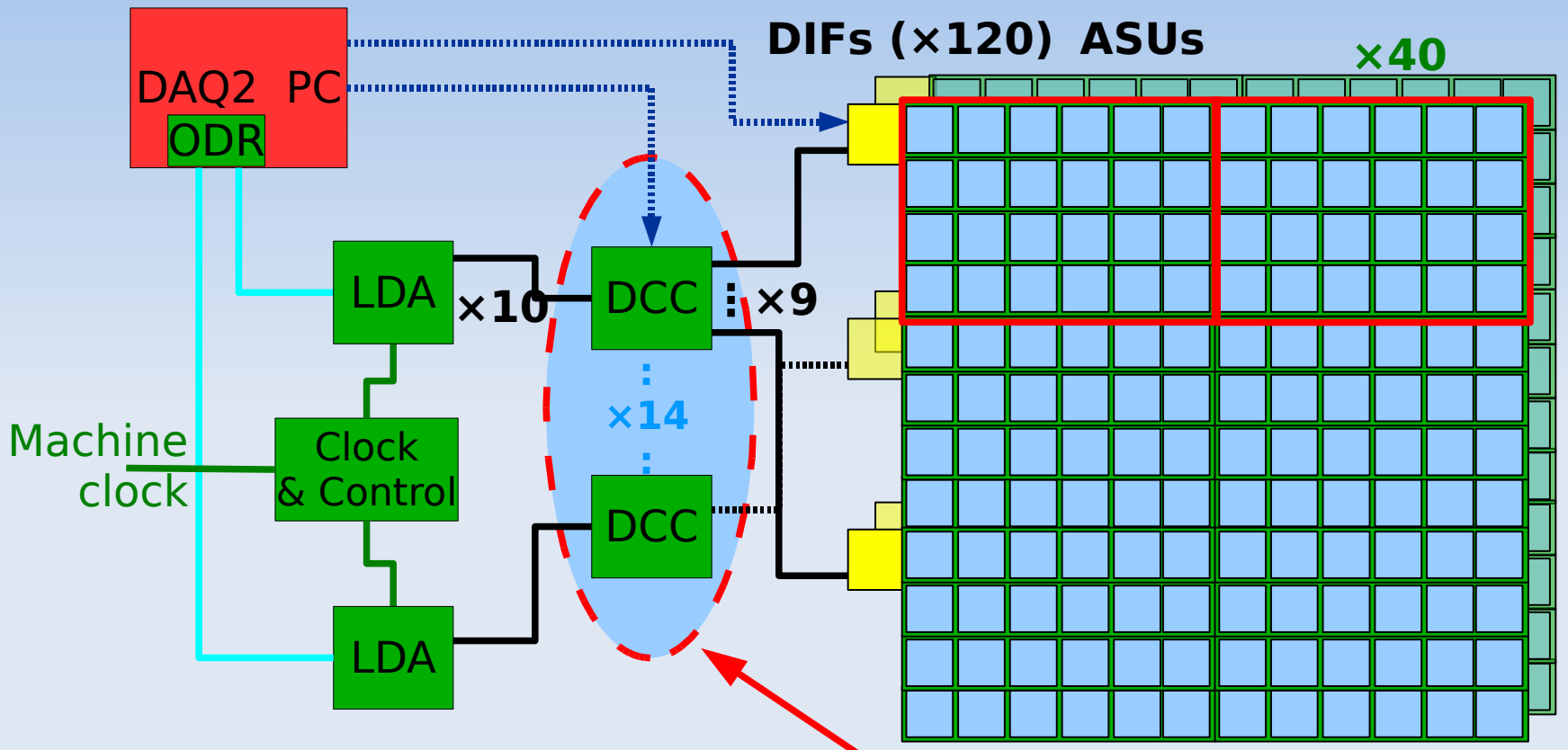


ASUs

- RPC: 50×33.3 cm² (24 HR) boards produced & tested
- μMeGas 32×8 cm² 4 HR produced and tested
- HR1 ASICs used

μMeGas + 4 HR ASU + DIF TB ***data available***
⇒ not yet analysed

EUDET DAQ2 for the DHCAL



120 DIF → 12 LDA → 4 ODR

120 DIF → 14 DCC → 2 LDA → 1 ODR

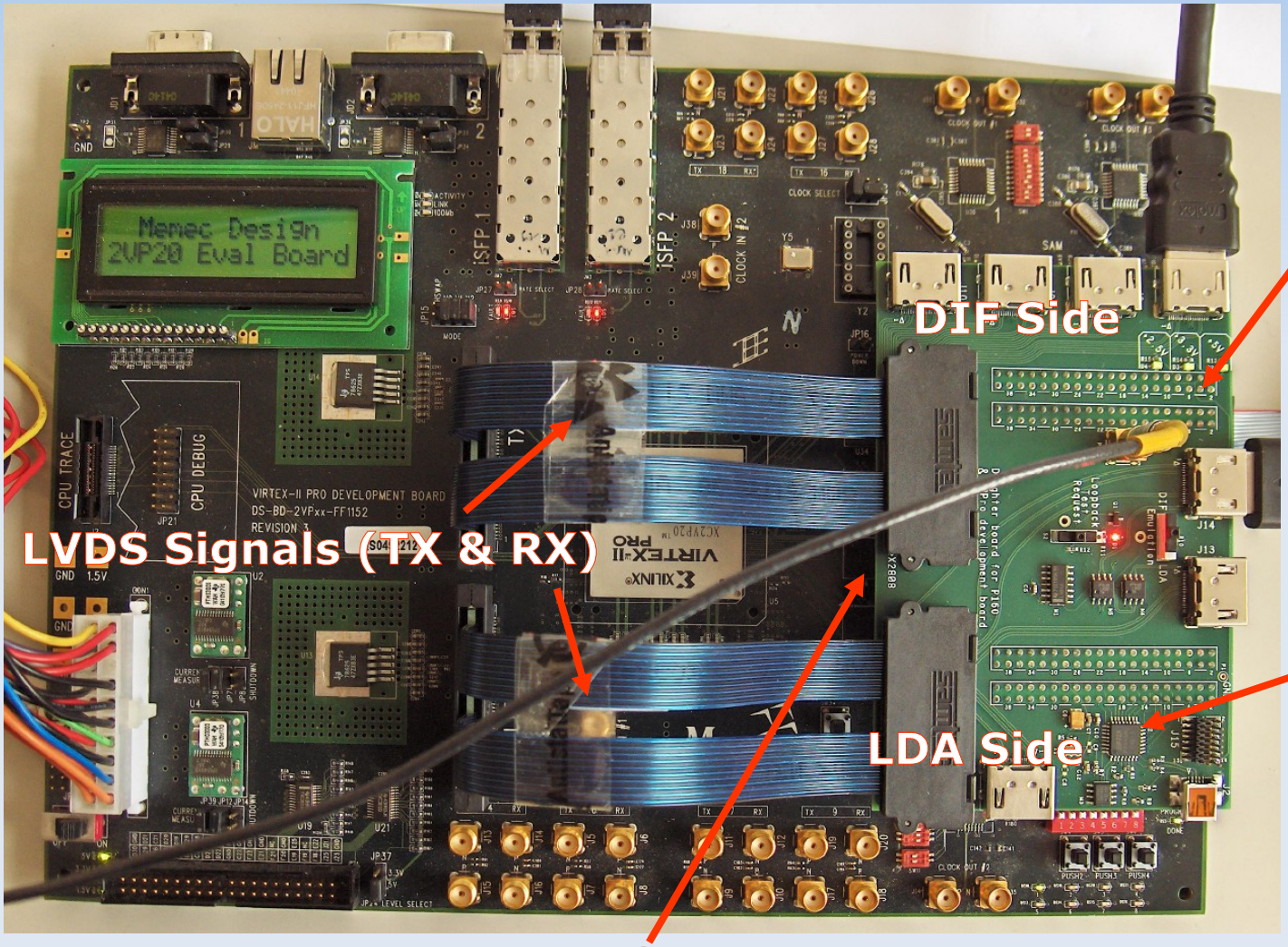
Gain for DCC ≤ 1600€

Carte DCC

Goals
- Transparency on the path DIF-LDA
- Optimization of flux
- Low cost

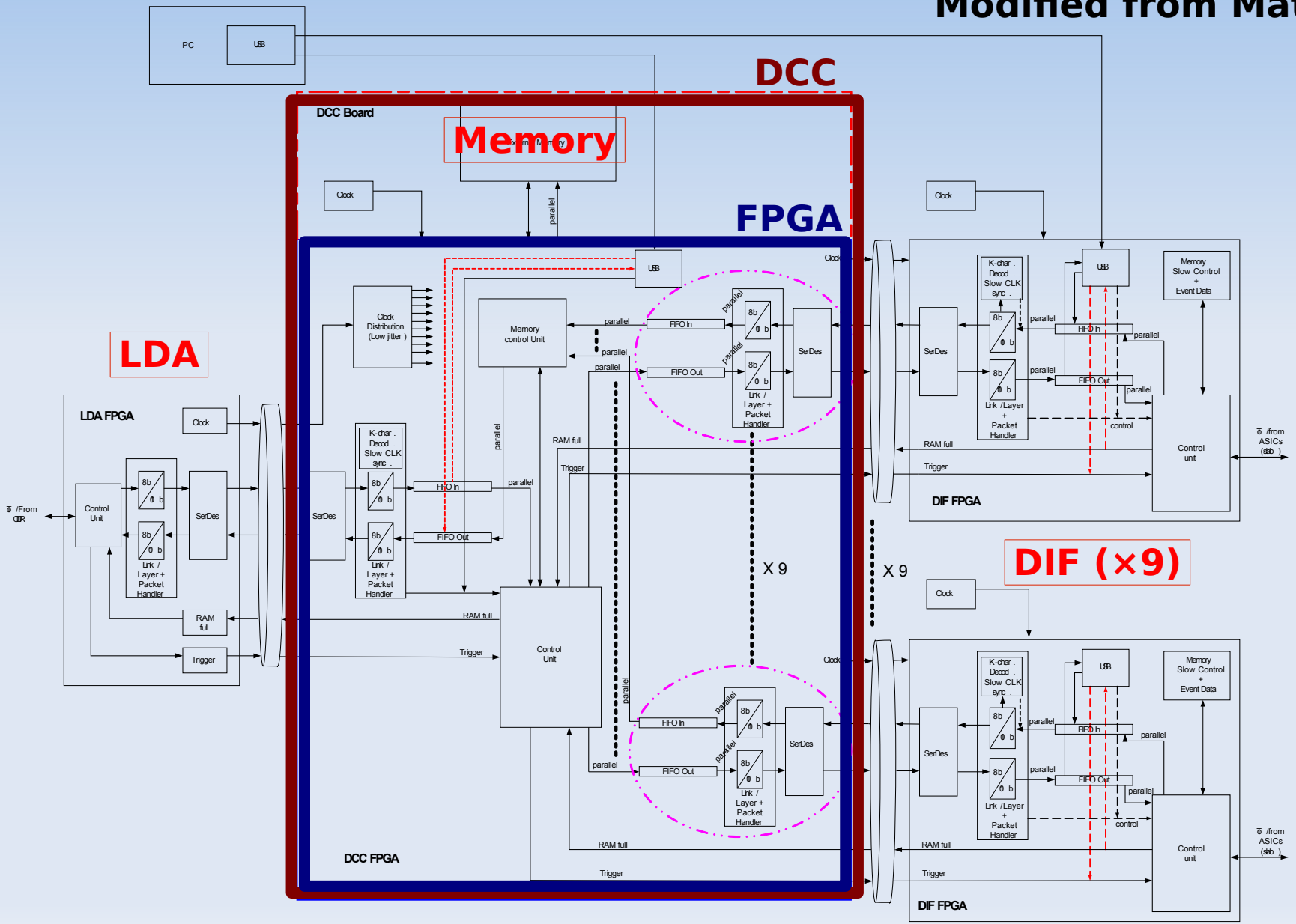
- Pre-proto (proto-0)
  - 4 DIFs connections
  - Implantation et tests du code VHDL
- Based on a XILINX evaluation board:
  - 128 Mbits SDRAM
  - Daughter board:
    - HDMI connecteurs
    - USB blocs
- **Développements**:
  - Marc Kelly (U. Man) : blocs Ser-Des, coding 8b/10b
  - USB blocs (Clément Jauffret)
  - Original VHDL blocs:
    - Memory controller, commands, buffers (FIFO),.....)

Franck Gastaldi
Antoine Matthieu

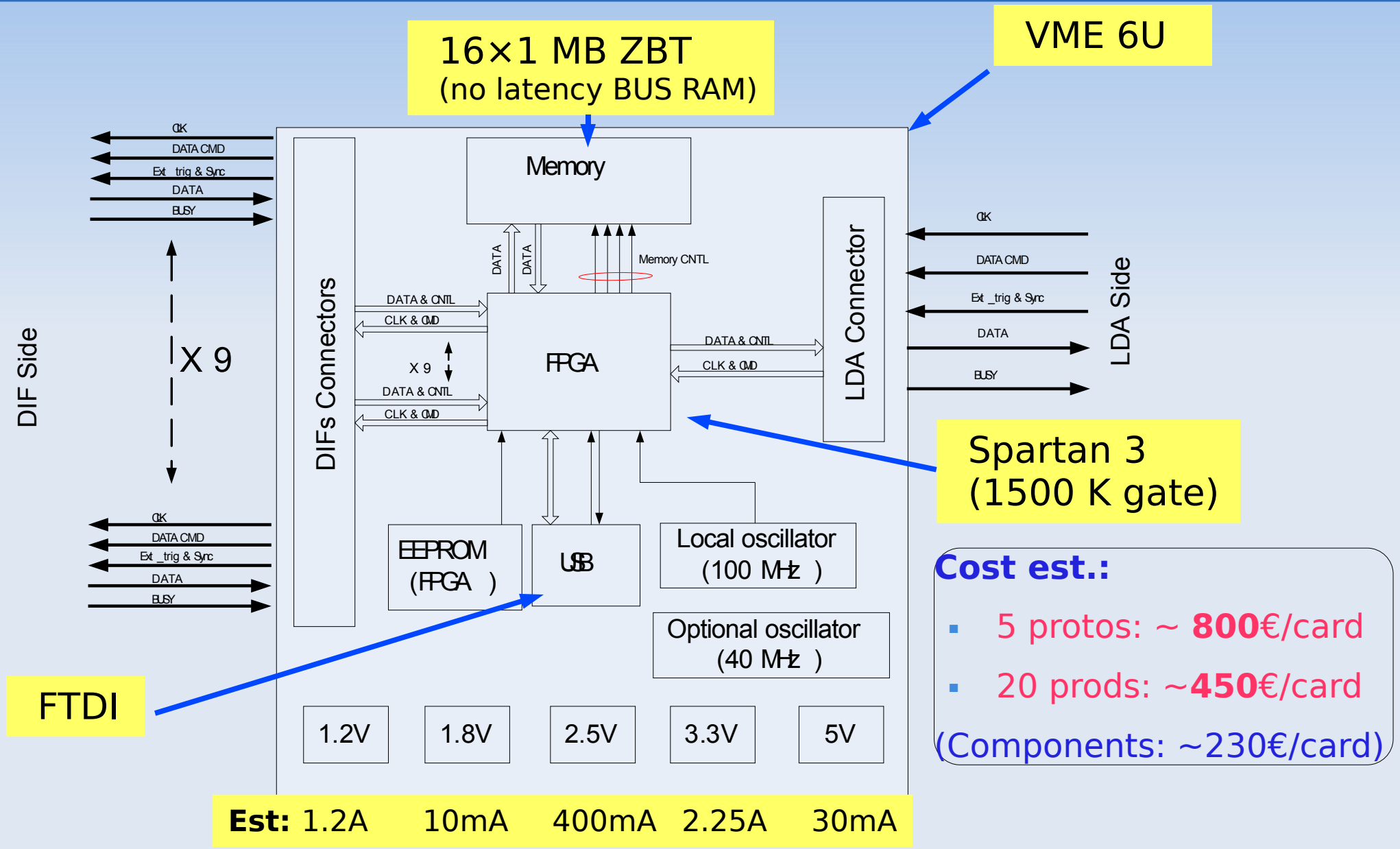

Daughter board
DIF Side
LVDS Signals (TX & RX)
USB part
LDA Side
MEMORY
Memec Design
2VP20 Eval Board
VIRTEX-II PRO DEVELOPMENT BOARD
DS-BD-2VPxx-FF1152
REVISION 3
CPU TRACE
CPU DEBUG

DCC prototype data flux

Modified from Matthias



DCC Proto-1



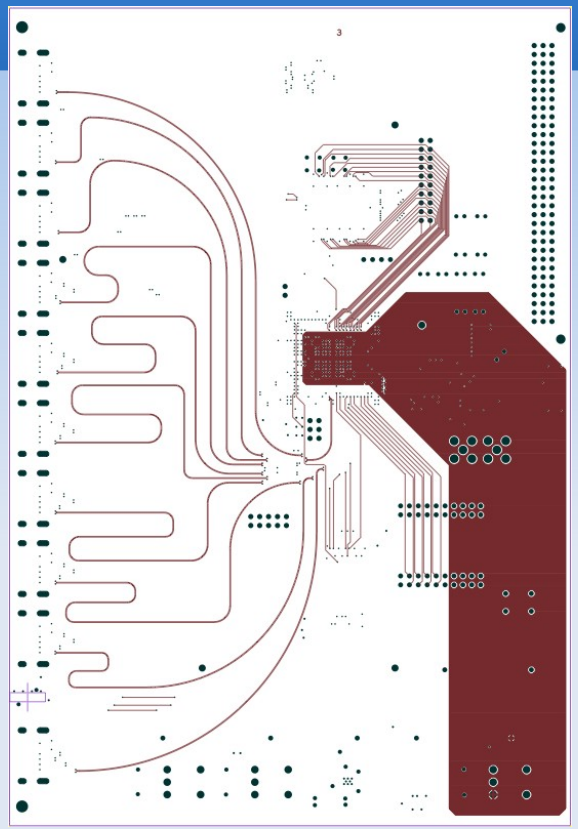
Cost est.:

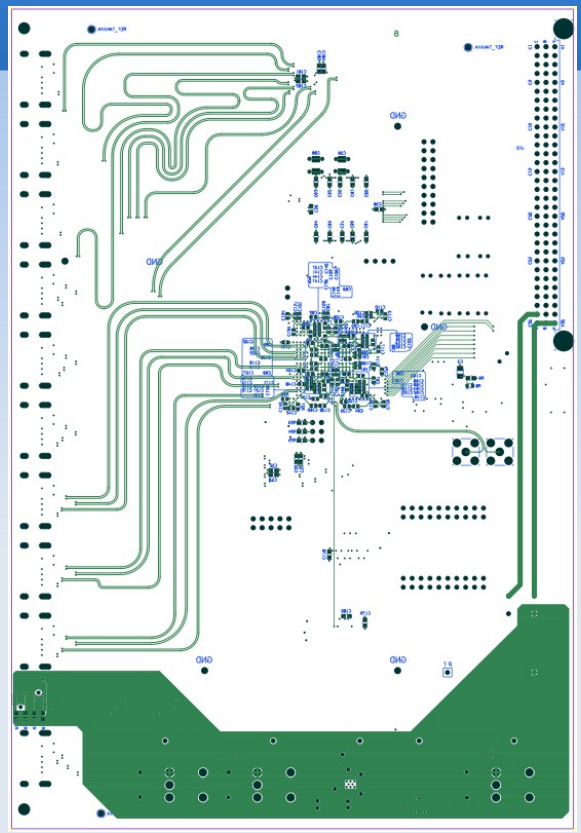
- 5 protos: ~ **800**€/card
- 20 prods: ~**450**€/card

(Components: ~230€/card)

Planning DCC

- January 09:
  - Finalisation of Schematic and routing of PCB
    - equal length of lines
    - inversion of diff lines





- January- April 09
  - Fabrication of prototype
  - Test bench mounting
  - Validation & integration of VHDL blocs
- Mai – June 09 (estimation)
  - Production of boards for the m^3

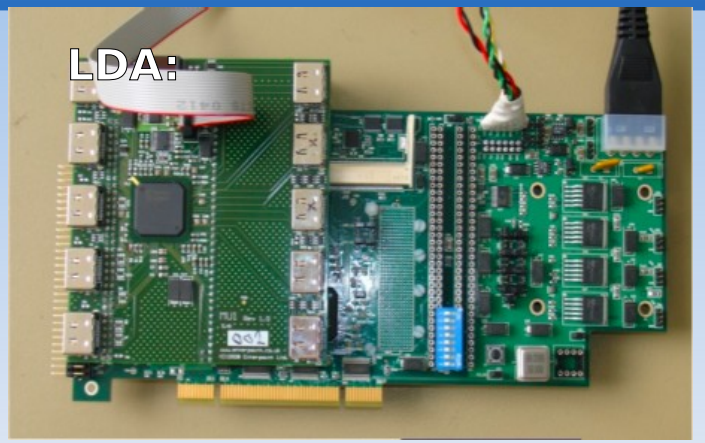
→

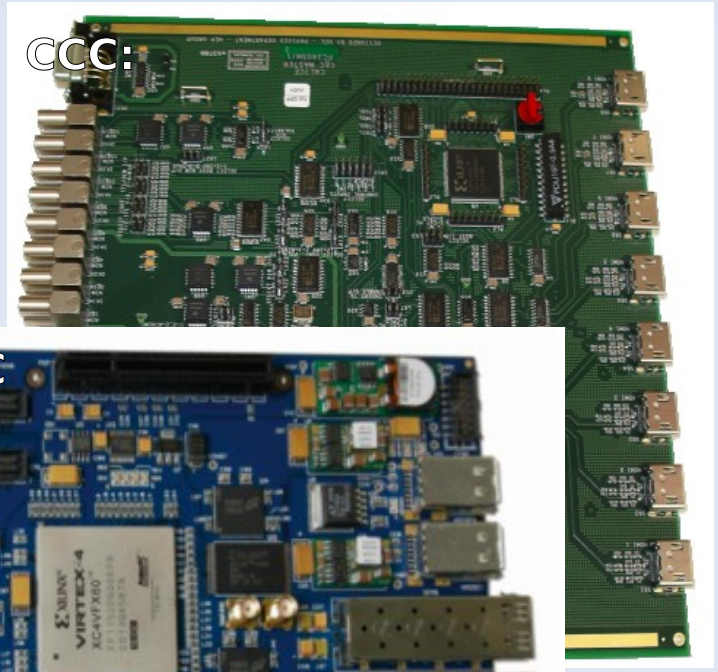
- Looping DCC-DIF / DCC-LDA
- Connection with the DIF (code on DIF: started)

DAQ2 Hardware: status of 12/12/08

http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=3196

- Components:
  - 1 Proto-DIF ✔, ECAL DIF (5 protos) ✔
    - Integration code LDA-DIF on going
  - 1 LDA (HW ✔, FW ongoing)
  - 1 CCC ✔ (2 cards avail., 8 more in prod)
  - 1 ODR v2 + 1 PC DAQ ✔ (mid feb.)
  - 1 proto DCC (march) or proto-0
- HW and protocoles: on-going → March ?
- Mars 09 →Jun 09
  - DAQ code DOOCS
  - Integration for a m³
    - Config Database (calib)
    - Slow Control, Event Display
    - Raw online analysis
    - SLCIO data writing





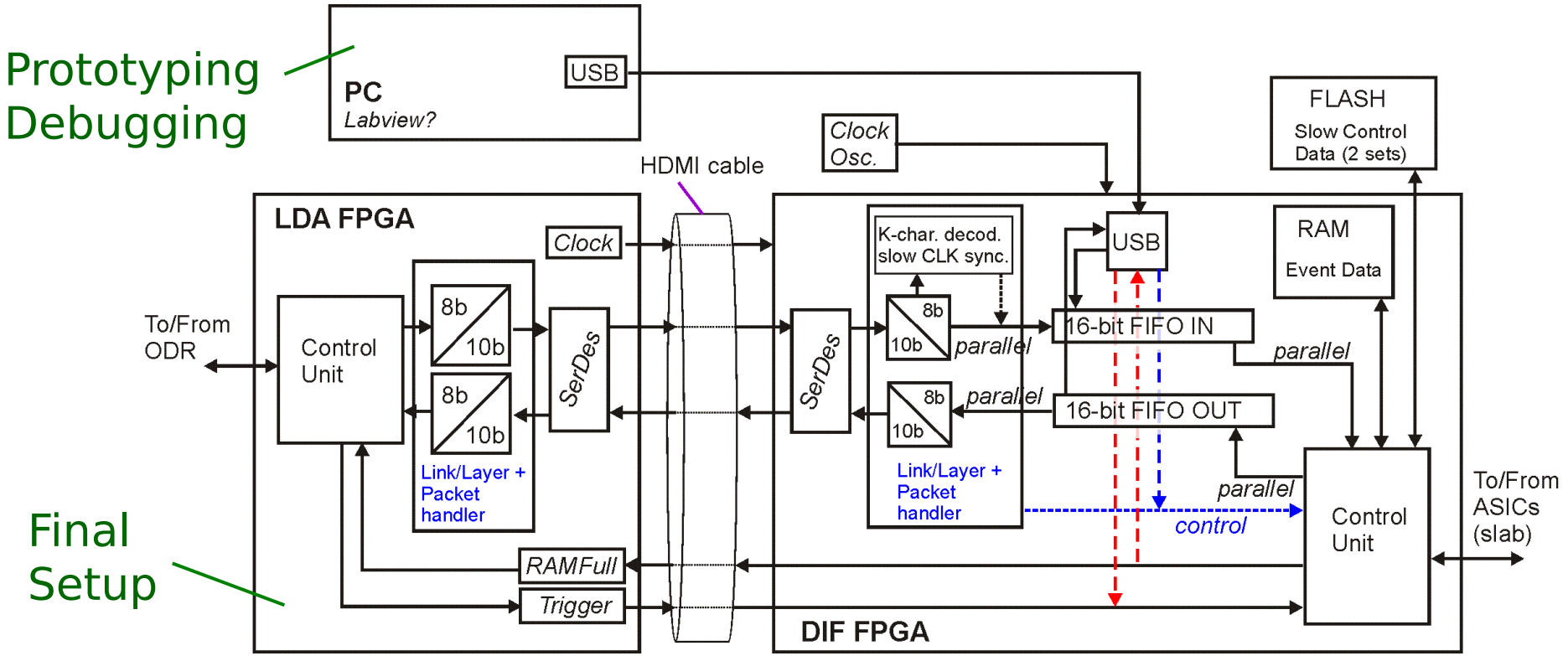
DAQ2 FW components

- DIF code (Many)
  - integration of DIF-LDA module
- LDA code (M. Kelly)
  - Ethernet OK
  - DIF code OK
  - Middle part on-going

DIFs Commands/Protocole:

- User Manual being written
  - See M. Reinecke presentation
  - fast commands
    - sync, start/stop ACQ, trigger, reset BCID
    - specific commands for CALOs and DCC
  - Slow commands and Data transfer
    - power, reset, modes (sleep/idle), power pulsing
- Data format → LDA ~fixed
- DIF code sharing can start...
- Addressing still needs clarification

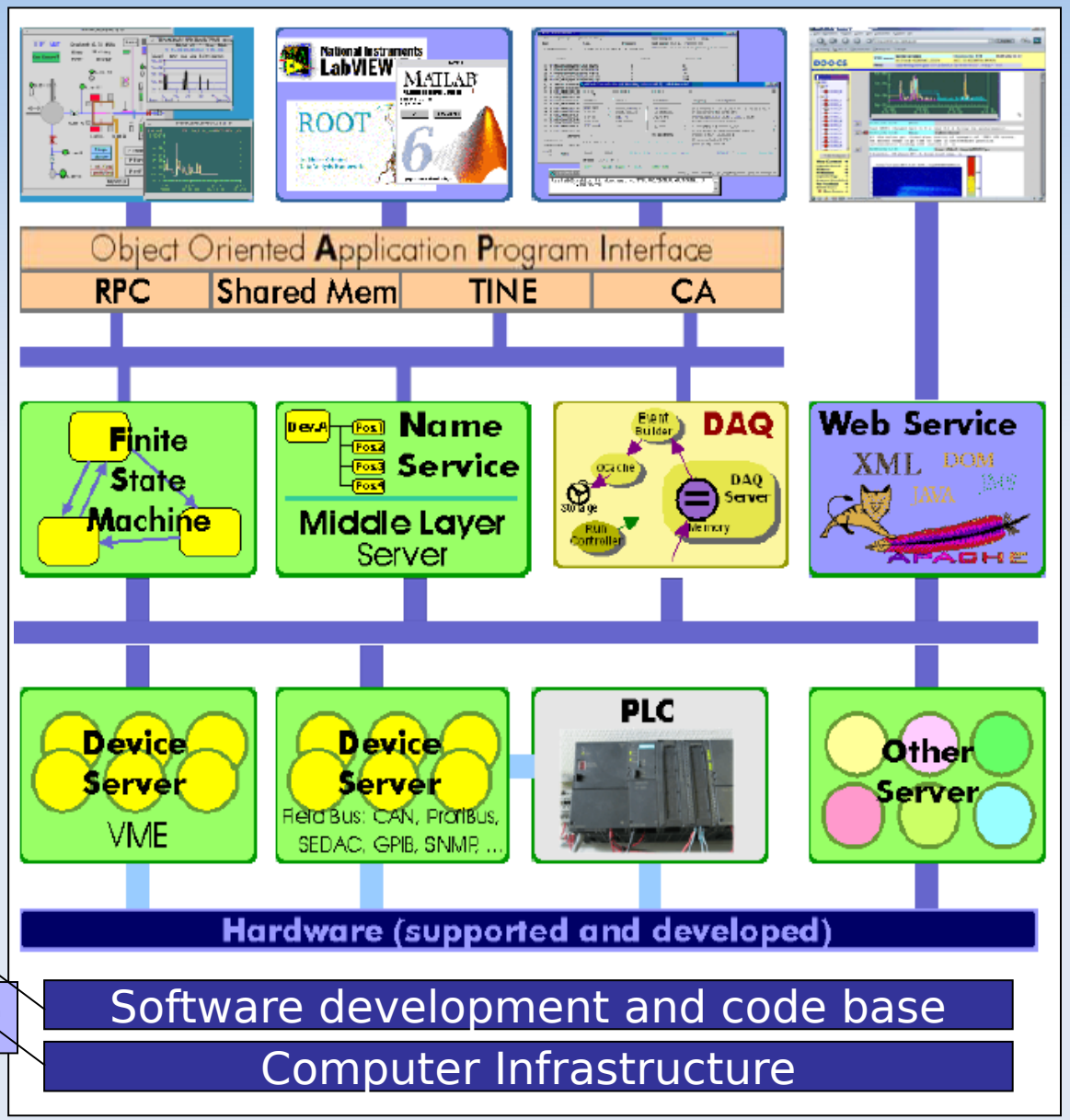
Command Interface - Structure



- DIF clock (from LDA): 100MHz (40-120MHz).
- Standard data transfer: 8b/10b channel-coding.
- Trigger/RAMFull: uncoded.

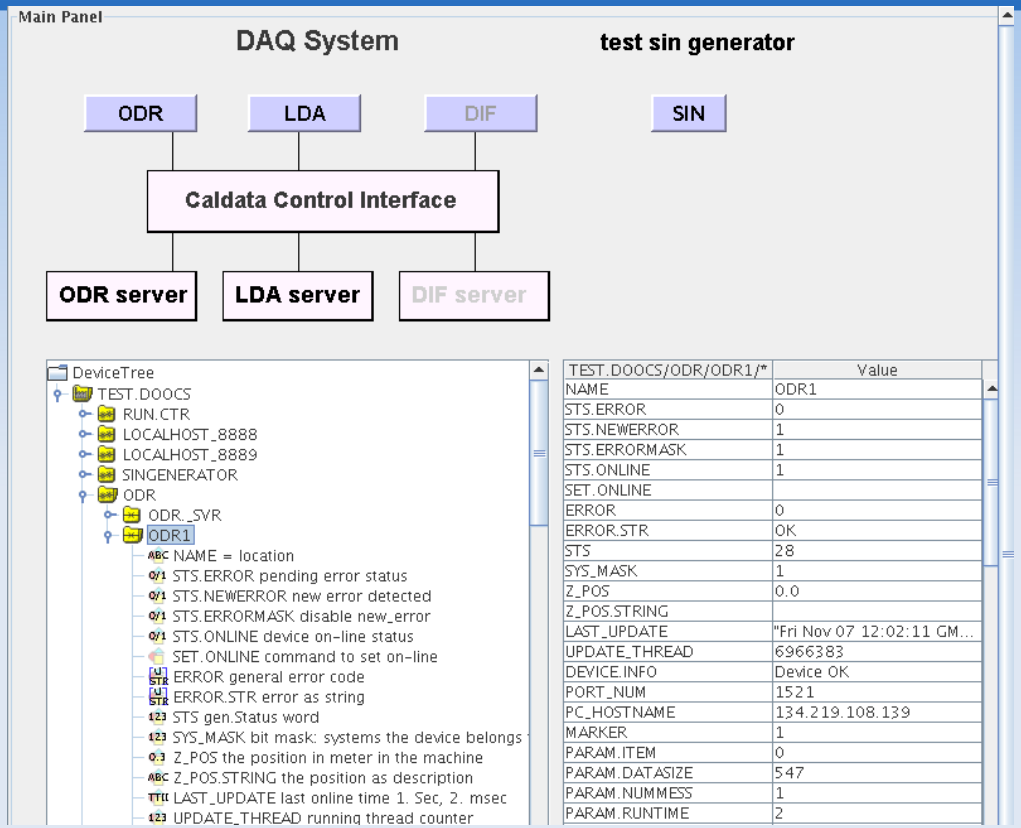
USB interface emulates LDA interface (clock-source: free of choice).

DAQ2 SW components: DOOCS



DAQ SW components: DOOCS

- Drivers: ODR √ vers 2 ongoing
  - Used to test an emulated LDA
  - LDA, DIF, DCC: **not yet**
  - CCC: just started with HW
- Prototype DB for cards (LDA, DCC, DIF, ASICs) parameters (Valeria Bartsch)



DOOCS DAQ running with ODR
• no state machine yet

Current status of database

- Choice of database: MySQL;
- Entity diagrams has been made;
- Use cases has been made and evaluated;
- database is populated with mockup data;
- C++ connector wrapped by MySQL++ to be built in DOOCS framework.

Optional solution !

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DAQ2 SW To do's & Timeline

Some essentials

- The components are not integrated in software,
  - LDA / DIF / ASICs
  - Full chain will be available ~Jan/2009.
- No event building & LCIO converting
  - Data are saved to local disk in raw format;
  - Just provide interfaces in the framework;
  - More flexible way to leave them free for sub-detector groups to develop.

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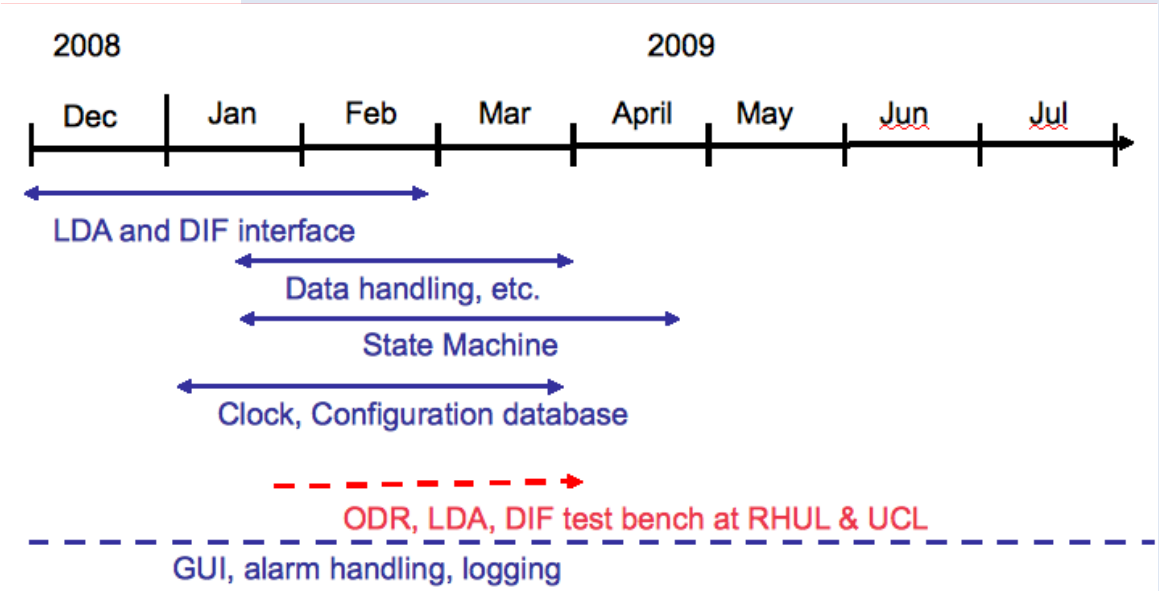

DAQ2 test benchs

- Meeting 12/12/2008 in DESY: needs of various groups
- 1st bench in UK: being build
- 1 bench in LLR:
  - DAQ PC + ODRv2 mid-February **D. Decotigny**
    - now: PC + DCC pre-proto
  - test with USB connection on DCC, Debug DIF → for cosmic test
    - scripting (python ?)
  - integration of all DOOCS components
    - LCIO data writing
    - Event display
    - Database integration with LCDB (MySQL based)
    - Slow Control

REM: knowledge passing ASAP

Summary

- All HW component for the DAQ are now available
  - some need extra prod (LDA, CCC)
  - DCC is advancing well according to planning
    - test prod this month (3 wks)
- FW: on-going everywhere
  - DHCAL DIF OK for USB but needs integration of DIF-LDA blocks
  - Effort of DIF Task force to write modular code on-going
  - LDA & DCC in intensive development
  - Protocol definition crystallising
- SW: Almost full skeleton working
  - integration of HW started
  - needs implementation in a real test bench with real objects (in part. ASICs) → @ UCL and LLR soon
- Good hope for full working system at end of spring